The Design of High Gain Amplifier with Transformer Feedback Combination

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Abstract—In this paper, we present a low power consumption and high gain low noise amplifier based on transformer feedback to neutralize the gate-source and gate-drain overlap capacitance of a FET. It is a single-ended amplifier designed in 65nm CMOS technology for 60 GHz transceiver. This LNA achieves a simulated gain of 10.64 dB, noise figure of 3.10 dB at 60 GHz.

Keywords—CMOS, Amplifier, mm-wave, transformer-feedback

I. INTRODUCTION

For short-range and high data rate wireless transmission demands, mm-wave communication has been attracting tremendous interest recently. The frequency range drawing most attention is the unlicensed 60 GHz band that offers several GHz bandwidth for multi-Gb/s data transmission. Owing to the rapid progress in technology, CMOS has become the most promising technology to realize a fully-integrated 60 GHz transceiver. In the receiver end of a 60 GHz system, the low-noise amplifier (LNA) that must provide high enough gain and low enough noise figure (NF) with low DC power is crucial to the overall system performance. The CMOS LNAs designed for 60 GHz operations have been published [1]–[7]. Many of the previous reported LNAs are based on the conventional transmission-line matching networks, which occupy a relatively large chip area even at 60 GHz. In contrast, the design approach with lumped spiral inductors is more area-efficient. This paper designs a transformer-feedback 60 GHz LNA with low-power consumption by 65 nm CMOS. The transformer feedback technique has been widely used for the LNA design in different applications, but mostly at relatively low frequencies [8]–[11]. Compared with the design using spiral inductors, making good use of this technique can not only enhance the circuit performance due to the feedback of the transformers but also entwine inductors to further reduce the chip area. In this design, gate-source transformer-feedback techniques are employed in a single stage common-source topology to achieve a low-power and compact LNA with good gain and noise characteristics.

II. GATE SOURCE FEEDBACK

A. Gate-source feedback

The small signal model for the general gate-source feedback common source (GSFB-CS) circuit is shown Fig.1.

The GSFB-CS transformer based amplifier has a dual feedback structure, with inductor L2 providing series-series feedback and a transformer comprised of the coupled inductors L1 and L2 providing series-shunt feedback. Using a conventional expression for the transformer while applying KCL and KVL,

\[
\begin{aligned}
V_m &= \begin{pmatrix}
sn^2 L_2 & -k_m n s L_2 \\
k_m n s L_2 & s L_2 
\end{pmatrix}
\begin{pmatrix}
I_1 \\
I_2
\end{pmatrix} \\
I_m &= I_1 + s C_g (V_m - V_s) \\
Y_o &= g_o + s C_o \\
I_2 &= (V_m - V_s) (g_o + s C_g)
\end{aligned}
\]

From (4) and defining \( \alpha = C_o / C_g \) and \( L_2 = L_1(1-k_m^2) \), it can be shown that

\[
\frac{V_o}{V_m} = \frac{(g_o + s C_g) s L_{21} - \frac{k_m}{n}}{1+(g_o + s C_g) s L_{21} + s^2 \left( C_o + C_g \right) L_{21}}
\]

\[
\alpha^2 (1+\alpha) C_g L_{21} = 1
\]

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If the transformer is assumed to operate in resonance (6), then using (5) an expression can be obtained for the input admittance, \( Y_{\text{in}} \), at frequencies close to the carrier \( \omega_c \). The impedance looking into the SGFB-CS stage is a parallel resonant network with a matched impedance at \( \omega_c \) given by (7). This expression is valid for the practical condition, \( k \neq 1 \). When \( k = 1 \), the leakage inductance \( L_{21} = 0 \) and (6) is no longer valid.

\[
Re(Y_{\text{in}}) = \left( \frac{k_m}{n} \frac{1}{1+\alpha} \right)^2 \left( g_m + g_n \right)
\]

(7)

B. Gate-drain feedback

The gate-drain feedback common source (GDFB-SC) topology was first introduced in [6] as a technique to neutralize the gate-drain overlap capacitance, \( C_{gs} \), thus improving the stability of the amplifier. From Fig. 2, expressions can be derived for the input admittance (8) and voltage gain (9) of the circuit.

\[
\frac{I_m}{V_m} = s(C_{gs} + C_{sh}) + \frac{Y_m n^2 + g_m nk_m}{1 + sL_1 Y_m (1 - k_n^2)}
\]

(8)

\[
\frac{V}{V_m} = \frac{g_msL_2 + k_m}{1 - g_msL_2}
\]

(9)

\[
\omega L_2 Y_m (1 - k_n^2) < 1
\]

(10)

While possible to achieve a \(|S11| < -10\text{dB}\) over a wide bandwidth, the GDFB topology has limited applications because of the difficulty in achieving, simultaneously, both a high voltage gain and a 50 \( \Omega \) input match. Assuming, \( g_m \) is high, (10) indicates that \( n > 1 \) is desired for input matching, whereas to obtain a voltage gain, (9) requires \( n < 1 \).

III. DESIGNED STRUCTURE

Fig. 3 shows the circuit schematic of the proposed transformer feedback LNA, which is composed of single-ended common source stages with a transformer feedback configurations. The gate-source transformer feedback at the input stage is used for simultaneous noise and input impedance matching, and improved power gain. An extra strip-line based inductor was used in conjunction with the GDFB to realize the input matching network.

For the LNA designed in a cascade topology, the first stage dominates the overall noise characteristic of the amplifier. Using the transformer with the design parameters of self-inductances (L1 and L2), the mutual inductance (M), and the coupling coefficient (k), the input stage can achieve a simultaneous impedance and noise matching for high-gain and low-noise characteristics. The following equations, derived based on the small-signal model with the assumption of an ideal transformer provide a guidance for the transformer design on achieving input impedance matching to the source resistance \( R_s \) (\( R_s = 50 \Omega \) in this case).

\[
Z_m = \frac{j\omega L_s}{1 - \omega^2 C_{sh} (L_1 + L_2 + 2M) + j\omega g_m (L_2 + M)}
\]

(11)

From (8), the input matching criteria could be derived as

\[
\text{Re}[Z_m] = \frac{1}{g_m} \frac{L_1}{L_2 + M} = \frac{n^2}{(1 + n)g_m} = R_s
\]

(12)

and

\[
\text{Im}[Z_m] = 0 \Rightarrow L_1 = \frac{1}{\omega C_{sh}} \left( \frac{n}{\omega (n+1)} \right)^2
\]

(13)

Besides, the associated noise factor \( F \) can be expressed as

\[
F = 1 + \frac{R_s}{g_m} \left[ 1 - \omega^2 C_{sh} (L_1 + L_2 + 2M) + j\omega L_s / R_s \right] \left[ j\omega (L_1 + M) \right]^2
\]

(14)
where $\gamma$ is the channel noise parameter. Equation (6) indicates that $F$ can be lowered by increasing $n$, and noise matching is wideband as $F$ is independent of frequency ($\gamma$ is a constant). Note that $g_m$ is also a critical design parameter for input matching as can be seen from (11). A large $g_m$ is required for input matching if a large $n$ is used, but which could result in increased power consumption PDC or transistor size. In practical design, tradeoffs exist among $g_m$, PDC, and parasitic capacitances of the input transistor. Also, the coupling coefficient $k$ and the quality factor $Q$ of the transformer should be considered.

The proposed 60 GHz LNA is simulated in a TSMC 65 nm CMOS technology. The transistor of the single stage is designed to obtain a large enough transconductance. In addition to the gate-source transformer, a drain inductor is used for gain peaking and interstage matching. For lowering the power consumption and parasitic capacitances, the transistors of the additional stages are chosen with a smaller size and bias current. The details of transistor sizes and bias conditions of LNA are shown in Fig. 3.

The inductor and the transformer in the circuit are all designed by Metal 9 and Metal 8, and simulated rigorously by the EM simulation tool HFSS. The inductances and the coupling factors are designed according to the tradeoffs among the impedance and noise matching, gain, and bandwidth. The gate-source transformer is designed using vertical coupling between Metal 9 and Metal 8, which is more effective than lateral coupling design. Note that the grounded-coplanar waveguide (GCPW) configuration is used for all the signal paths to minimize the signal loss and interference from the substrate.

In this design, ADS is used to simulate circuit and HFSS is used to simulate the transformer. We compare designed LNA with general LNA.

Fig. 4 shows simulated gain results of designed LNA and general LNA. At 60 GHz, The designed LNA has a 10.64 dB gain which is about 3.17 dB higher than of general LNA. The gain flatness is about 1.57 dB with a 6 GHz bandwidth.

Fig. 5 shows simulated noise figure results of designed LNA and general LNA. At 60 GHz, The designed LNA has a 3.10 dB noise figure which is about 1.25 dB lower than of general LNA. The deviation of noise figure is about 0.28 dB with a 6 GHz bandwidth.

IV. CONCLUSION

In this paper we designed a gate-source feedback and gate-drain feedback common source transformer 60GHz LNA with low power consumption and high gain. The transformer matching technique enables the full integration of the transformer matching network on-chip while it also exhibits a low noise figure. Simulations of a LNA have been done verifying this matching technique. The amplifier achieved a
maximum gain of 10.78 dB with a 6 GHz bandwidth, and a minimum of noise figure of 2.98 dB.

REFERENCES


