Extended CPM for System Power Integrity Analysis

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Abstract— Power integrity (PI) co-analysis of Chip-package-system (CPS) is a powerful tool to accomplish the extremely challenging goal; lower cost but better performance. However, the conventional PI analysis of CPS using chip power model (CPM) has limitations on the design evaluation and optimization of board and package. In this paper, we demonstrate the limitation first and share our experience on the development of PI analysis flow using Extended CPM (ECPM) technique on CPS to overcome the limitation.

Keywords—component; Power Integrity, PI, Chip power model, CPM, ECPM, Extended CPM

I. INTRODUCTION

The competitive mobile AP market has forced designers to accomplish the extremely challenging goal; lower cost but better performance. One of the important breakthroughs to get closer to the goal is chip-package-system (CPS) co-analysis [1]. It aims to enable mobile AP system designers to find and minimize overdesigns which could never be found from an optimization of each individual level of chip, package and board. The first and most important step of CPS co-analysis is an accurate modeling of the chip operation. Particularly for power integrity (PI) analysis, the chip power model (CPM) from RedHawk, Apache Solutions Inc., is one of good solutions. It is a compact and highly accurate electrical representation of a chip in various operating scenarios. It expresses a characteristic of chip operation in a form a piecewise-linear (pwl) time-domain current and parasitic RC components seen at chip bumps or wire-bonding pads [2]. Then, by stacking of board, package PDN model and CPM, we could composite a complete platform for the PI analysis of a system.

However, PI analysis of CPS using CPM still has limitations. The most important one is the insufficient modeling of low and mid-frequency characteristic of chip operations in CPM. It makes PI optimizations of board and package designs of a mobile AP system very difficult. To resolve these difficulties, we propose the PI analysis of CPS using Extended CPM technique in this paper. In this paper, we demonstrate the limitation of PI analysis of CPS using CPM. Then, the concept, generation, application flow and verification of Extended CPM are introduced.

II. LIMITATION OF SYSTEM LEVEL PI ANALYSIS WITH CPM

System designers of mobile AP are struggling for low power design. Power gating, clock gating and dynamic voltage/frequency scaling (DVFS) are those techniques to maximize the power efficiency of a system. Unfortunately, those gatings and DVFS make radical changes on the chip current which could cause a serious simultaneous switching noise (SSN) on VDD. If SSN by them is not well characterized and prepared in a system design stage, increasing the lowest VDD voltage, LVcc, is our last option to guarantee the normal operation of the system under the SSN after the fabrication. In other words, we have to waste additional power.

Table 1 summarizes those low power techniques which possibly cause SSN. Among major 4 items, the most important one we need to care in the PI analysis of CPS using CPM is the clock gating. SSN caused by DVFS and power gating usually have their energy on kHz to 0.1MHz range. It is easily eliminated or compensated by PMIC and rush current control on chip. Therefore, we don’t need to give close attention to it during PI analysis of CPS. The dynamic clock gating is much faster and cause SSN at beyond hundreds MHz. The amount of on-die decoupling capacitor is critical to suppress SSN at

<table>
<thead>
<tr>
<th>Origin</th>
<th>Transition time</th>
<th>Expected freq. component of SSN</th>
<th>Suppression technique</th>
<th>Consideration/Required Model in PI analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVFS</td>
<td>ms order</td>
<td>&lt;kHz</td>
<td>VDD monitoring by PMIC</td>
<td>Not required</td>
</tr>
<tr>
<td>Power Gating</td>
<td>μs to ms</td>
<td>kHz~0.1M Hz</td>
<td>VDD monitoring by PMIC and rush current control</td>
<td>Not required</td>
</tr>
<tr>
<td>Clock Gating</td>
<td>μs order</td>
<td>0.1~100M Hz</td>
<td>BD decap. PKG decap</td>
<td>Required/Not developed yet</td>
</tr>
<tr>
<td>Dynamic Clock gating</td>
<td>ns order</td>
<td>&gt;100MHz</td>
<td>On-die decap.</td>
<td>Required/CPM</td>
</tr>
</tbody>
</table>

Table 1 summarizes those low power techniques which possibly cause SSN. Among major 4 items, the most important one we need to care in the PI analysis of CPS using CPM is the clock gating. SSN caused by DVFS and power gating usually have their energy on kHz to 0.1MHz range. It is easily eliminated or compensated by PMIC and rush current control on chip. Therefore, we don’t need to give close attention to it during PI analysis of CPS. The dynamic clock gating is much faster and cause SSN at beyond hundreds MHz. The amount of on-die decoupling capacitor is critical to suppress SSN at
this high freq. range. Since the CPM includes modeling of the
dynamic clock gating, the amount of required on-die
decoupling capacitor can be determined by PI analysis of CPS
using CPM.

In case of SSN caused by clock gating, it has its energy
between 0.1MHz to 100MHz, which is dominated by board
and package design of a system. Accordingly, board, package
designs and the amount of decoupling capacitors on those
levels are important factors to decide the amount of SSN by
clock gating. However, those factors are hard to be well
evaluated with PI analysis of CPS using CPM due to the
insufficient modeling of low and mid-frequency characteristic
of chip operations in CPM. The time-length of pwl current in
CPM we can generate is often limited to a few hundred ns or
less due to its enormous consumption of time and computing
resource. This is too short time for even rough capturing of
low and mid frequency characteristic of chip operation, such
as the clock gating operation.

Figure 1 show two examples of CPM current in time and
frequency domain. In these cases, the frequency domain plot
show that CPM do not contain low frequency information of
chip operation; <1GHz and 200MHz in these examples,
respectively. Accordingly, CPM does not provide the enough
information for the evaluation impacts of board, package
designs and the amount of decoupling capacitors on SSN by
clock gating. Figure 2 shows the self-impedance ($Z_{11}$) at chip
bump in the frequency domain and VDD in time domain as
the result of PI analysis of CPS using CPM. While the
different number of PKG embedded decoupling capacitors
differentiate the magnitude of self-impedance in the frequency
domain, SSN at chip bump in time domain is not showing any
changes in its peak-to-peak value.

III. PI ANALYSIS WITH EXTENDED CPM TECHNIQUE

Even though PI analysis in the frequency domain is useful,
the criteria to judge pass or fail of designs is still defined in the
time domain at the end. Therefore, we have to figure out how
could we enhance PI analysis of CPS with CPM in time
domain for the proper evaluation of board and package
designs in low and mid frequency range.

A. Concept of Extended CPM and its generation

The key of the enhancement is the mimicking of clock
gating operation of chip into CPM. Figure 3 shows that why
the clock gating should be considered in PI analysis of CPS.
Upper plot of Figure 3 shows demand current at a chip bump
with the clock gating operation. The radical changes of the
demand current by state changes
of the chip from idle to run
increase the amount of SSN. If the frequency components of
the demand current changes is overlapped with a frequency of
PDN resonance, which is possibly a resonance generated by
board and package PDN, the SSN increment by clock gating
($V_{pp_CG}$) make the total SSN ($V_{pp_CG}+V_{pp_cpm}$) much larger
than SSN we can estimate with CPM ($V_{pp_cpm}$) due to the
ringing and overshooting as shown in lower plot of Figure 3.

The mimicking of clock gating operation into CPM starts
with the time extension of CPM. At least ms order of time
length is required to proper mimicking of the clock gating
operation. Using pwl current data in CPM as a seed, we
arrange and stitch them in serial. Typical time-extension factor
is between 1000–10000 since the typical time length of pwl
data in CPM is hard to exceed hundreds ns.
Next step is generating a clock gating sequence. The clock gating sequence is time-varying depending on an amount job loading and a power/performance policy of systems. Moreover, the clock gating sequence has nothing like “unit interval” which is defined in jitter/skew analysis in IO channel designs. This non-uniformity of run and idle clock gating states makes defining a worst-case clock gating sequence very difficult. Instead, we had to use a random generation of the clock gating sequence. Multiple parameters have been required on generating a clock gating sequence, such as a rising/falling current slew rate, a time length of run and idle state, a leakage current, a toggle rate and so on. We define design specific ranges for those multiple parameters. Those ranges are also differently defined for each user scenario. Those ranges are randomly combinated within the ranges to composite a clock gating sequence. However, we could not guarantee that the generated clock gating sequence is representing a worst-case. Therefore, we apply an additional statistical analysis to predict a worst-case sequence after the random generation. The statistical analysis is explained in the next part. In the last step, we modulate the time-extended pwl current from the first step with the generated clock gating sequence from the second step. Then, export the new pwl current data in CPM format. We named final output in CPM format as Extended CPM (ECPM). Figure 4 shows the generation flow of ECPM.

Fig. 3. The radical change of demand current by clock gating operations increase the total SSN (Vpp_CPM) much larger than SSN we can estimate with CPM (Vpp_CPM) can be generated

Fig.4. Generation flow of Extended CPM

Fig.5. Demand current in the freq/time domain by a generated Extended CPM at chip bump. Low and mid frequency energy (~100MHz) is enforced in the demand current of ECPM by the mimicking of clock gating.

Fig.6. Estimated SSN with the generated ECPM (Vpp_ECPM)
Figure 5 shows an example of ECPM. We can clearly identify the run and idle states in the demand current of ECPM at a chip bump. We verified the modulated clock gating sequence makes the current energy on the low and mid frequency (<~100MHz). Especially, the energy is highly concentrated below 10MHz. In that region, PDN impedance is usually dominated by the board and package designs. Accordingly, we could expect that PI analysis of CPS using ECPM enables us to see an impact of board, package designs and decoupling capacitor changes on SSN.

Figure 6 shows the estimated SSN from PI analysis of CPS using the generated ECPM. We verify that SSN from ECPM ($V_{pp,ECPM}$) is much larger than SSN from CPM ($V_{pp,CPM}$). As already mentioned, the increment of SSN comes from the ringing and overshooting of VDD due to the radical current change during run/idle state change of clock gating.

B. System PI evaluation with Extended CPM

We performed the system-level PI analysis with Extended CPM to see it overcomes the limitation of CPM. We want to verify how well ECPM helps to predict the impact of PKG design difference on the amount of SSN on chip PDN. Four designs are prepared which have the same silicon and evaluation board but different PKG designs (# of PKG embedded decap). Figure 7 shows HSPICE simulation results of $Z_{11}$ at a chip bump and time-domain supply noise with ECPM of the test cases with different number of PKG embedded decap. $Z_{11}$ at a chip bump shows that there is the clear difference on $Z_{11}$ originated from the PKG design difference. The normalized difference of $V_{drop}$ from HSPICE transient simulation of those test cases are summarized in the Table II. $V_{drop}$ represents the amount of maximum voltage drop from nominal VDD. As we expected, the analysis with ECPM successfully captures the difference on $V_{drop}$ in the time-domain due to PKG decap changes while the analysis with CPM does not. The analysis result with ECPM clearly reveals that using 3 PKG embedded decap was overdesign.

IV. Conclusion

To accomplish a low cost but high performance system design, now, we have to search through any tiny hidden room for the design optimization at the every level of system, board, package and chip, from PI co-analysis of CPS. However, even that has a limitation on the PI analysis and optimization of board and package designs, we have developed the PI analysis of CPS using Extended CPM (ECPM). This paper introduced the limitation of PI analysis with CPM. Then, the key concepts of the ECPM technique, the time-extension and mimicking of a clock gating operation of a chip, is introduced. From the test system PDN with different PKG PDNs, we verified that the PI analysis with ECPM successfully captures the difference in supply noise from PKG PDN changes while analysis with CPM does not.

References