ECE 342

Review

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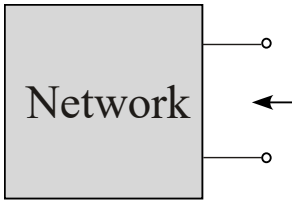
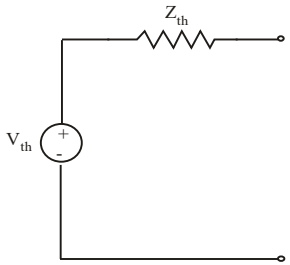
Thevenin Equivalent



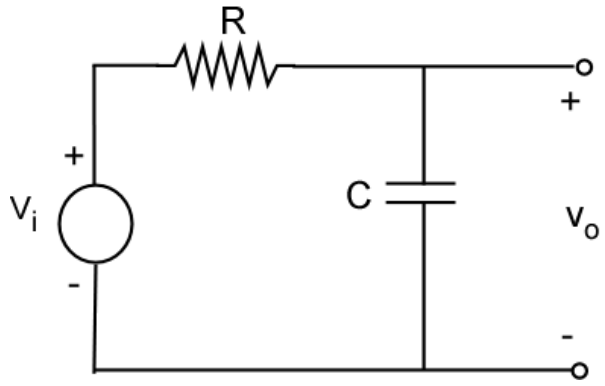


- **Principle**
  - Any linear two-terminal network consisting of current or voltage sources and impedances can be replaced by an equivalent circuit containing a single voltage source in *series* with a single impedance.

- **Application**
  - To find the Thevenin equivalent voltage at a pair of terminals, the load is first removed leaving an open circuit. The open circuit voltage across this terminal pair is the Thevenin equivalent voltage.

  - The equivalent resistance is found by replacing each independent voltage source with a short circuit (zeroing the voltage source), replacing each independent current source with an open circuit (zeroing the current source) and calculating the resistance between the terminals of interest. Dependent sources are not replaced and can have an effect on the value of the equivalent resistance.

Low-Pass Circuit



In frequency domain:

$$V_o = \frac{V_i}{R + \frac{1}{j\omega C}} \cdot \frac{1}{j\omega C}$$

$$V_o = \frac{V_i}{1 + j\omega RC} \Rightarrow A_v = \frac{V_o}{V_i} = \frac{1}{1 + j\omega RC}$$

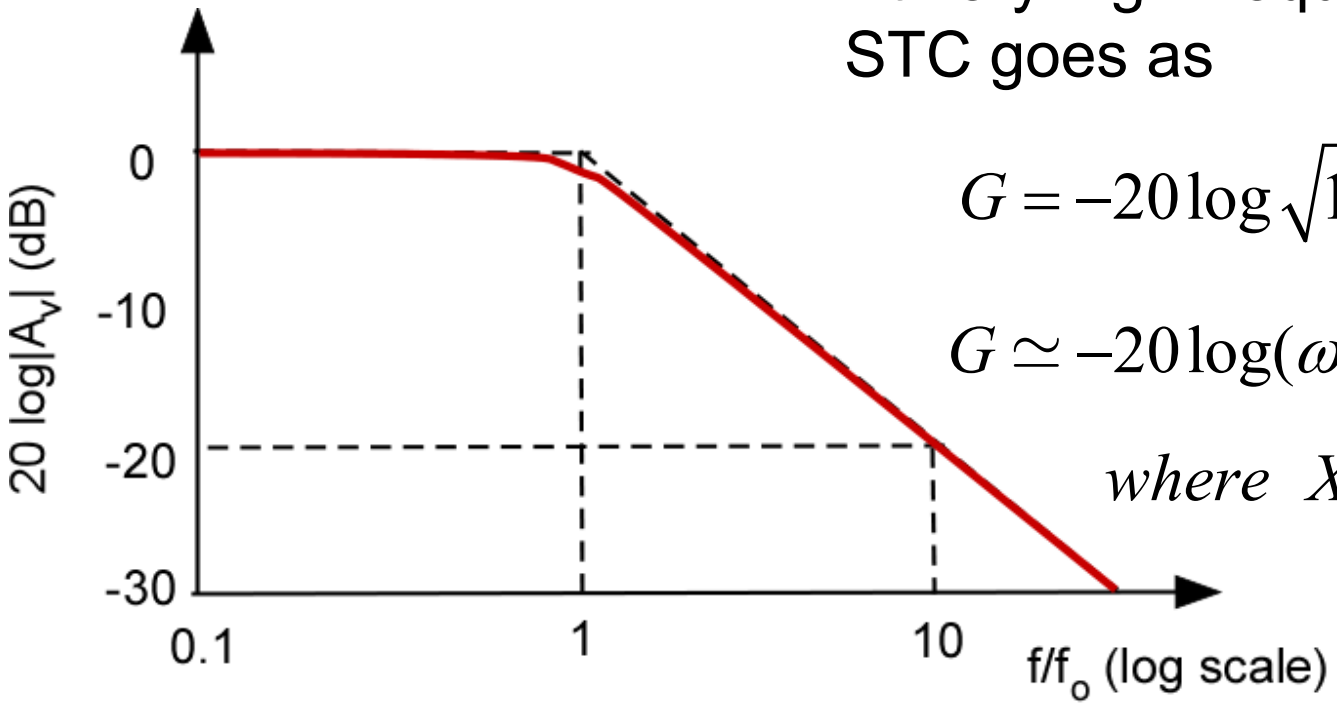
$$A_v = \frac{1}{1 + j\omega RC} = \frac{1}{1 + jf / f_2}$$

Low-Pass Circuit

$$f_o = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau}$$

$$\tau = RC = \text{time constant}$$

At very high frequencies, STC goes as



$$G = -20\log\sqrt{1+(\omega/\omega_o)^2}$$

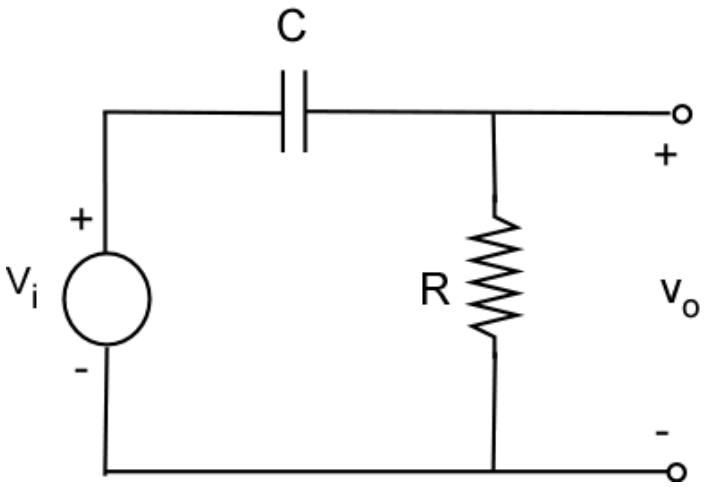
$$G \simeq -20\log(\omega/\omega_o) = -20X$$

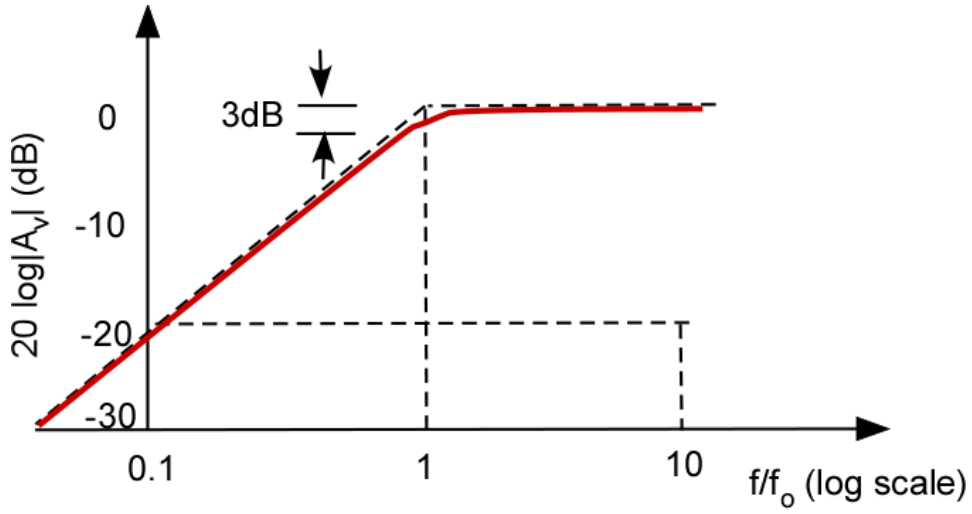
$$where \quad X = \log(\omega/\omega_o)$$

At high frequencies, slope of curve is –20 dB

$$if \quad X = 1\,(\omega = 10\omega_o),\ decrease\ is -20\ dB \Rightarrow -20dB/decade$$

High-Pass Circuit

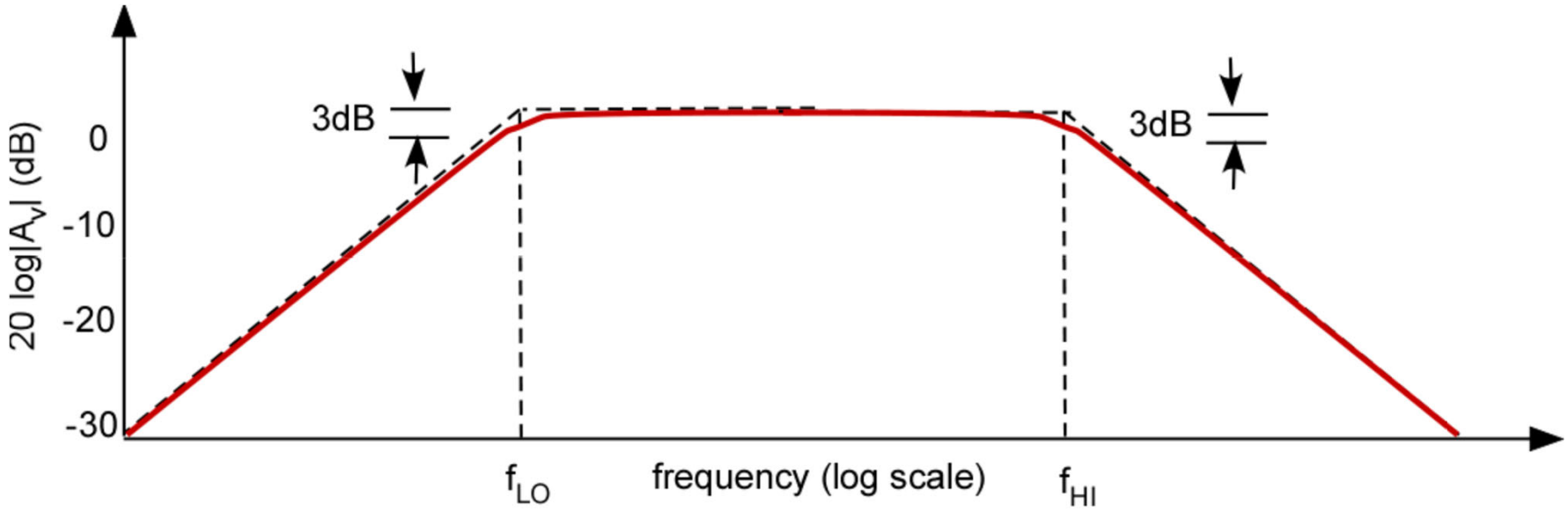




$$V_o = \frac{V_i R}{R + \frac{1}{j\omega C}} = \frac{V_i}{1 + \frac{1}{j\omega RC}}$$

$$A_v = \frac{V_o}{V_i} = \frac{1}{1 - j\frac{1}{2\pi fRC}} = \frac{1}{1 - jf_o / f}$$

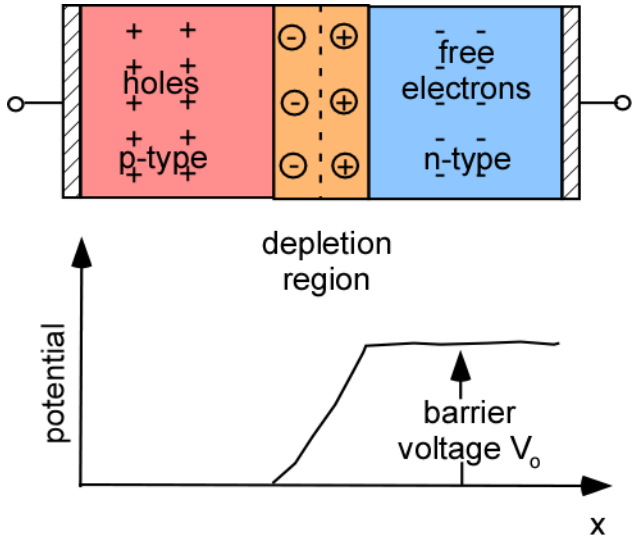
Octave & Decade



Overall gain $A(f)$ is

$$A(f) = A_o \cdot \frac{jf / f_{lo}}{1 + jf / f_{lo}} \cdot \frac{1}{1 + jf / f_{hi}}$$

PN Junction

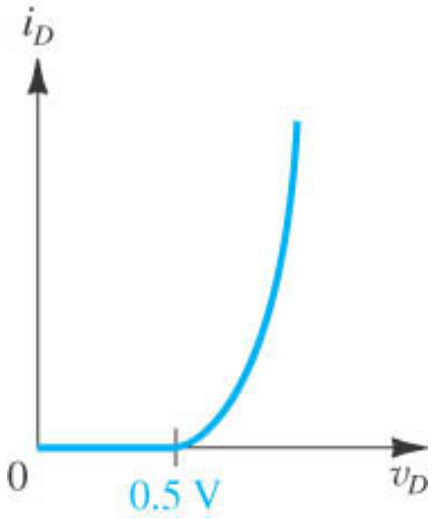


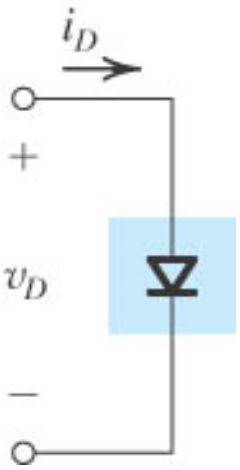
- **When a p material is connected to an n-type material, a junction is formed**
  - Holes from p-type diffuse to n-type region
  - Electrons from n-type diffuse to p-type region
  - Through these diffusion processes, recombination takes place
  - Some holes disappear from p-type
  - Some electrons disappear from n-type

A depletion region consisting of bound charges is thus formed
Charges on both sides cause electric field ➔ potential = V_o

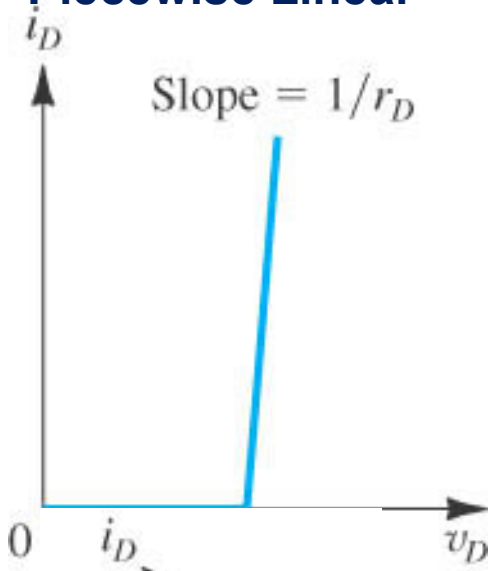
Diode Models

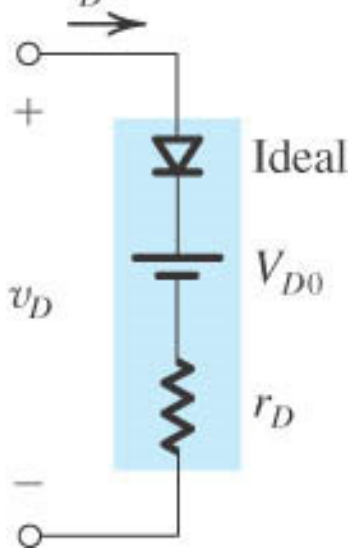
Exponential



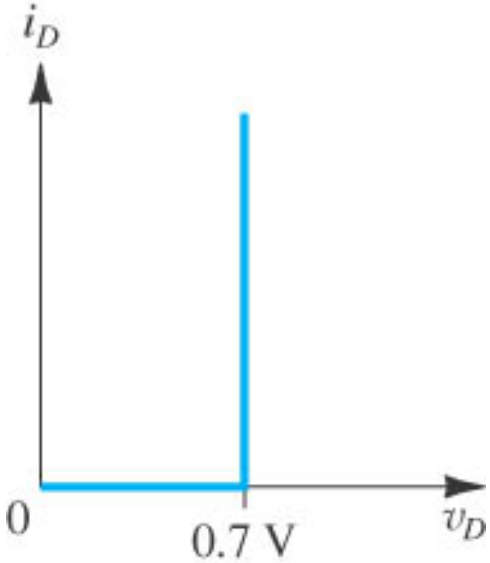


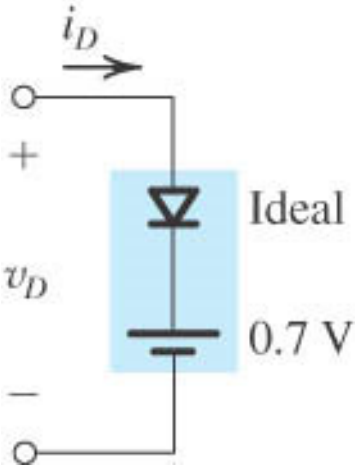
Piecewise Linear





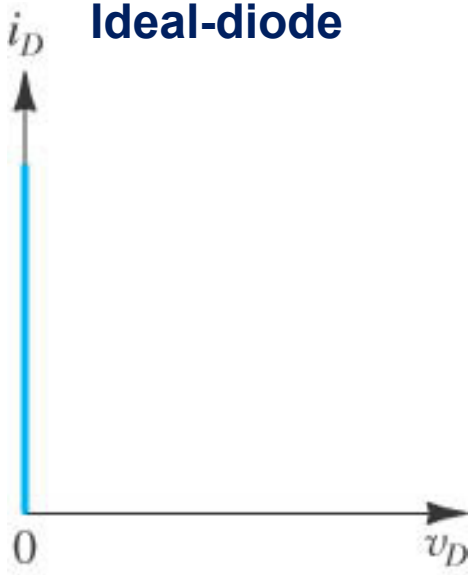
Constant-Voltage-Drop



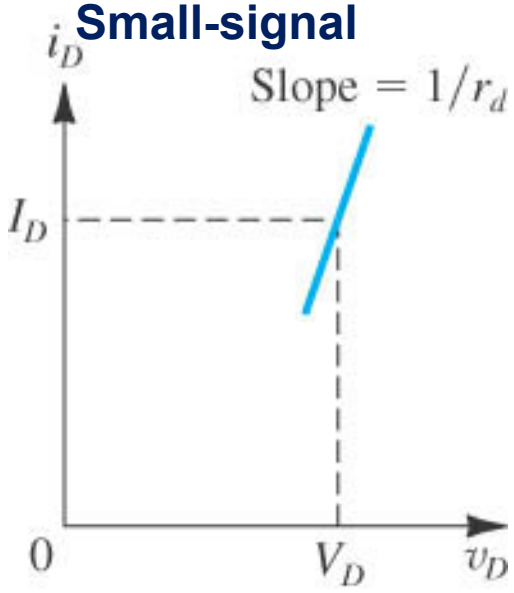


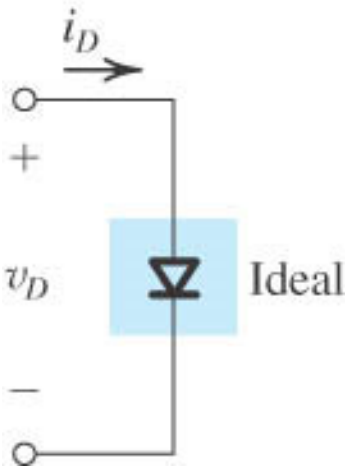
Diode Models

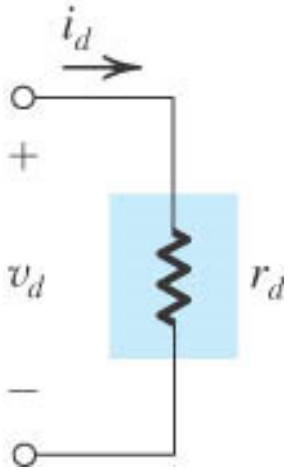
Ideal-diode



Small-signal

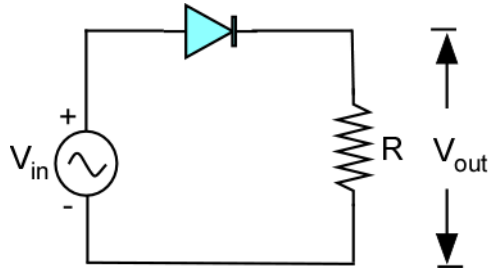


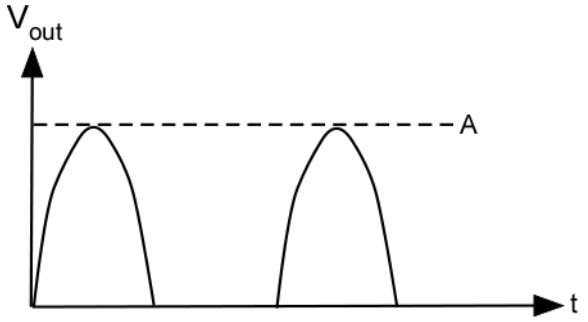


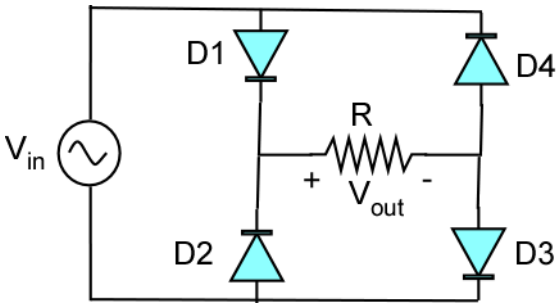


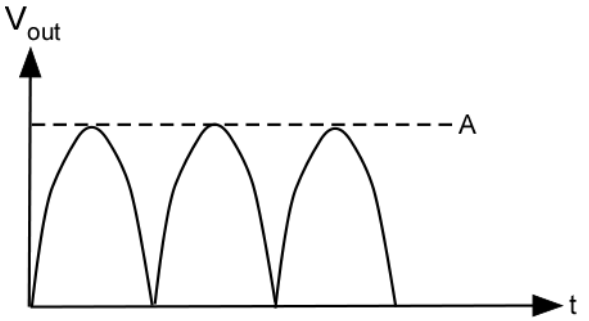
Diode Circuits - Rectification

$$V_{in} = A \sin \omega t$$



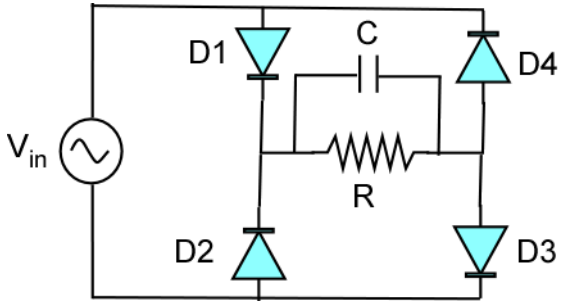


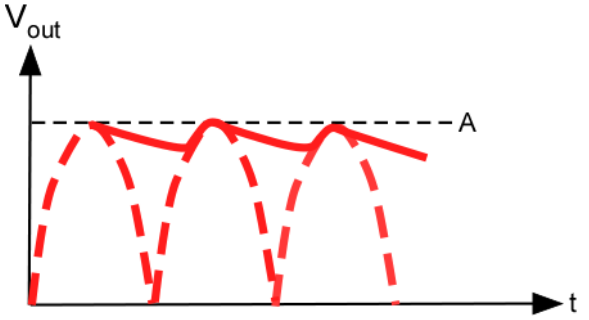




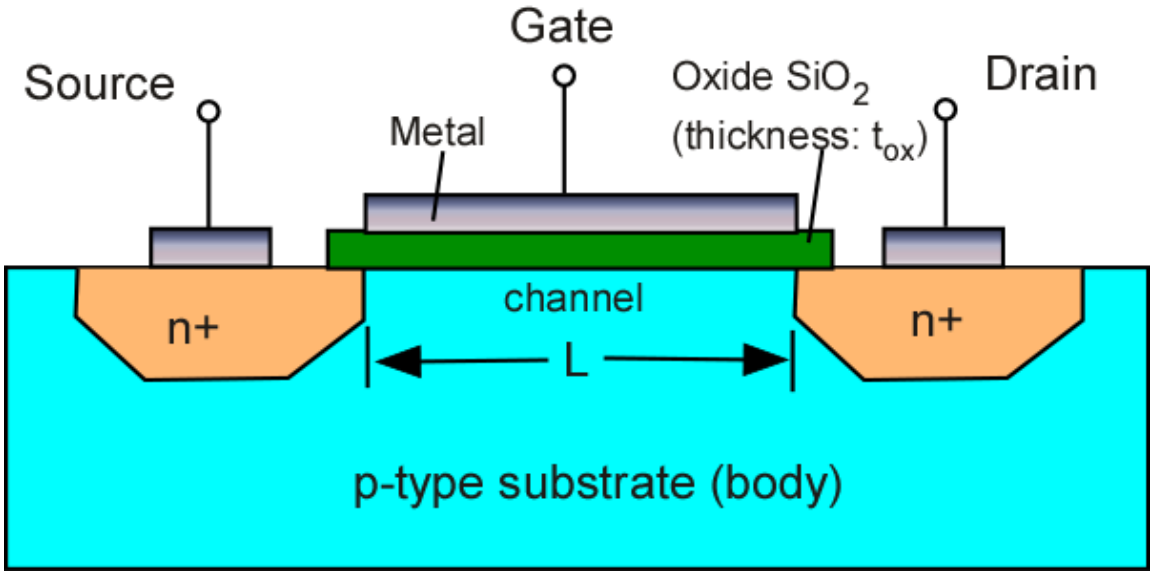
Rectification with ripple reduction.

C must be large enough so that RC time constant is much larger than period



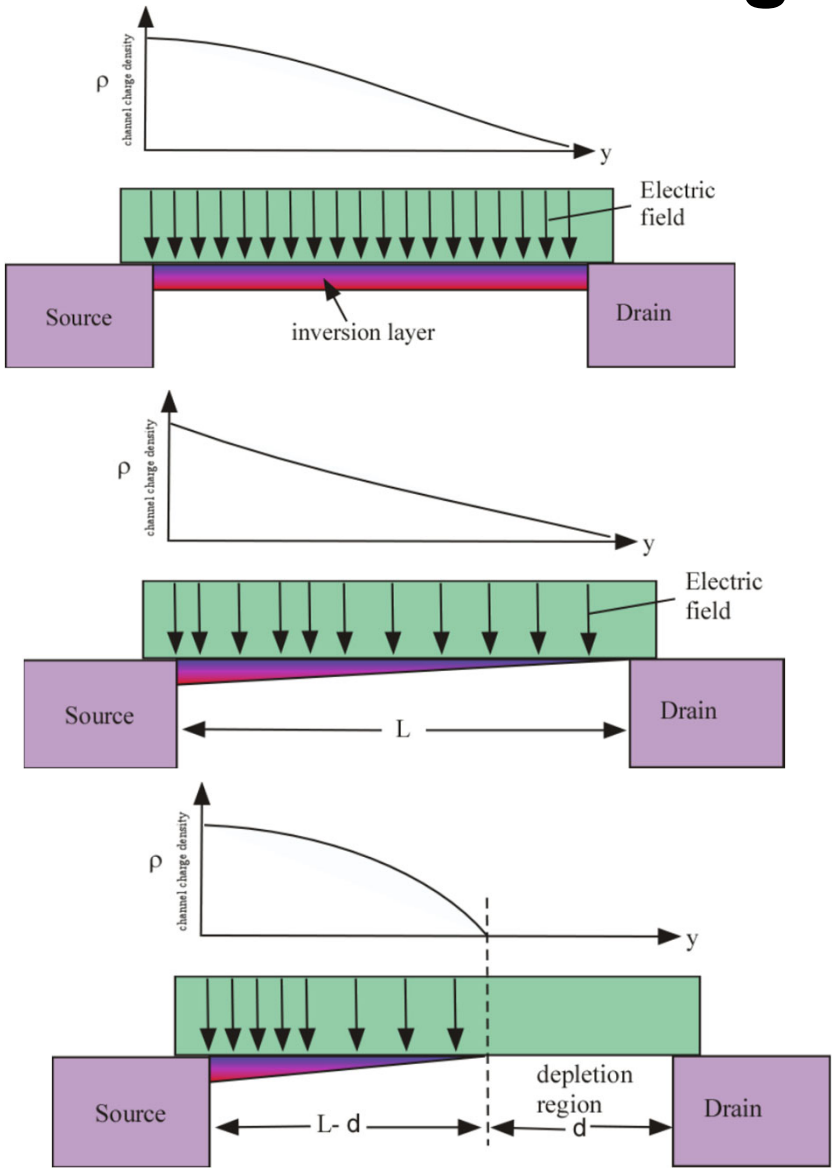


NMOS Transistor



- **NMOS Transistor**
  - N-Channel MOSFET
  - Built on p-type substrate
  - MOS devices are smaller than BJTs
  - MOS devices consume less power than BJTs

MOS Regions of Operation



Triode

Resistive

$$V_{GS} > V_T$$

$$V_{DS} \ small$$

Nonlinear

$$V_{GS} > V_T$$

$$V_{DS} < (V_{GS} - V_T)$$

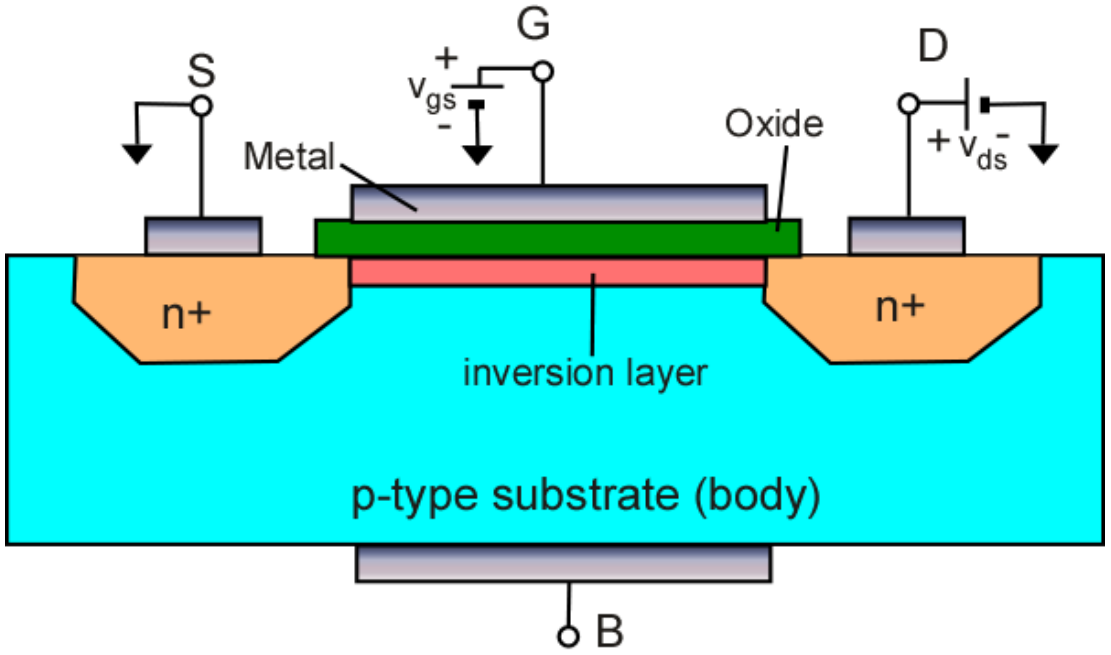
Active

Saturation

$$V_{GS} > V_T$$

$$V_{DS} \geq V_{GS} - V_T$$

MOS – Triode Region - 1



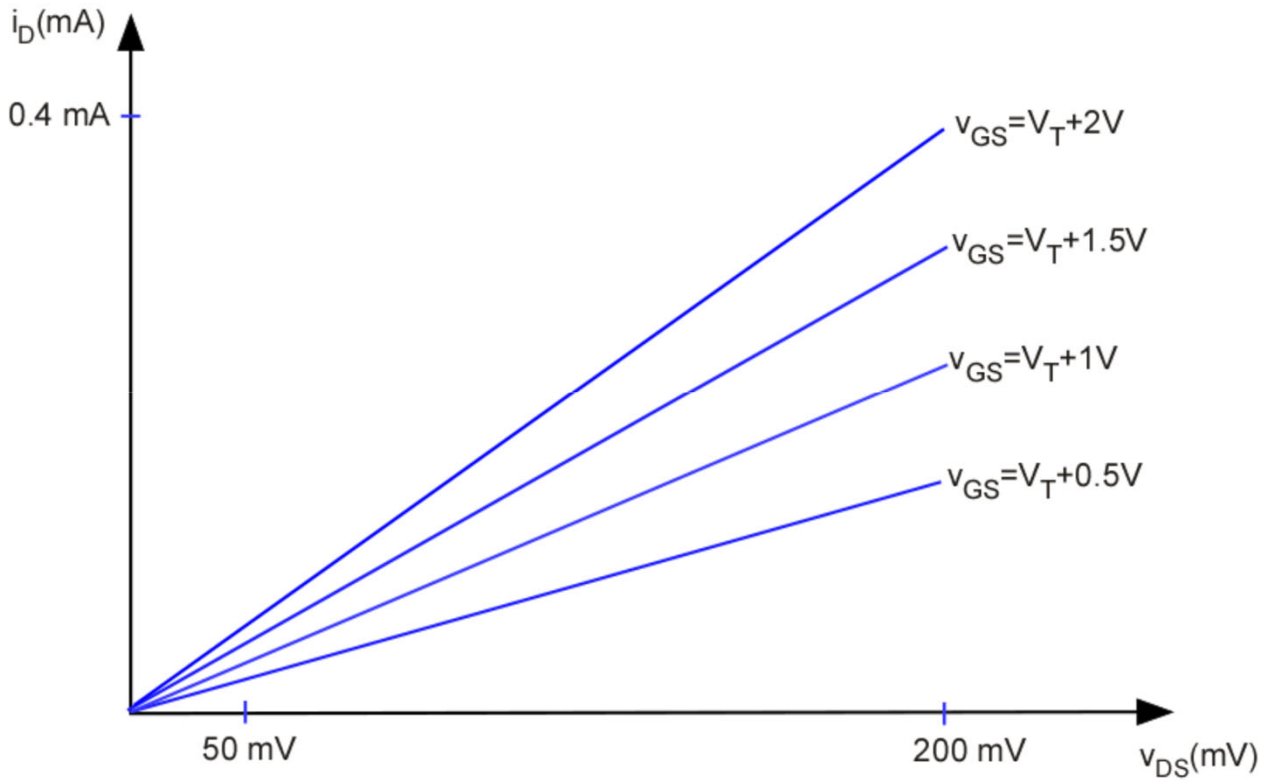
$$I_D = \mu \frac{W}{L} C_{ox} \left[\left(V_{GS} - V_T \right) V_{DS} \right]$$

$$V_{DS} << \left(V_{GS} - V_T \right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\varepsilon_o}{t_{ox}}$$

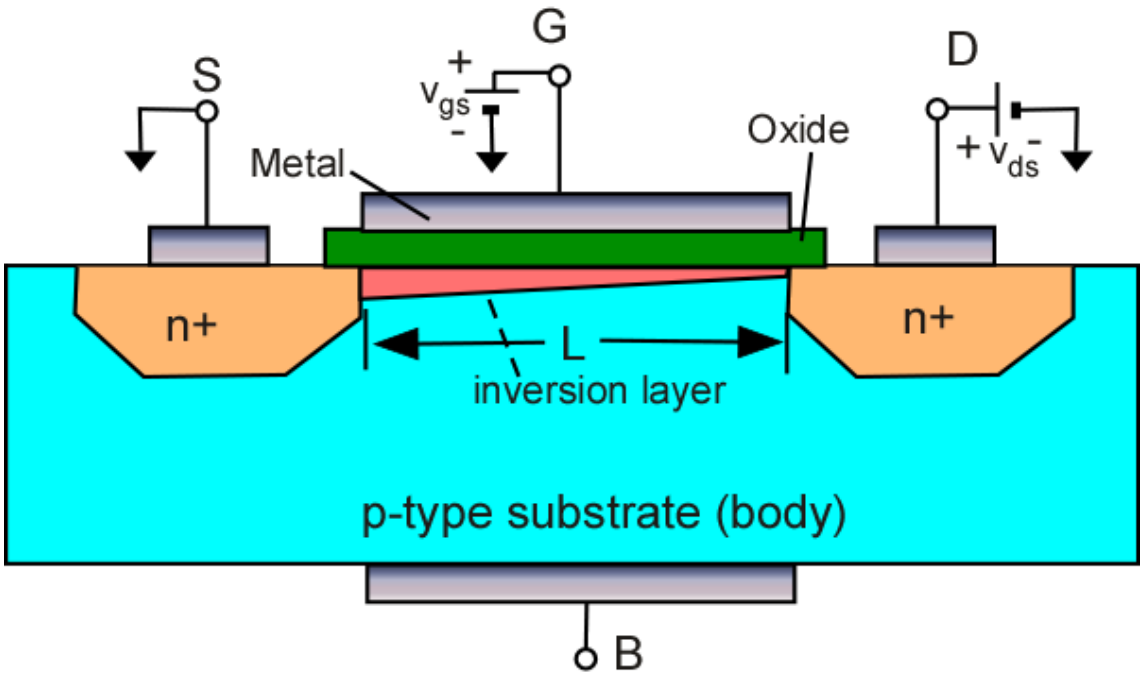
C_{ox}: gate oxide capacitance
μ: electron mobility
L: channel length
W: channel width
V_T: threshold voltage

MOS – Triode Region



FET is like a linear resistor with $r_{ds} = \dfrac{1}{\mu_n C_{ox} \dfrac{W}{L}\left(V_{GS} - V_T\right)}$

MOS – Triode Region - 2



$$V_{GS} > V_T$$

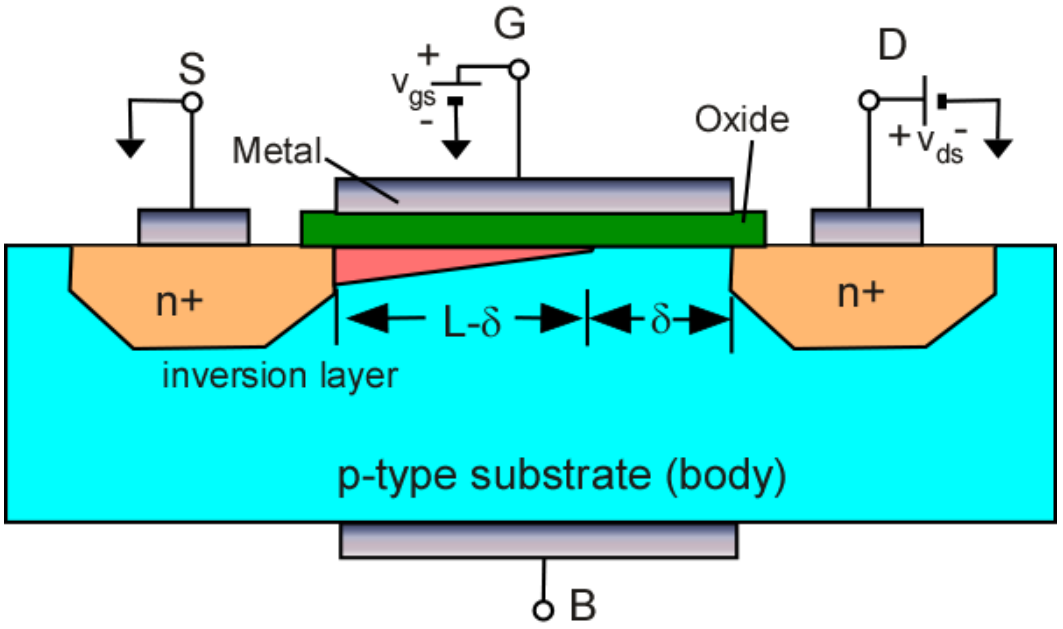
$$V_{DS} < (V_{GS} - V_T)$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

- Charge distribution is nonuniform across channel
- Less charge induced in proximity of drain

MOS – Active (Saturation) Region

Saturation occurs at pinch off when $V_{DS} = (V_{GS} - V_T) = V_{DSP}$



$V_{GS} > V_T$

$V_{DS} > (V_{GS} - V_T)$
(saturation)

$$I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2$$

Body Effect

- **The body effect**
  - V_T varies with bias between source and body
  - Leads to modulation of V_T

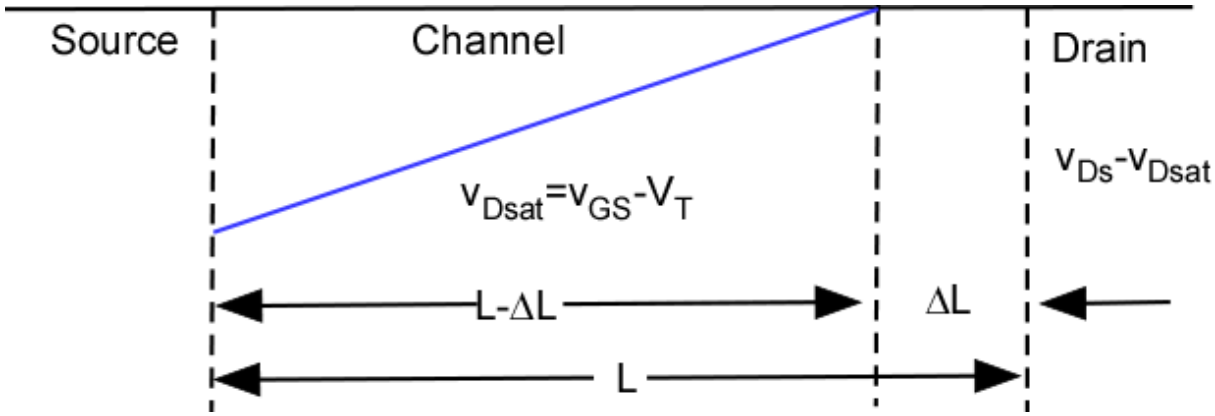
Potential on substrate affects threshold voltage

$$V_T(V_{SB}) = V_{To} + \gamma\left[\left(2|\phi_F| + V_{SB}\right)^{1/2} - \left(2|\phi_F|\right)^{1/2}\right]$$

$$|\phi_F| = \left(\frac{kT}{q}\right)\ln\left(\frac{N_a}{n_i}\right)$$ Fermi potential of material

$$\gamma = \frac{\left(2qN_a\varepsilon_s\right)^{1/2}}{C_{ox}}$$ Body bias coefficient

Channel-Length Modulation



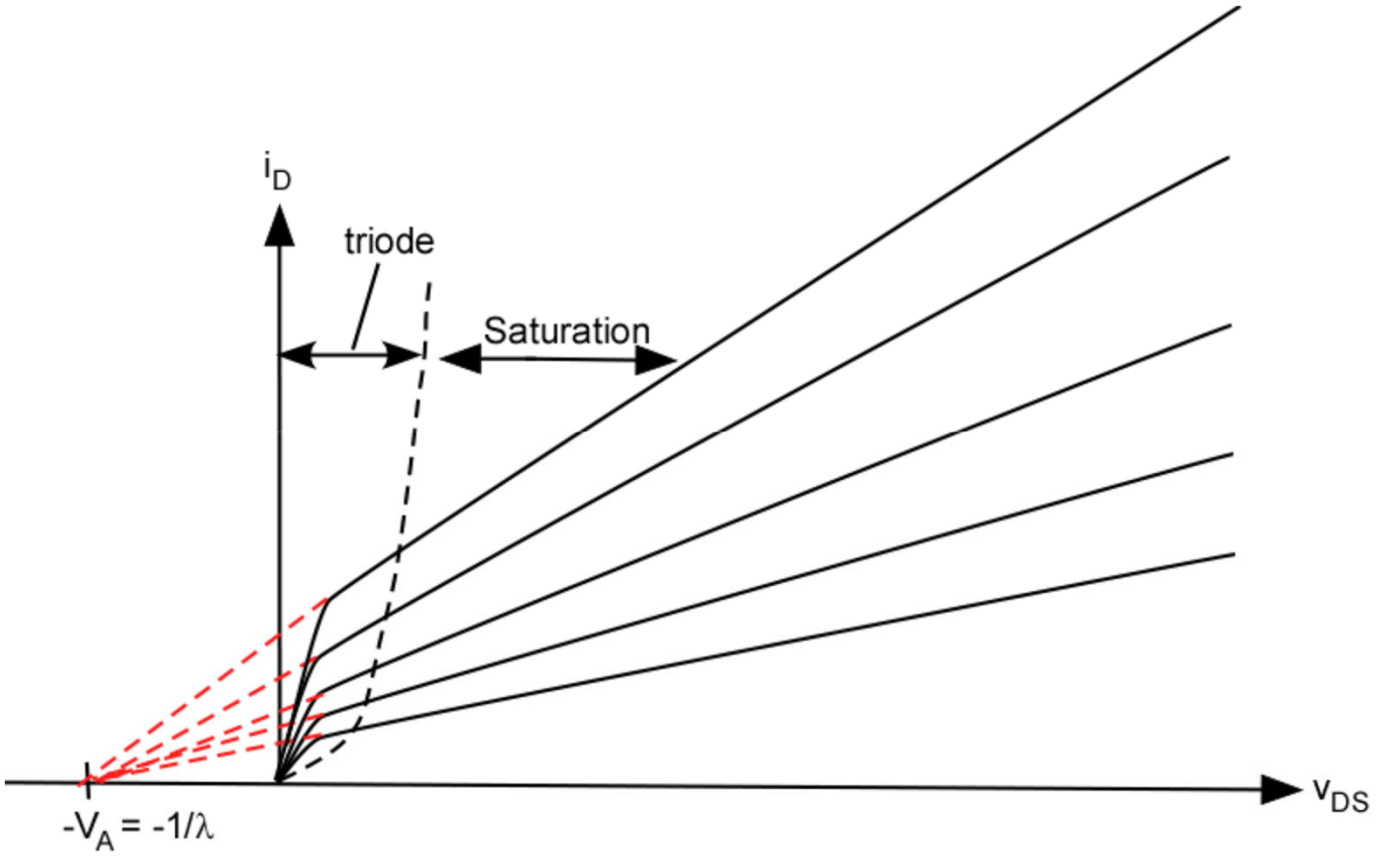
With depletion layer widening, the channel length is in effect reduced from *L* to *L-ΔL* ➔ Channel-length modulation

This leads to the following I-V relationship

$$i_D = \frac{1}{2} k_n' \frac{W}{L} \left(v_{GS} - V_T \right)^2 \left(1 + \lambda v_{DS} \right)$$

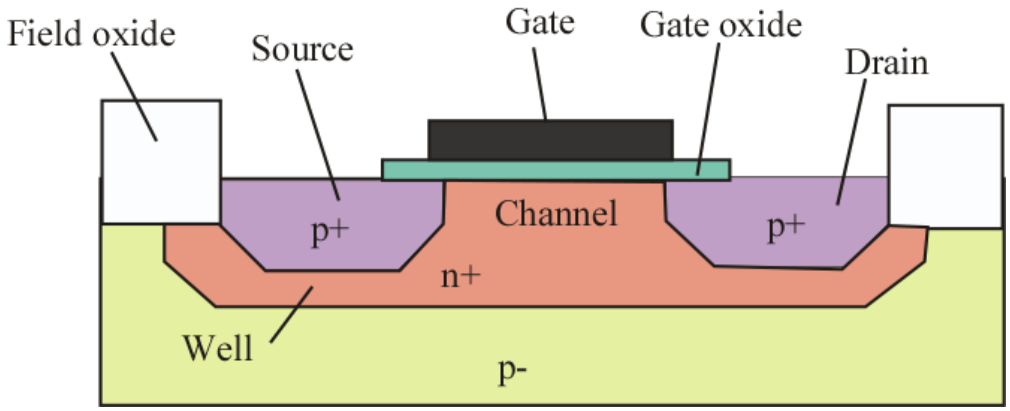
Where λ is a process technology parameter

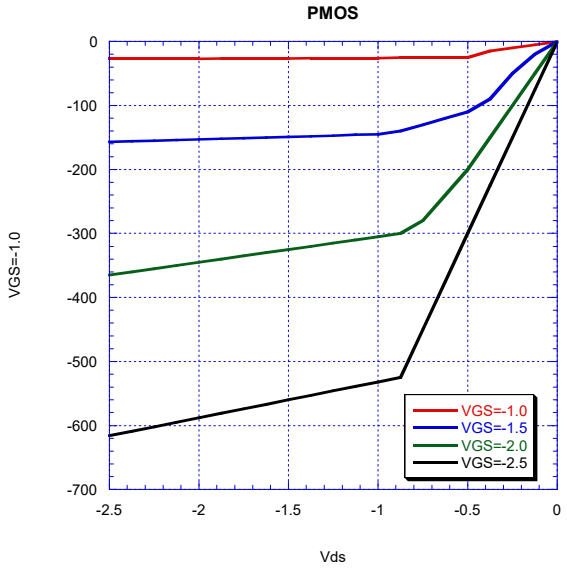
Channel-Length Modulation



Channel-length modulation causes i_D to increase with v_{DS} in saturation region

PMOS Transistor

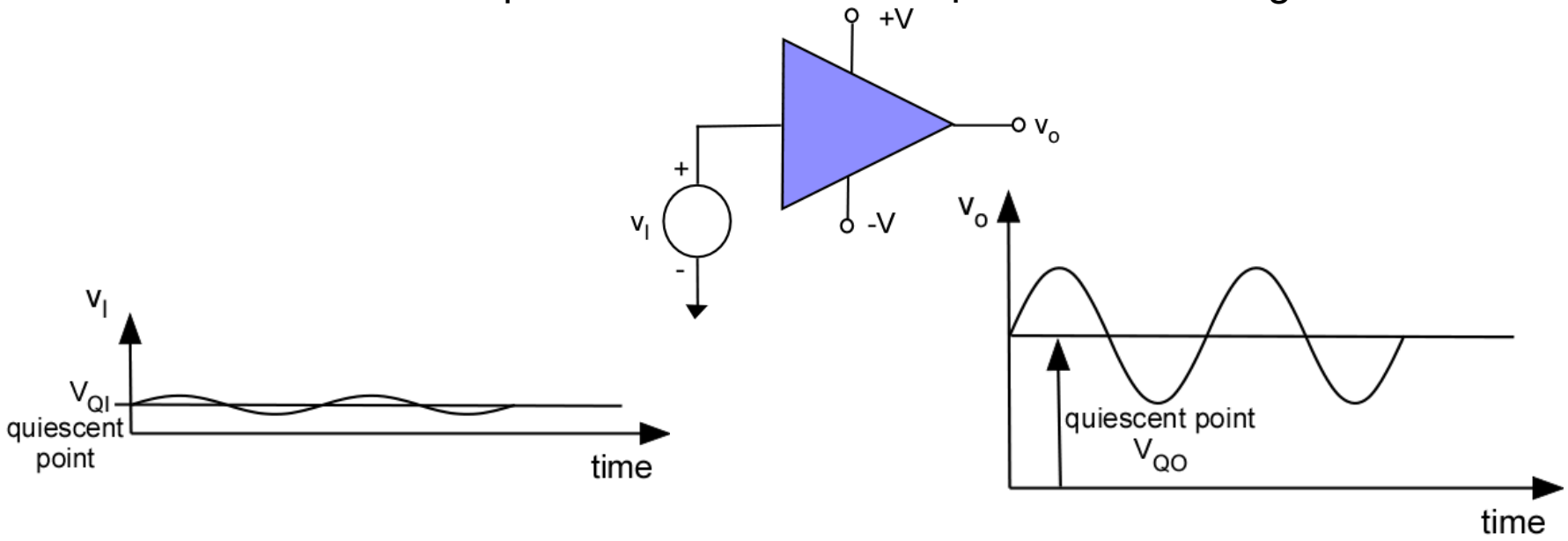




- All polarities are reversed from nMOS
- v_{GS}, v_{DS} and V_t are negative
- Current i_D enters source and leaves through drain
- Hole mobility is lower $\Rightarrow$ low transconductance
- nMOS favored over pMOS

Biasing of Amp

Bias will provide quiescent points for input and output about which variations will take place. Bias maintain amplifier in active region.



$$V_I(t) = V_{QI} + v_I(t)$$

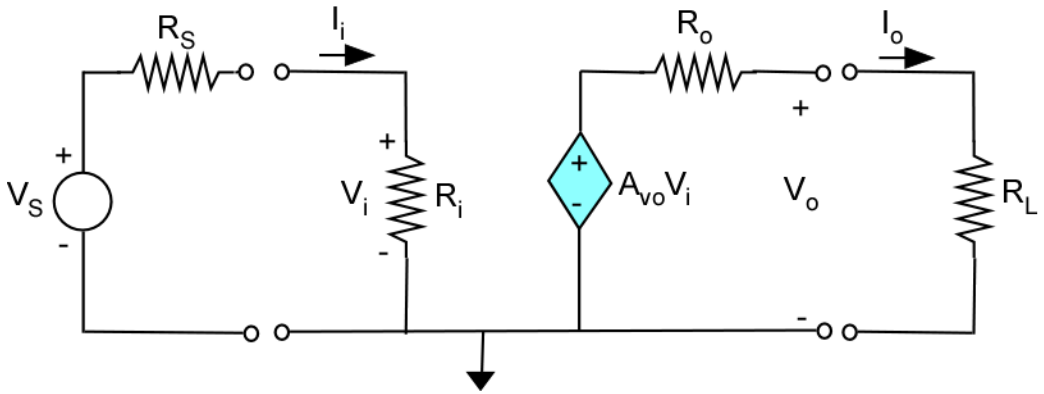
$$V_o(t) = V_{QO} + v_o(t)$$

$$v_o(t) = A_v v_I(t)$$

$$A_v = \left.\frac{dv_o}{dv_I}\right|_{at\ Q}$$

Amplifier characteristics are determined by bias point

Voltage Amplifier



$$Voltage\ gain\ is: \frac{v_o}{v_i} = A_v = \frac{A_{vo}R_L}{R_L + R_o}$$

$$Input\ v_i = v_s \frac{R_i}{R_i + R_S}$$

$$v_o = \frac{A_{vo}v_i R_L}{R_L + R_o}$$

Want R_i large (so $v_i \approx v_s$) (actually want $R_i >> R_s$) ideal $R_i = \infty$

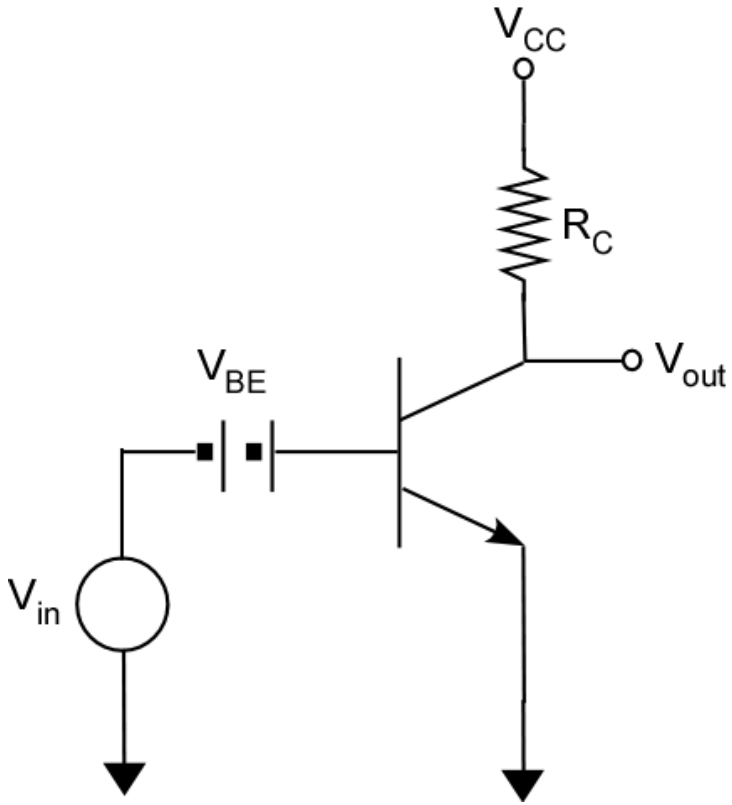
Want R_o small (as small as possible) to achieve maximum gain ➔ ideal $R_o = 0$

$$Overall\ gain: \frac{v_o}{v_s} = A_{vo} \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o}$$

Small-Signal Model

- **What is a small-signal incremental model?**
  - Equivalent circuit that only accounts for signal level fluctuations about the DC bias operating points
  - Fluctuations are assumed to be small enough so as not to drive the devices out of the proper range of operation
  - Assumed to be linear
  - Derives from superposition principle

Common Emitter Configuration



The emitter current I_E can be approximated as:

$$I_E \simeq I_S e^{V_{BE}/V_T}$$

An incremental conductance g_e can be defined as

$$g_e \equiv \frac{\partial I_E}{\partial V_{BE}} = \frac{I_S}{V_T} e^{V_{BE}/V_T} = \frac{I_E}{V_T}$$

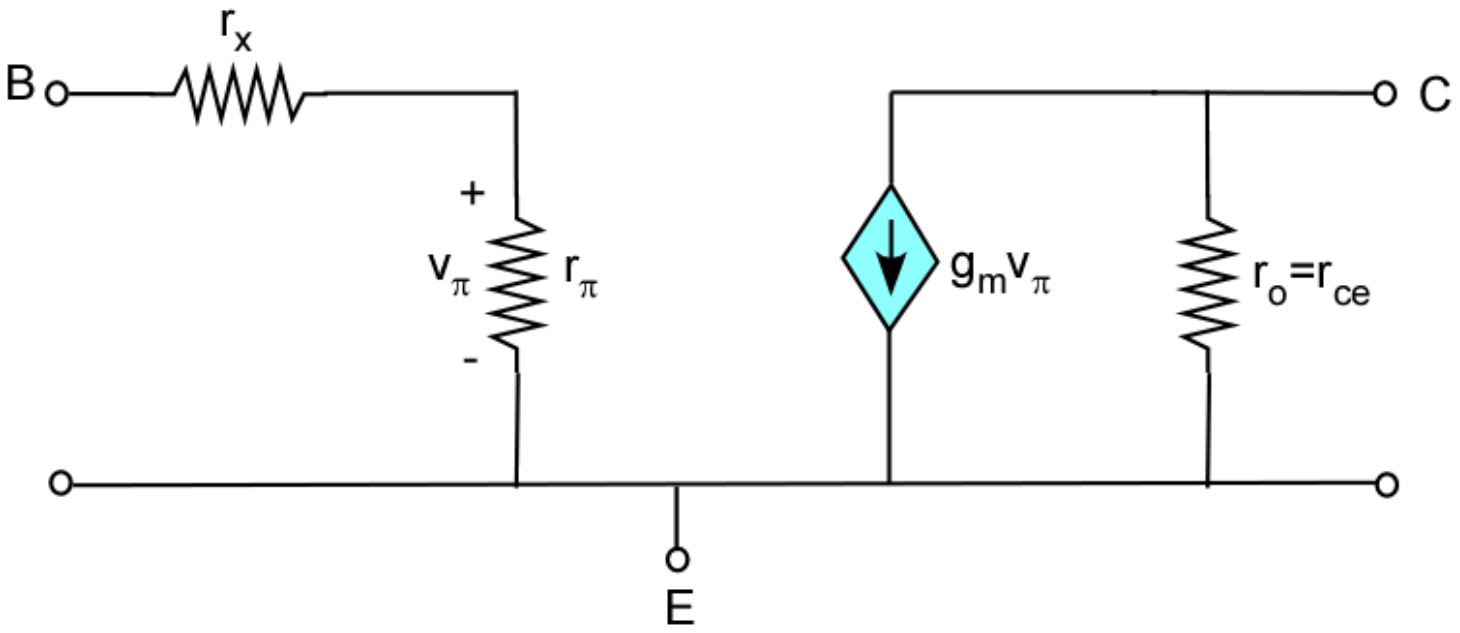
From which we get:

$$r_e = \frac{1}{g_e} = \frac{V_T}{I_E}$$

Emitter resistance

$$\text{Usually, } V_T = 26\,mV \Rightarrow r_e = \frac{26\,mV}{I_E}$$

Hybrid-π Incremental Model for BJTs



r_π: input resistance looking into the base
r_x: parasitic series resistance looking into base – ohmic base resistance
g_m: BJT transconductance
r_o=r_{ce}: output collector resistance related to the Early effect

Hybrid-π Parameters

$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{I_C = cons\tan t} = \frac{I_C}{V_T}$$

$$r_\pi \text{ is defined as: } r_\pi = \frac{v_\pi}{i_b}$$

$$\text{Since } i_b = \frac{g_m v_\pi}{\beta} \text{ then } r_\pi = \frac{\beta}{g_m}$$

Can show that

$$r_\pi = (\beta + 1) r_e$$

$$g_m = \frac{\alpha}{r_e}$$

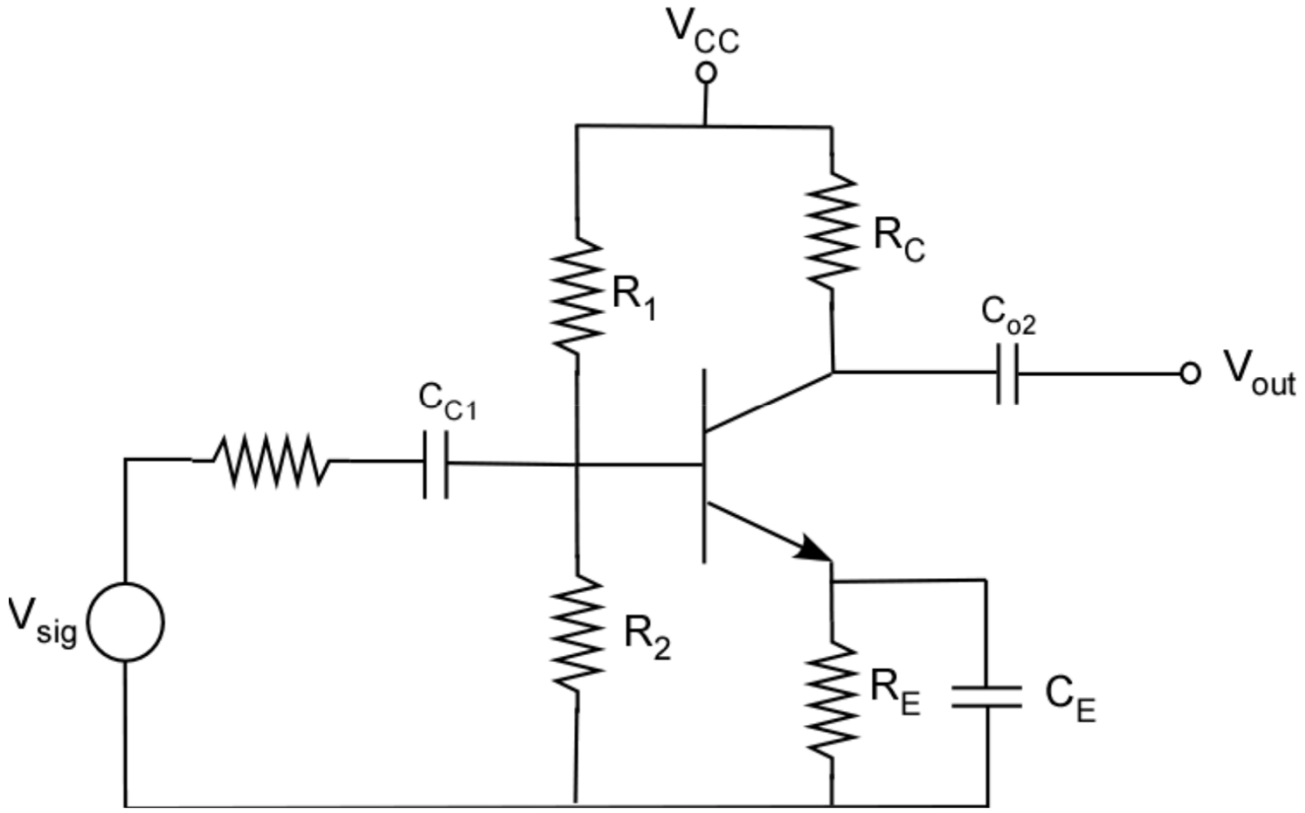
$$\beta = g_m r_\pi$$

$r_{ce} = r_o$ is associated with the Early effect

$$r_{ce} = r_o = \frac{|V_A|}{I_C} = \frac{|V_A|}{\beta I_B}$$

$$g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

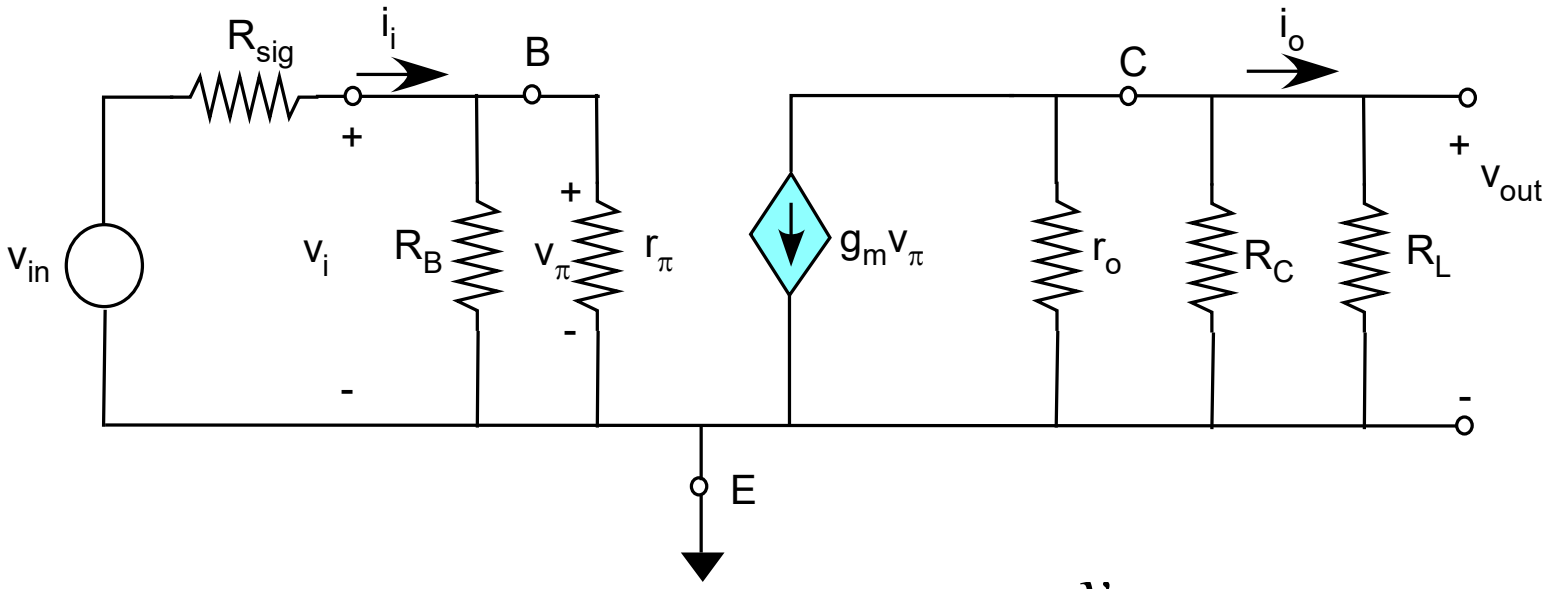
Common Emitter (CE) Amplifier



Bias: Choose R_1 & R_2 to set $V_B \rightarrow V_E$ is then set. Choose R_E to set $I_E \sim I_C$.
Quiescent point of V_{out} will be determined by R_C. Emitter is an AC short.

Incremental Model for CE Amplifier

Hybrid-π model (ignoring r_x)



$$R_B = R_1 \,||\, R_2$$

$$R_{in} = \frac{v_i}{i_i} = R_B \,||\, r_\pi$$

$$\textit{Sometimes } R_B \gg r_\pi \textit{ and } R_{in} \simeq r_\pi$$

CE Amplifier

Output Impedance

$$R_{out} = R_C \,||\, r_o$$

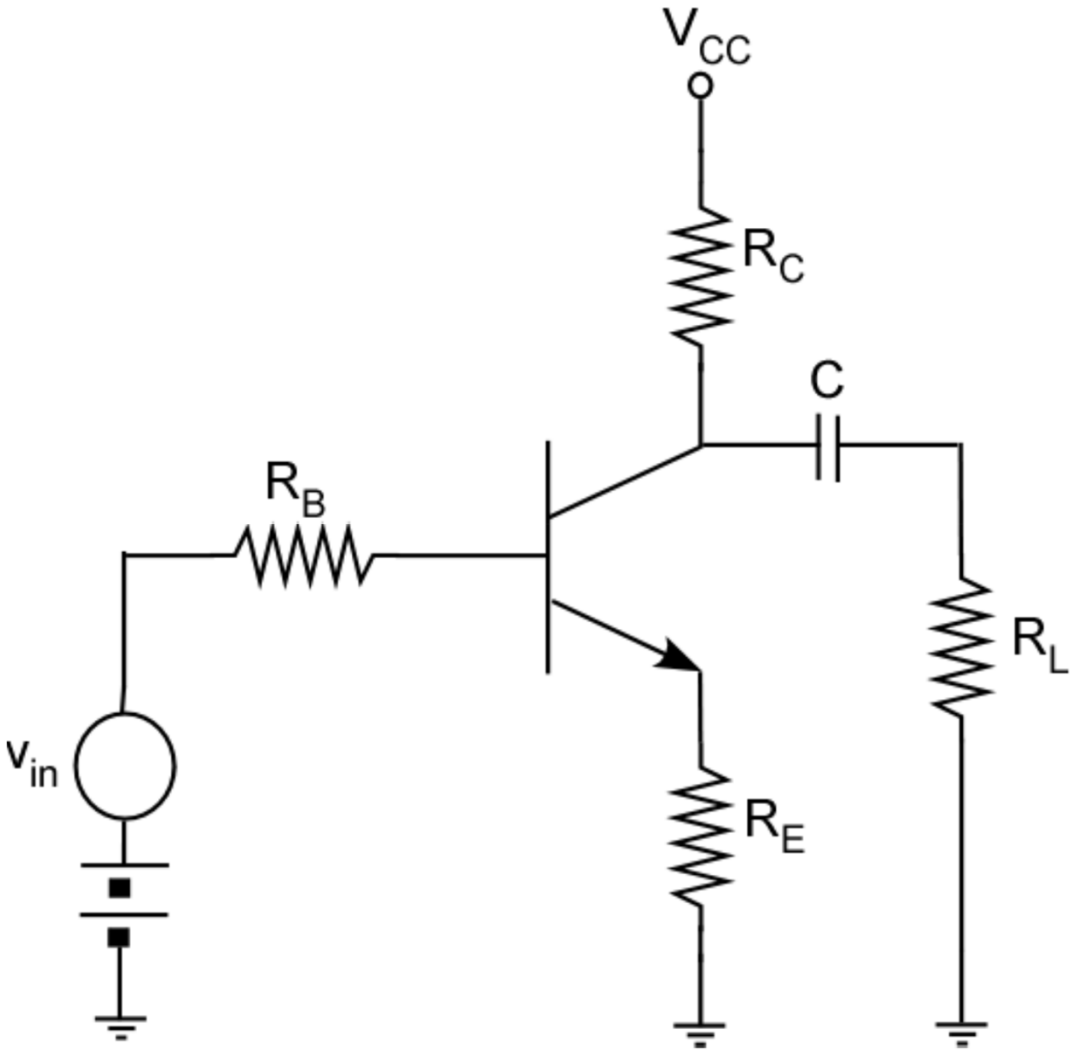
$$If\ r_o \gg R_C,\ R_{out} \simeq R_C$$

$$from\ which\ A_v = A_{vo}\left(\frac{R_L}{R_L + R_o}\right)$$

It can be seen that if R_{sig} >> r_π, the gain will be highly dependent on β. This is not good because of β variations

$$If\ R_{sig} \ll r_\pi,\quad G_v \simeq -g_m\left(R_C \,||\, R_L \,||\, r_o\right)$$

CE with External Resistors



CE with External Resistors

$$\frac{v_{out}}{v_{in}} = -\frac{g_m r_\pi \left(R_L \| R_C\right)}{g_m r_\pi R_E + R_E + r_\pi + R_B} = -\frac{g_m r_\pi \left(R_L \| R_C\right)}{R_E\left(\beta+1\right) + r_\pi + R_B}$$

$$A_{MB} = -g_m\left(R_L \| R_C\right)\frac{1}{\frac{R_E\left(\beta+1\right)}{r_\pi} + \frac{R_B}{r_\pi} + 1}$$

$$A_{MB} = -\frac{\beta\left(R_L \| R_C\right)}{R_E\left(\beta+1\right) + r_\pi + R_B}$$

R_E and R_B degrade the gain

CE with External Resistors

The gain can be written as:

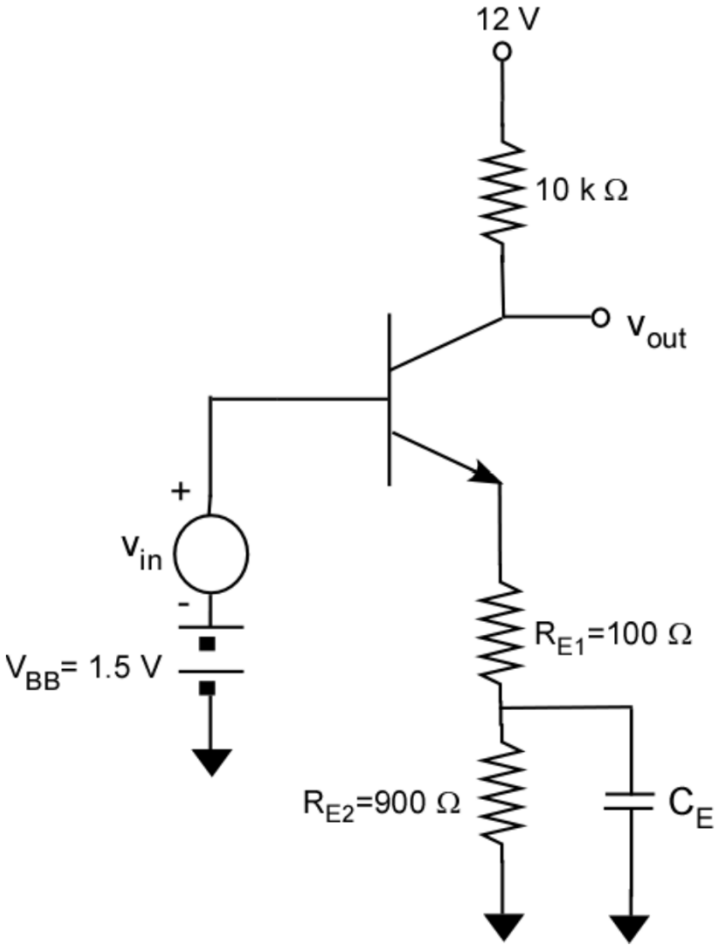
$$A_{MB} = -\frac{\beta\left(R_L \parallel R_C\right)}{R_E\left(\beta+1\right)+r_\pi+R_B} = -\frac{\left(\frac{\beta}{\beta+1}\right)\left(R_L \parallel R_C\right)}{R_E+\frac{r_\pi}{\left(\beta+1\right)}+\frac{R_B}{\left(\beta+1\right)}}$$

and since $\frac{\beta}{\left(\beta+1\right)}=\alpha$ neglecting $\frac{R_B}{\left(\beta+1\right)}$

$$A_{MB} = -\frac{\alpha\left(R_L \parallel R_C\right)}{R_E+r_e}$$

Example

Given V_{BEON}=0.6V, find the gain for the circuit shown



$$V_{BQ} = 1.5\,V$$

$$V_{EQ} = 1.5\,V - 0.6\,V = 0.9\,V$$

$$I_E \simeq \frac{0.9}{R_{E1} + R_{E2}} = \frac{0.9}{1\,k\Omega} = 0.9\,mA$$

Example (Cont')

$$I_C \simeq 0.9\,mA \Rightarrow V_{outQ} = 12\,V - 0.9 \times 10 = 3\,V$$

AC analysis: R_{E2} is shorted and R_E=R_{E1}=100Ω. Since β is not known, use:

$$A_{MB} = -\frac{\alpha R_C}{R_E + r_e} \quad with \quad \alpha \simeq 1$$

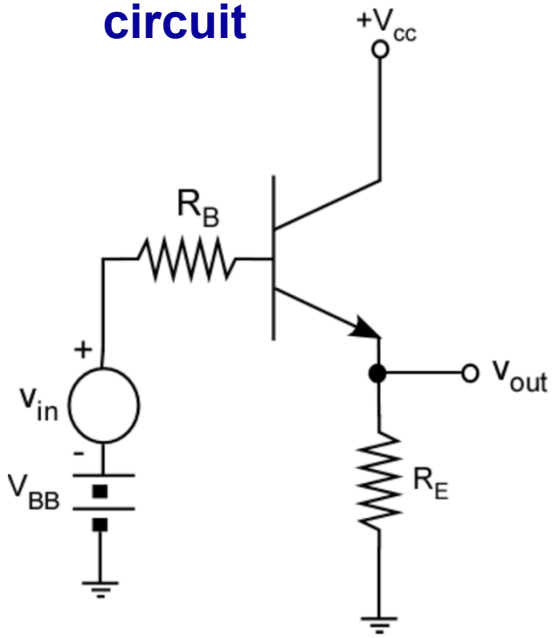
$$r_e = \frac{V_T}{I_E} = \frac{26}{0.9} = 28.8\,\Omega$$

$$A_{MB} = -\frac{10{,}000}{100 + 28.8} = -77.5$$

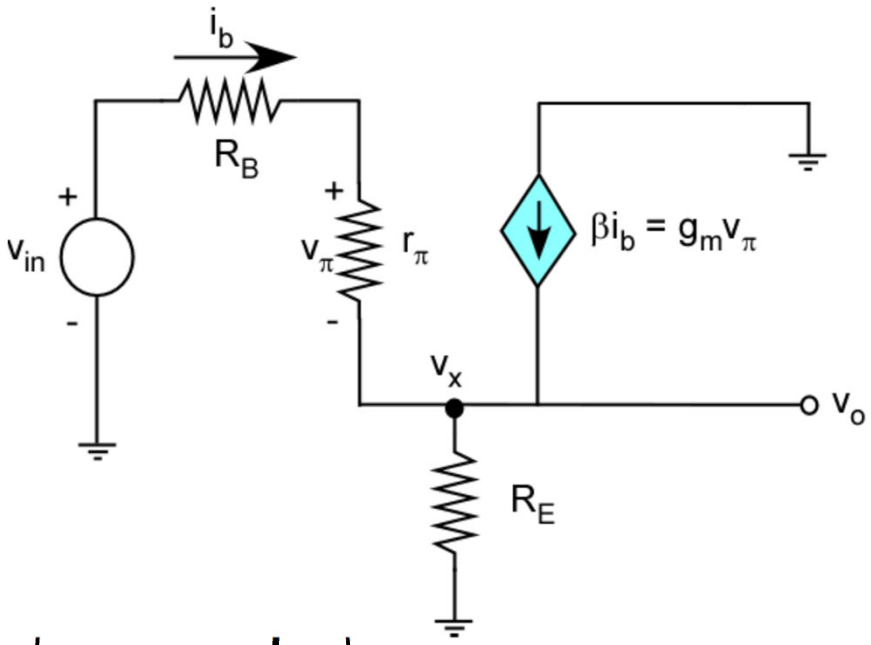
$$A_{MB} = -77.5$$

Emitter Follower

circuit



Incremental model



$$v_o = \left(g_m v_\pi + \frac{v_\pi}{r_\pi} \right) R_E = v_\pi \left(g_m + \frac{1}{r_\pi} \right) R_E$$

$$v_{in} = v_\pi + R_B i_b + v_o = v_\pi + v_\pi R_E \left(g_m + \frac{1}{r_\pi} \right) + \frac{v_\pi}{r_\pi} R_B$$

Emitter Follower

$$v_{in} = v_\pi \left[1 + \frac{R_B}{r_\pi} + R_E \left(g_m + \frac{1}{r_\pi} \right) \right]$$

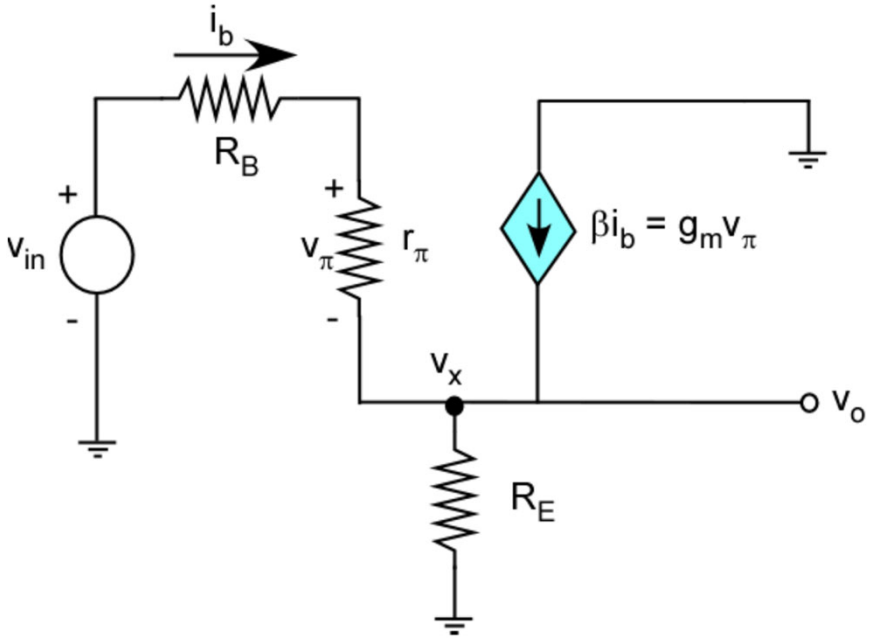
$$\frac{v_o}{v_{in}} = \frac{\left(g_m + \frac{1}{r_\pi} \right) R_E}{\left(g_m + \frac{1}{r_\pi} \right) R_E + 1 + \frac{R_B}{r_\pi}} = \frac{\left(g_m r_\pi + 1 \right) R_E}{\left(g_m r_\pi + 1 \right) R_E + r_\pi + R_B}$$

Using $g_m r_\pi = \beta$

$$\frac{v_o}{v_{in}} = \frac{\left(\beta + 1 \right) R_E}{\left(\beta + 1 \right) R_E + r_\pi + R_B} \simeq 1$$

Emitter follower has unity voltage gain

Emitter Follower – Input Impedance

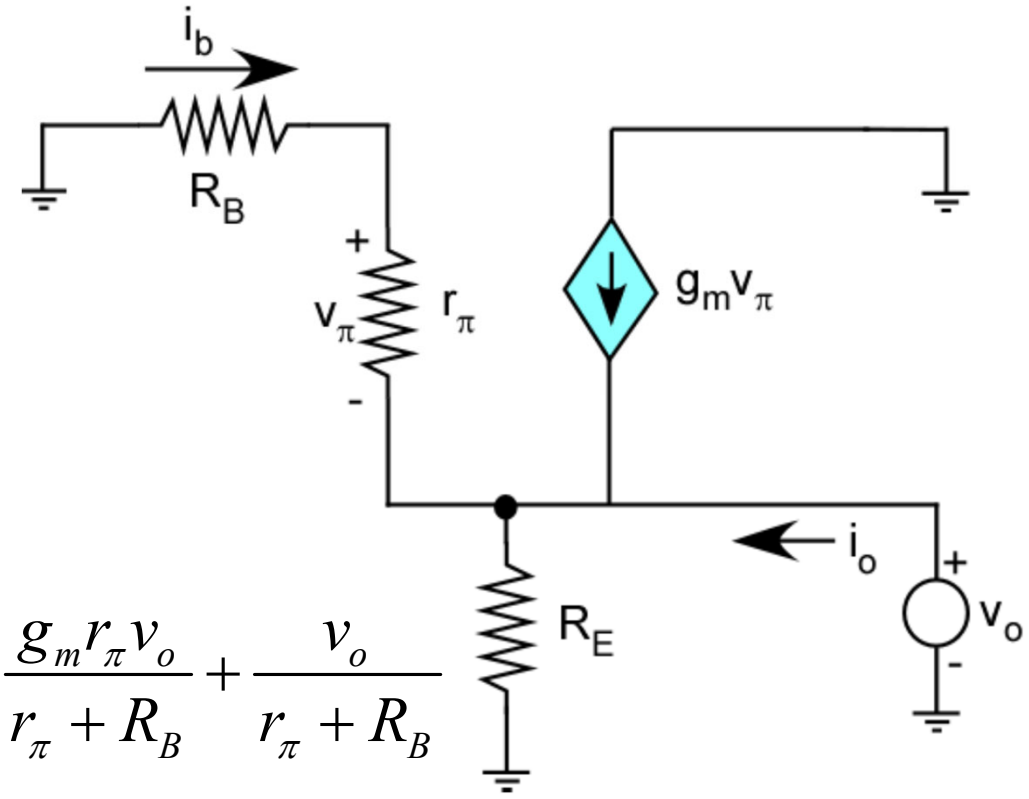


$$r_{in} = \frac{v_{in}}{i_b} = \frac{v_\pi \left[1 + R_B / r_\pi + R_E \left(g_m + 1 / r_\pi \right) \right]}{v_\pi / r_\pi}$$

$$r_{in} = r_\pi + R_B + R_E \left(\beta + 1 \right)$$

Emitter Follower – Output Impedance

$$i_B = -\frac{v_o}{r_\pi + R_B}$$



$$i_o = \frac{v_o}{R_E} - g_m v_\pi + \frac{v_o}{r_\pi + R_B} = \frac{v_o}{R_E} + \frac{g_m r_\pi v_o}{r_\pi + R_B} + \frac{v_o}{r_\pi + R_B}$$

$$i_o = v_o \left[\frac{1}{R_E} + \frac{g_m}{r_\pi + R_B} + \frac{1}{r_\pi + R_B} \right] = v_o \left[r_\pi + R_B + R_E(\beta + 1) \right] \frac{1}{R_E \left(r_\pi + R_B \right)}$$

Output Impedance (cont')

Using $g_m r_\pi = \beta$

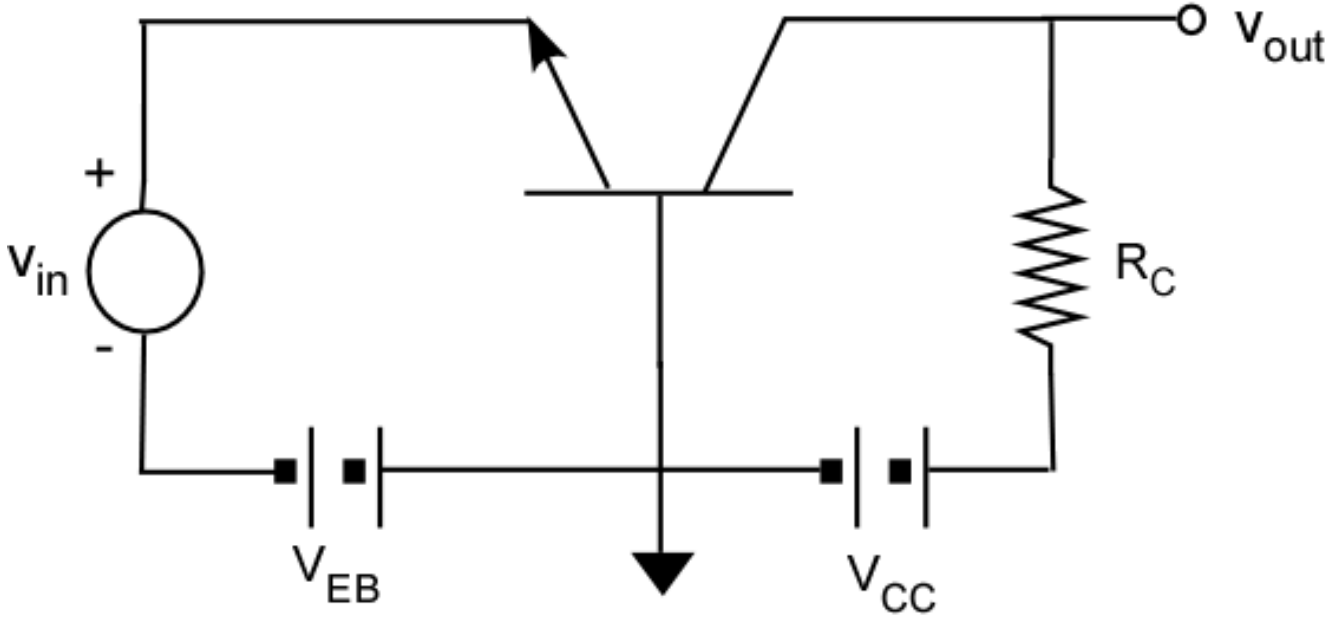
$$\frac{v_o}{i_o} = R_{out} = \frac{R_E\left(r_\pi + R_B\right)}{r_\pi + R_B + R_E(\beta+1)} = \frac{R_E\left(r_\pi + R_B\right)/(\beta+1)}{R_E + \left(r_\pi + R_B\right)/(\beta+1)}$$

$$R_{out} = R_E \,||\, \left(r_\pi + R_B\right)/(\beta+1)$$

If we neglect R_B

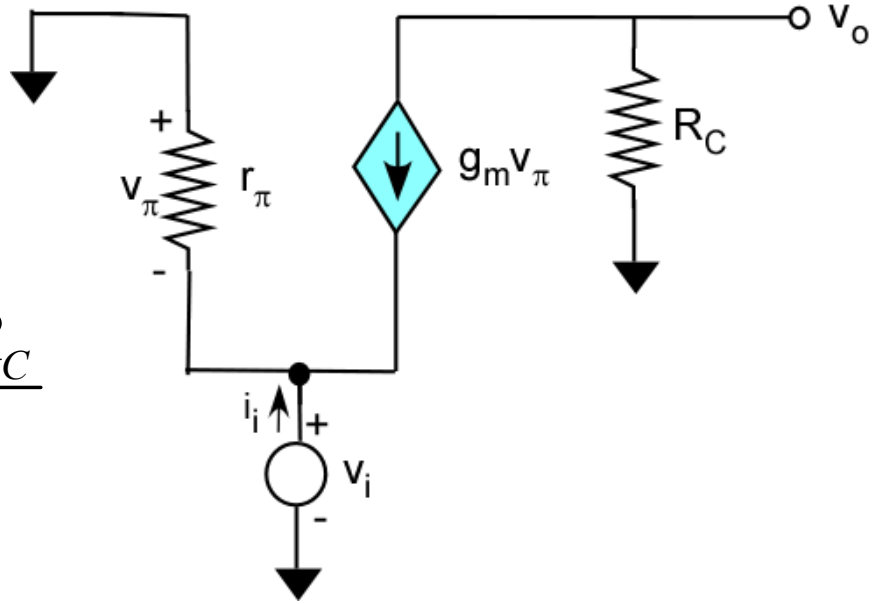
$$A'_{MB} = \frac{(\beta+1)R_E}{r_\pi + (\beta+1)R_E} \quad and \quad R'_{out} = R_E \,||\, \frac{r_\pi}{\beta+1}$$

Common Base Configuration



Common Base Configuration

$$v_i = -v_\pi, \quad v_o = -g_m v_\pi R_C = g_m v_i R_C$$



$$Voltage\ \ gain = \frac{v_o}{v_i} = g_m R_C = \frac{\alpha R_C}{r_e}$$

$$Current\ gain = \frac{i_o}{i_i} = \frac{g_m v_\pi}{i_i} = \frac{-g_m v_\pi}{\left(g_m + \frac{1}{r_\pi}\right)(-v_\pi)} = \frac{\beta}{\beta+1} = \alpha$$

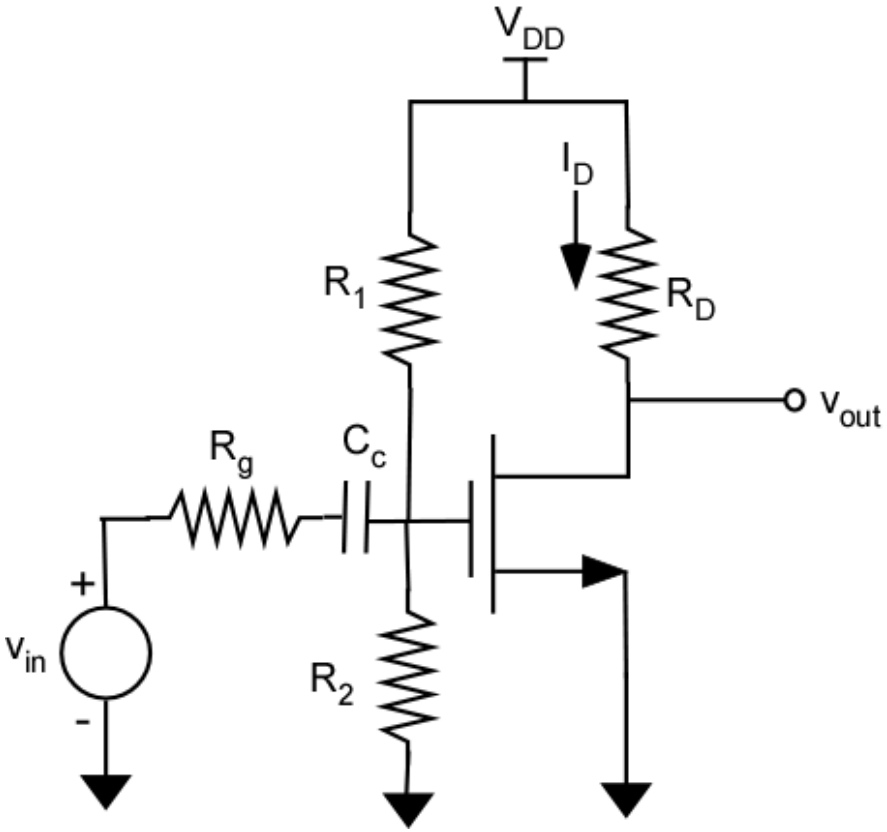
$$R_{out} = R_C$$

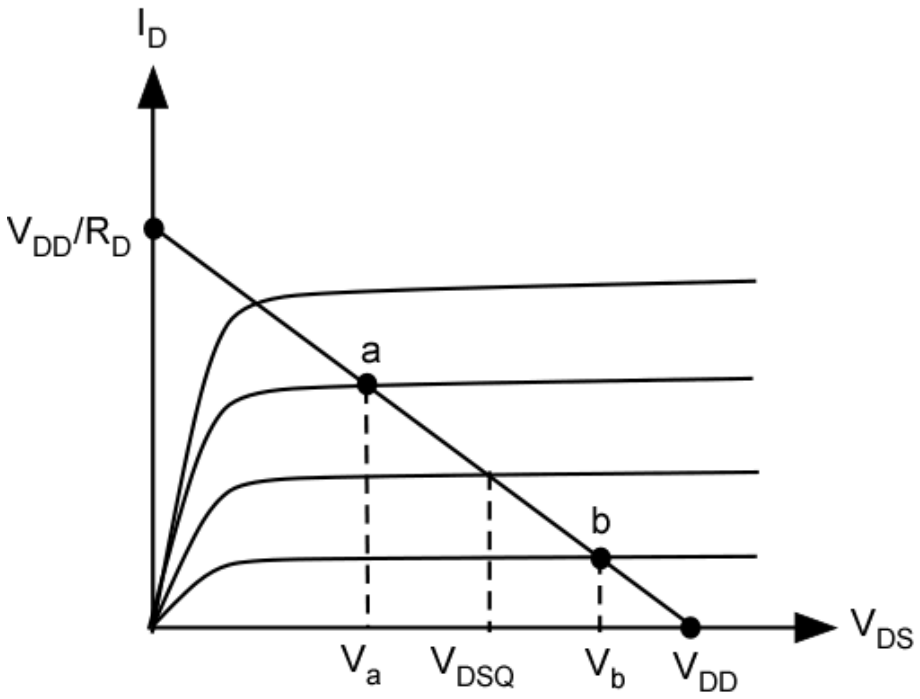
$$r_{in} = \frac{r_\pi}{\beta+1}$$

BJT Topologies - Summary

	CE	CB	EF
A_{vo}	$-g_m R_C$	$g_m R_C$	1
R_{in}	r_π	$\frac{r_\pi}{\beta+1}$	$r_\pi + R_E(\beta+1)$
R_{out}	R_C	R_C	$R_E \parallel r_\pi/(\beta+1)$

Common Source MOSFET Amplifier

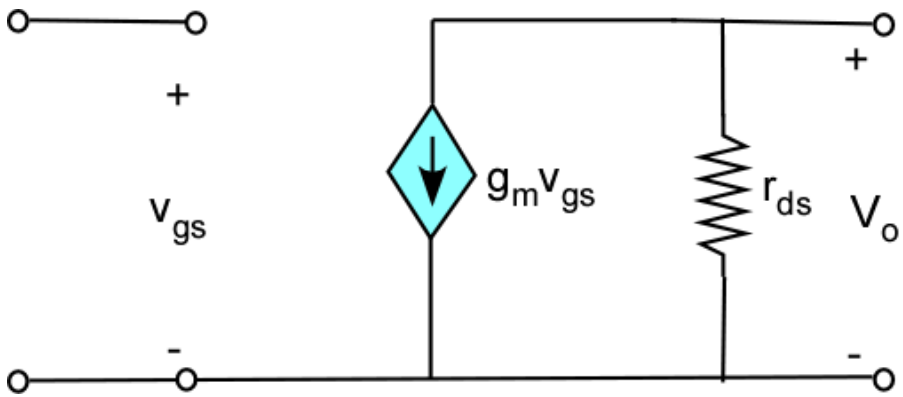




Bias is to keep MOS in saturation region

Common Source MOSFET Amplifier

Small-Signal Equivalent Circuit for MOS (device only)



$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2$$

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{GS}=V_{GSQ}} = \frac{2I_D}{V_{eff}}$$

$$where\ V_{GS} - V_T = V_{eff}$$

Which leads to

$$g_m = \sqrt{2k_n'}\ \sqrt{W/L}\ \sqrt{I_D}$$

$$g_m\ is\ proportional\ to = \sqrt{W/L}$$

MOSFET Output Impedance

To calculate r_{ds}, account for λ

$$r_{ds} = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_{V_{GS}=V_{GSQ}} = \frac{1}{\lambda\mu\frac{W}{2L}C_{ox}\left[V_{GS}-V_T\right]^2} = \frac{1}{\lambda I_{DP}}$$

$$I_{DP} = \frac{1}{2}k_n^{'}\frac{W}{L}\left(V_{GS}-V_T\right)^2$$

r_{ds}, accounts for channel width modulation resistance.

MOSFET Output Impedance

To calculate r_{ds}, account for λ

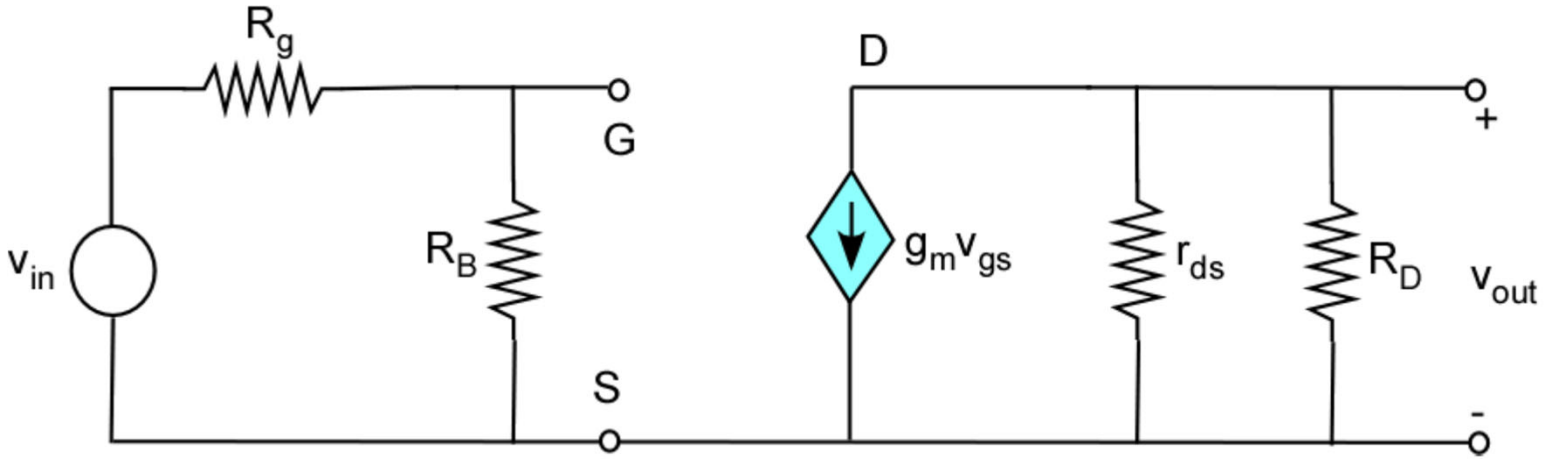
$$r_{ds} = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_{V_{GS}=V_{GSQ}} = \frac{1}{\lambda\mu\frac{W}{2L}C_{ox}\left[V_{GS}-V_T\right]^2} = \frac{1}{\lambda I_{DP}}$$

$$I_{DP} = \frac{1}{2}k_n^{'}\frac{W}{L}\left(V_{GS}-V_T\right)^2$$

r_{ds}, accounts for channel width modulation resistance.

Midband Frequency Gain

Incremental model for complete amplifier



$$A_{MB} = \frac{v_{out}}{v_{in}} = -\frac{R_B}{R_B + R_g} g_m \frac{r_{ds} R_D}{r_{ds} + R_D}$$

Body Effect

Potential on substrate affects threshold voltage

$$V_T(V_{SB}) = V_{To} + \gamma\left[\left(2|\phi_F| + V_{SB}\right)^{1/2} - \left(2|\phi_F|\right)^{1/2}\right]$$

$$|\phi_F| = \left(\frac{kT}{q}\right)\ln\left(\frac{N_a}{n_i}\right)$$

Fermi potential of material

$$\gamma = \frac{\left(2qN_a\varepsilon_s\right)^{1/2}}{C_{ox}}$$

Body bias coefficient

Body Effect – (Con't)

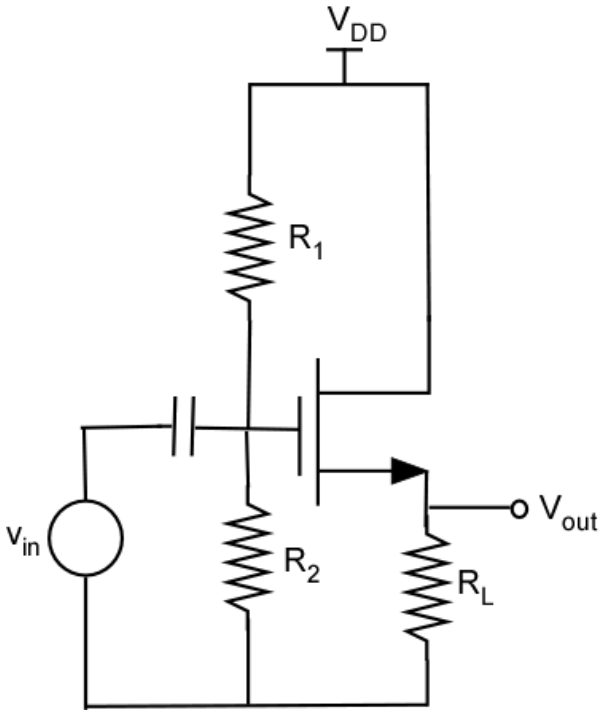
Define g_{mb} as the body transconductance

$$g_{mb} = \left.\frac{\partial I_D}{\partial V_{BS}}\right|_{\substack{V_{GS}=\text{constant} \\ V_{DS}=\text{constant}}}$$

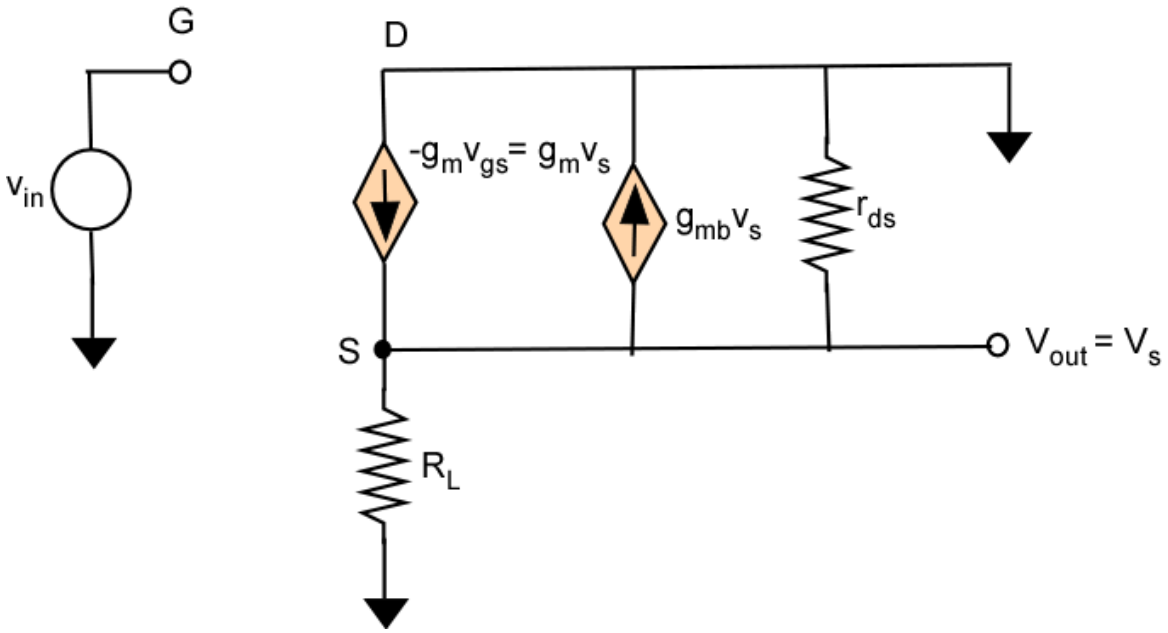
Can show that $$g_{mb} = \chi g_m$$

$$where\ \chi = \frac{\partial V_T}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{\phi_F + V_{SB}}}$$

Source Follower Configuration



Since source is not tied to the substrate, we need to model the body effect. Note: substrate is always tied to ground.



$$G_L = \frac{1}{R_L}$$

$$Define\ g_{ds} = \frac{1}{r_{ds}}\ and\ G = g_{ds} + g_{mb} + G_L$$

Source Follower

$$v_{out} = \frac{g_m v_{gs}}{G} = \frac{g_m \left(v_{in} - v_{out} \right)}{G}$$

$$v_{out} g_{ds} + v_{out} G_L + g_{mb} v_{out} = g_m v_{gs}$$

$$v_{out} G = g_m v_{gs} \Rightarrow v_{out} = \frac{g_m v_{gs}}{G} = \frac{g_m \left(v_{in} - v_{out} \right)}{G}$$

$$v_{out} G = g_m v_{in} - g_m v_{out}$$

Source Follower

$$v_{out}G = g_m v_{gs} \Rightarrow v_{out}\left(G + g_m\right) = g_m v_{in}$$

$$A_{GS} = \frac{g_m}{g_m + G} = \frac{g_m}{g_m + g_{mb} + g_{ds} + G_L}$$

$$A_{GS} = \frac{g_m}{g_m + G} = \frac{g_m}{g_m + g_{mb} + g_{ds} + G_L}$$

Source Follower

Neglecting G_L and g_{ds} (since they are small)

$$A_{GS} = \frac{g_m}{g_m + g_{mb}} \approx 1$$ This value is close to 1

Output impedance of source follower

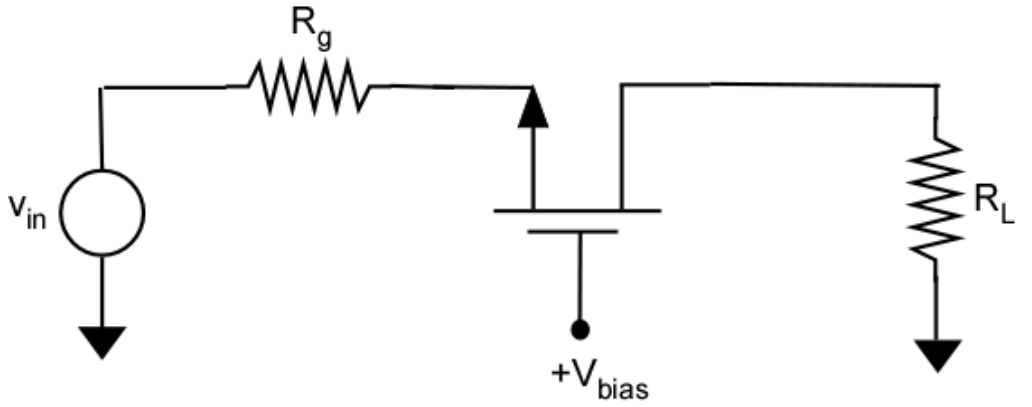
$$R_{out} = \frac{1}{g_m} \| \frac{1}{g_{mb}} \| r_{ds} \| R_L$$

Internal output impedance

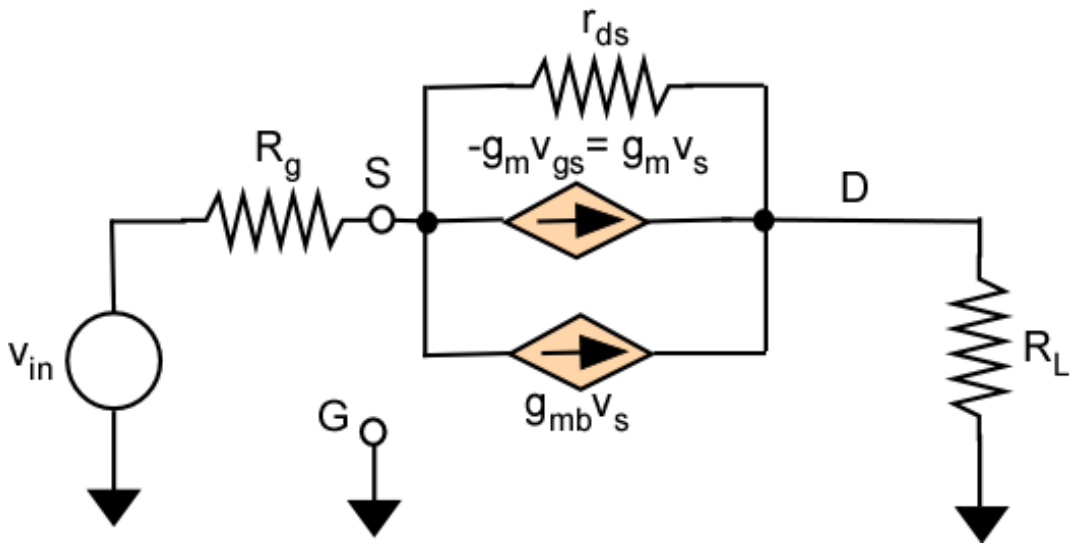
$$r_{out} = \frac{1}{g_m} \| \frac{1}{g_{mb}} \| r_{ds} \leftarrow \textit{This value is low}$$

Common Gate Amplifier

Circuit



Small-Signal Model



Common Gate Amplifier

$$A_{MB} = \frac{g_m + g_{mb} + g_{ds}}{G_L + g_{ds} + \left(g_m + g_{mb} + g_{ds}\right) G_L / G_g}$$

$$g_{ds} \ll \left(g_m + g_{mb}\right) to\ get$$

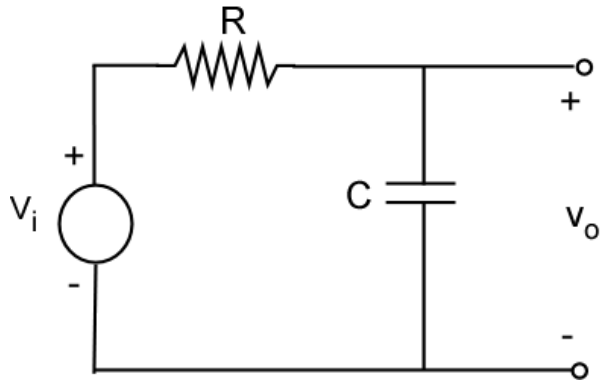
$$A_{MB} = \frac{\left(g_m + g_{mb}\right) R_L}{1 + \left(g_m + g_{mb}\right) R_g}$$

- **Common Gate (CG)**
  - CG amplifier is non-inverting
  - CG amplifier has low input impedance
  - CG is unity current-gain amplifier

MOS Topologies - Ideal

	CS	CG	SF
A_{vo}	$-g_m R_D$	$g_m R_D$	1
R_{in}	∞	$\frac{1}{g_m}$	∞
R_{out}	R_D	R_D	$\frac{1}{g_m}$

Low-Pass Circuit



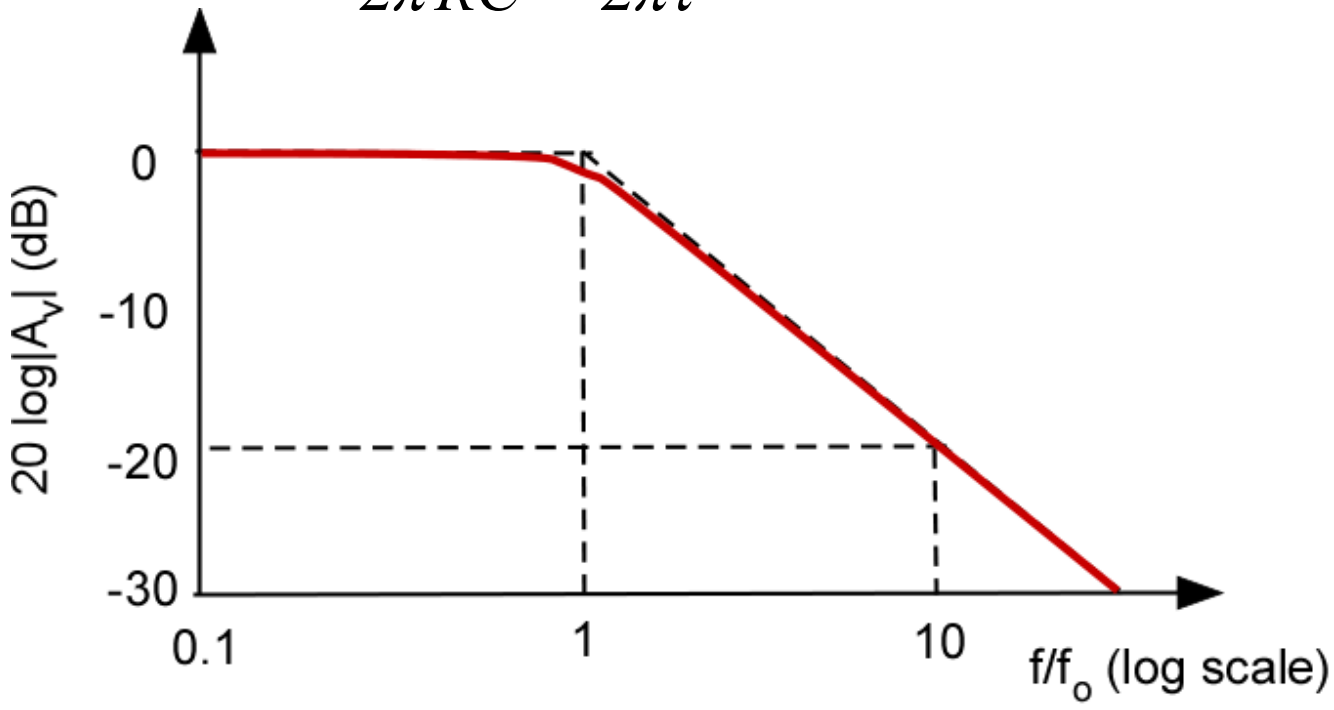
In frequency domain: $$V_o = \frac{V_i}{R + \frac{1}{j\omega C}} \cdot \frac{1}{j\omega C}$$

$$V_o = \frac{V_i}{1 + j\omega RC} \Rightarrow A_v = \frac{V_o}{V_i} = \frac{1}{1 + j\omega RC}$$

$$A_v = \frac{1}{1 + j\omega RC} = \frac{1}{1 + jf / f_2}$$

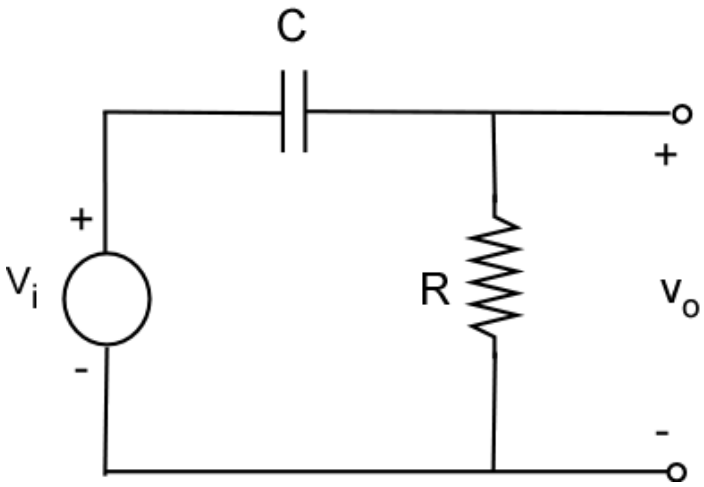
Low-Pass Circuit

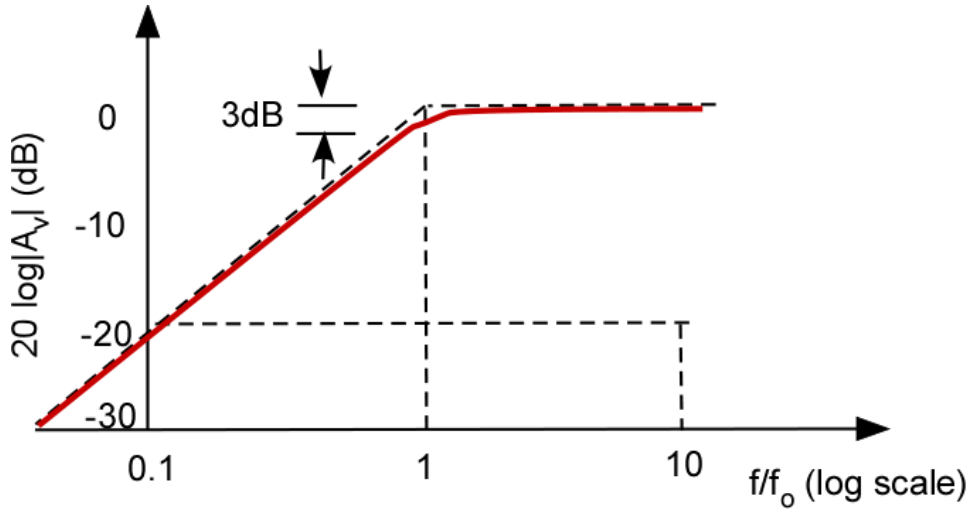
$$f_2 = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau}$$



$$\tau = 2\pi RC = \text{time constant}$$

High-Pass Circuit



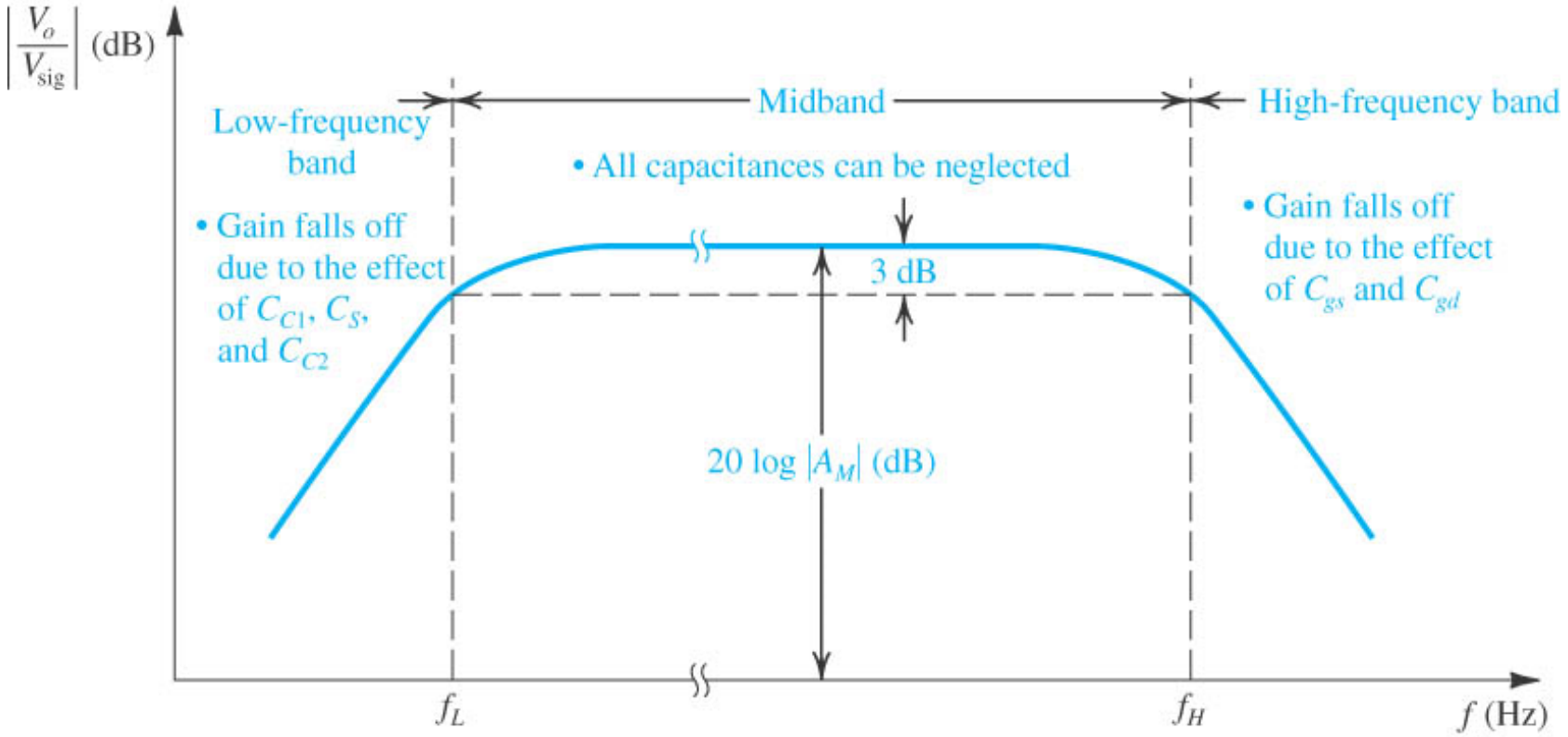


$$V_o = \frac{V_i R}{R + \frac{1}{j\omega C}} = \frac{V_i}{1 + \frac{1}{j\omega RC}}$$

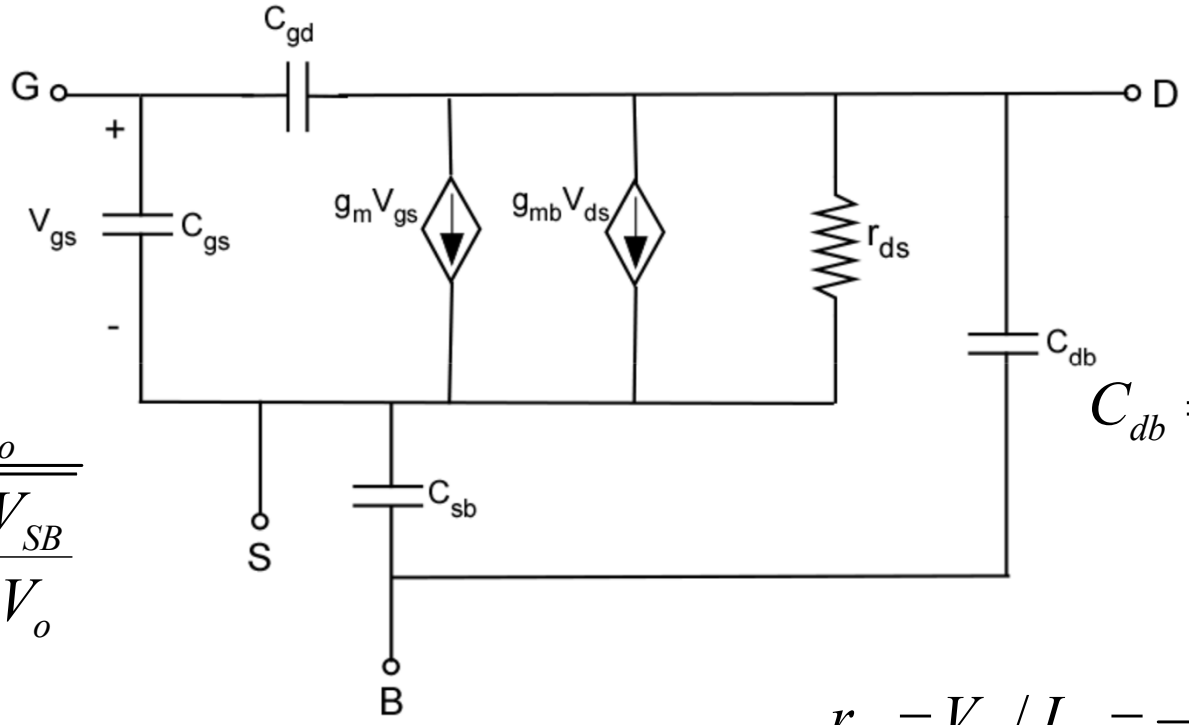
$$A_v = \frac{V_o}{V_i} = \frac{1}{1 - j\frac{1}{2\pi fRC}} = \frac{1}{1 - jf_2 / f}$$

$$f_2 = \frac{1}{2\pi RC}$$

Three Frequency Bands



MOSFET High-Frequency Model



$$C_{sb} = \frac{C_{sbo}}{\sqrt{1 + \frac{V_{SB}}{V_o}}}$$

$$C_{db} = \frac{C_{dbo}}{\sqrt{1 + \frac{V_{DB}}{V_o}}}$$

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{eff} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{eff}}$$

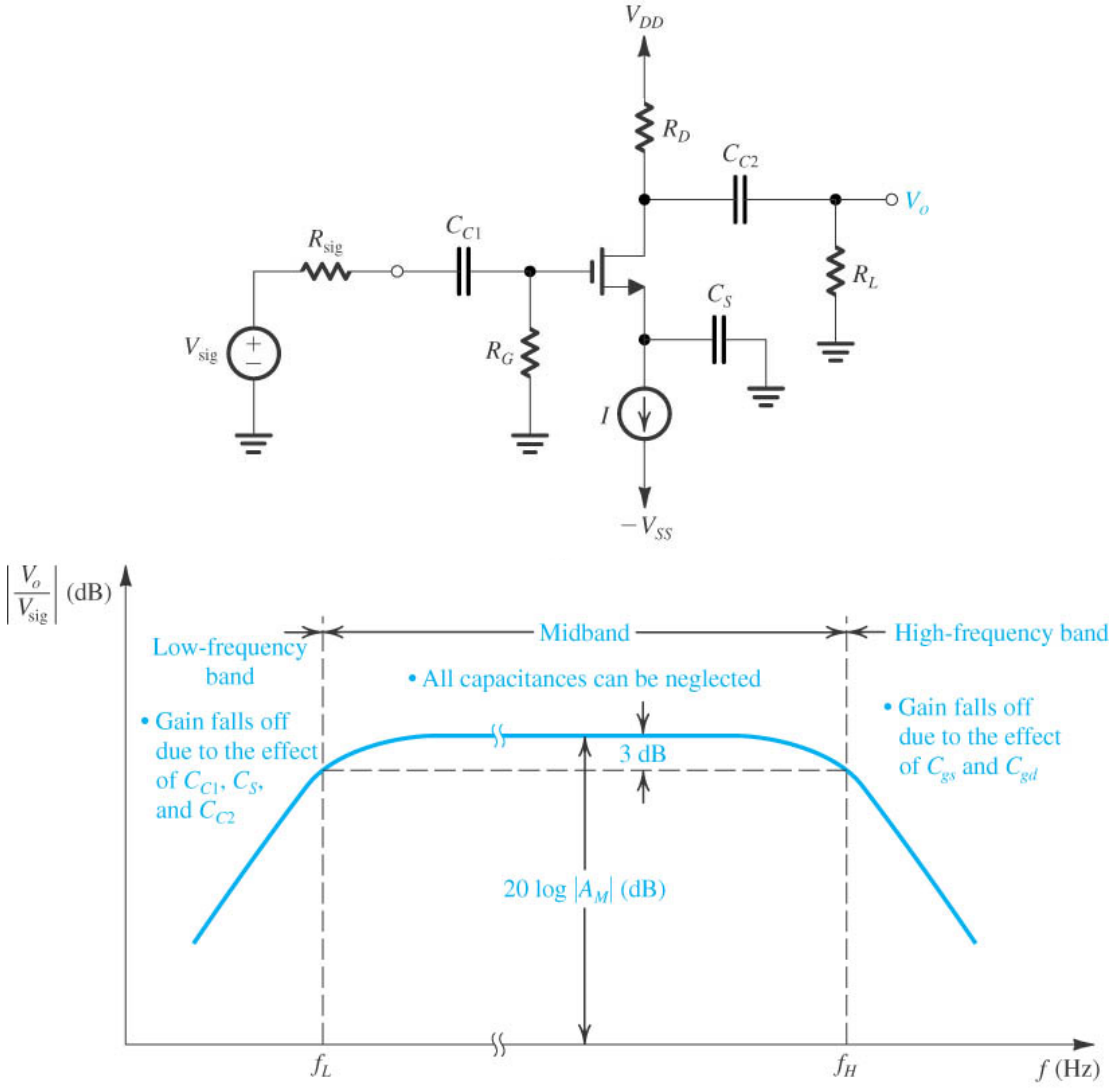
$$g_{mb} = \chi g_m = \frac{\gamma}{2\sqrt{2\phi_F + V_{sb}}} g_m$$

$$r_{ds} = V_A / I_D = \frac{1}{\lambda I_D}$$

$$C_{gs} = \frac{2}{3} WLC_{ox} + WL_{ov}C_{ox}$$

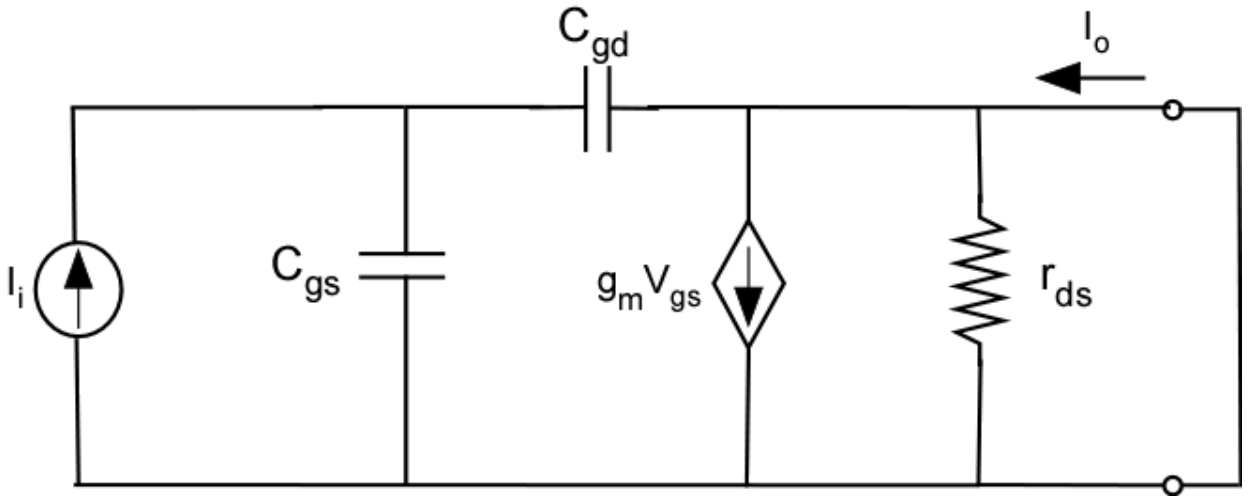
$$C_{gd} = WL_{ov}C_{ox}$$

CS - Three Frequency Bands



Unity-Gain Frequency f_T

f_T is defined as the frequency at which the short-circuit current gain of the common source configuration becomes unity



Define:

$$s = j\omega$$

(neglect $sC_{gd}V_{gs}$ since C_{gd} is small)

$$I_o = g_m V_{gs} - sC_{gd}V_{gs}$$

$$I_o \simeq g_m V_{gs}$$

$$V_{gs} = \frac{I_i}{s\left(C_{gs} + C_{gd}\right)}$$

$$\frac{I_o}{I_i} = \frac{g_m}{s\left(C_{gs} + C_{gd}\right)}$$

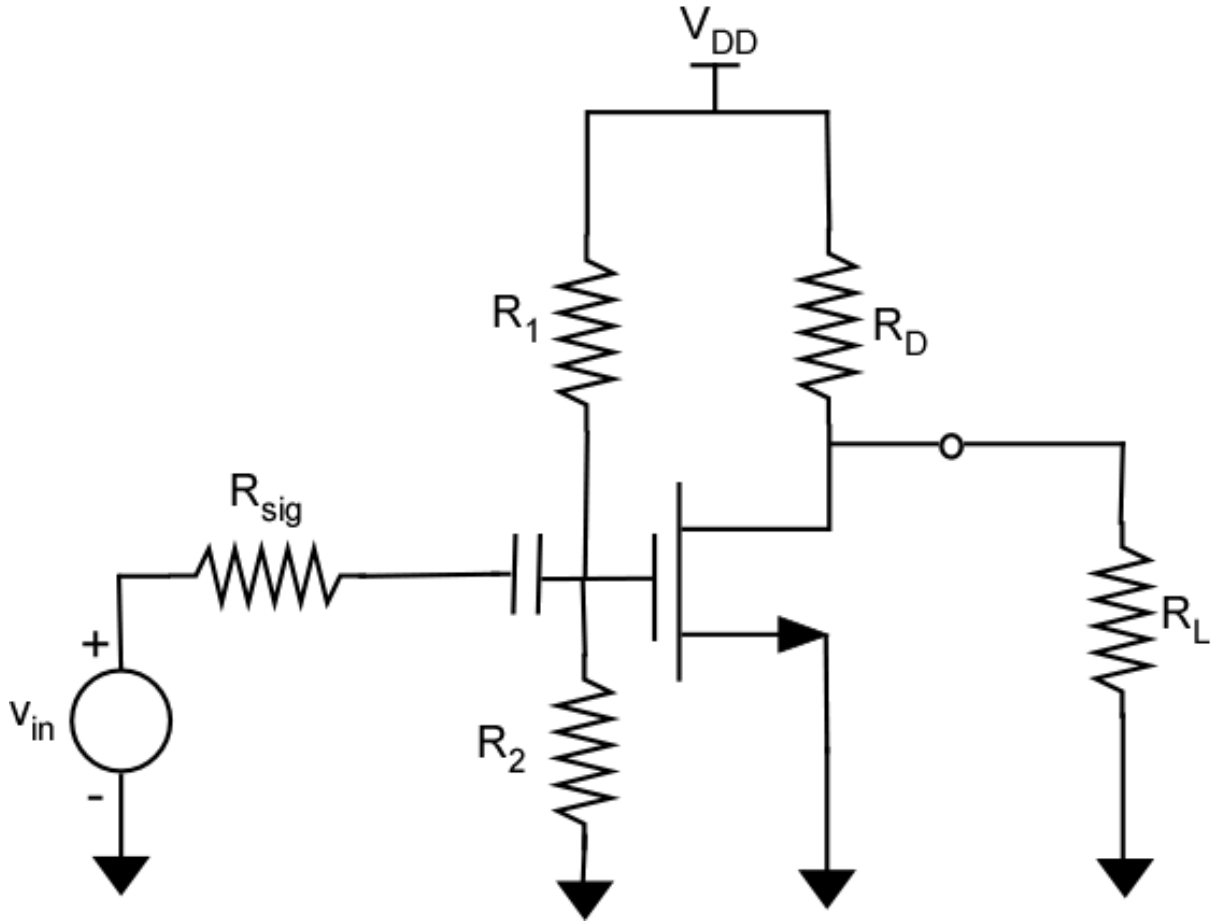
Calculating f_T

For $s=j\omega$, magnitude of current gain becomes unity at

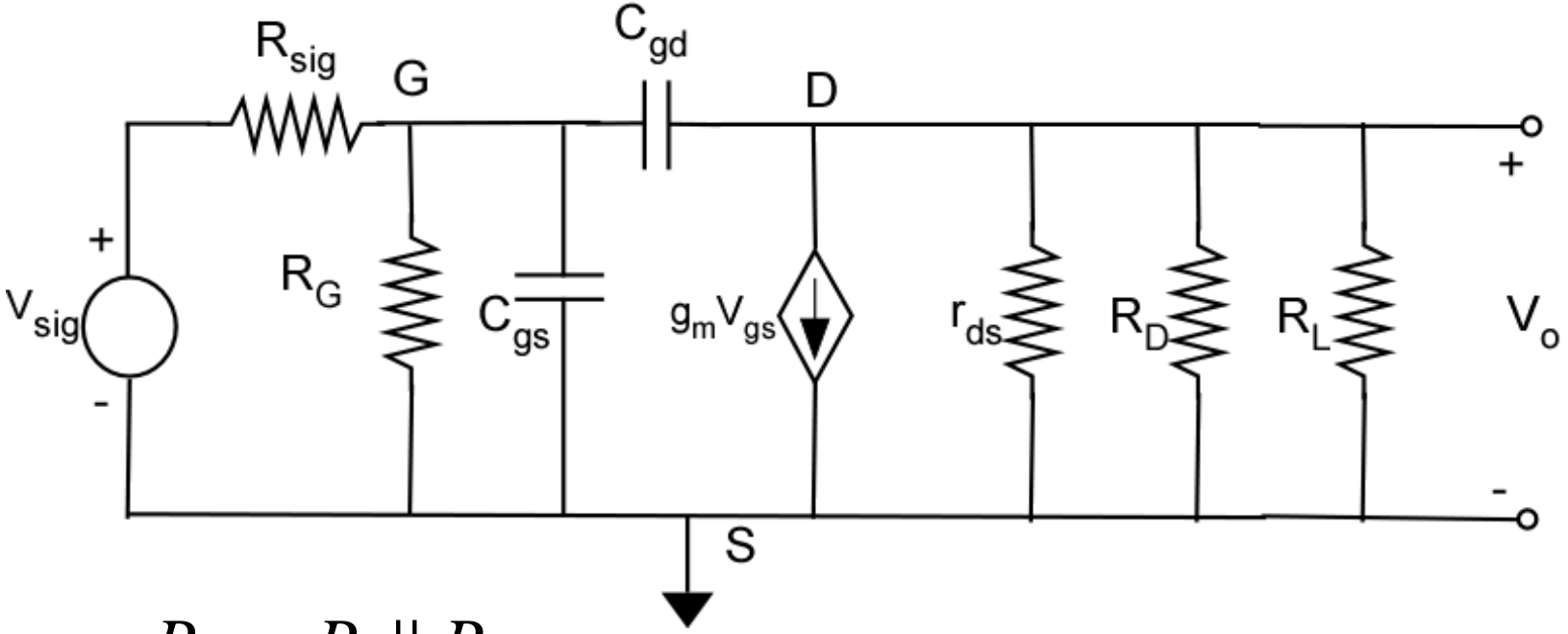
$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}} \Rightarrow f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}$$

f_T ~ 100 MHz for 5-μm CMOS, f_T ~ several GHz for 0.13μm CMOS

CS - High-Frequency Response



CS - High-Frequency Response

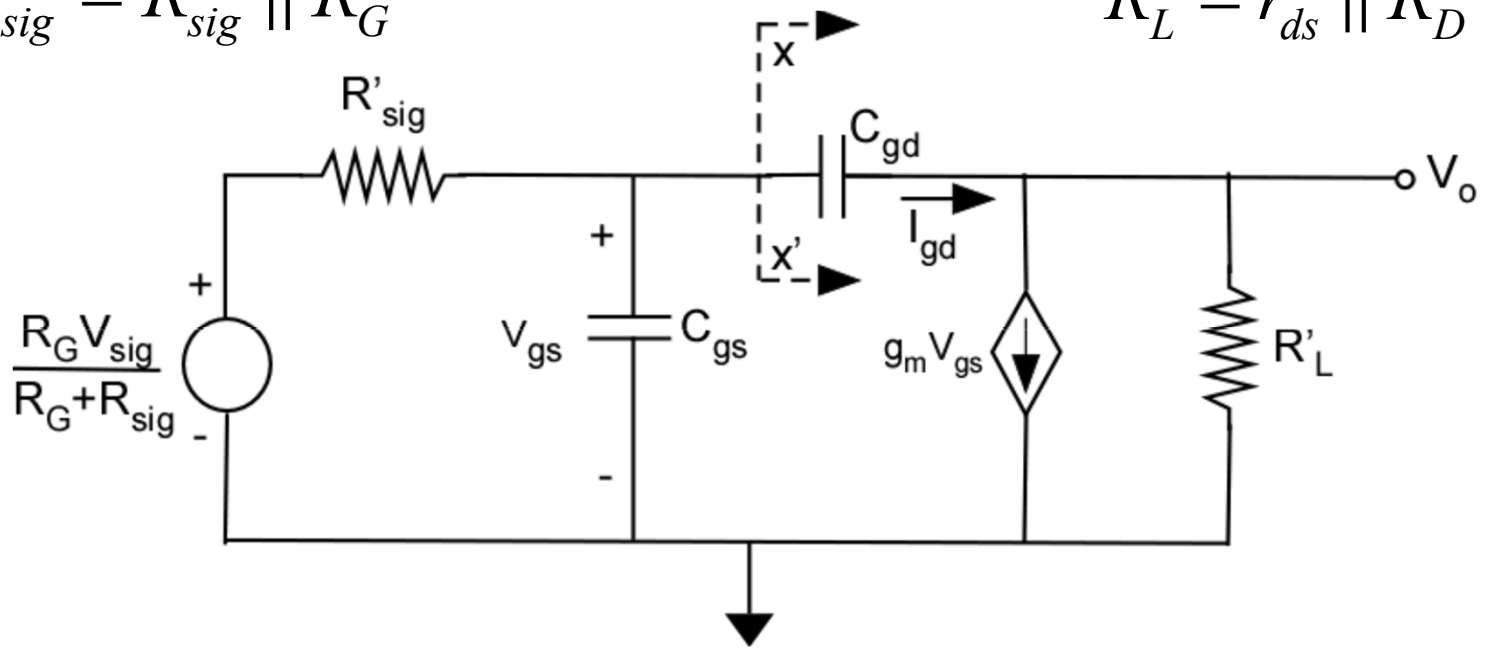


$$R_G = R_1 \,||\, R_2$$

CS - High-Frequency Response

$$R'_{sig} = R_{sig} \parallel R_G$$

$$R'_L = r_{ds} \parallel R_D \parallel R_L$$



$$I_{gd} = sC_{gd}\left(V_{gs} - V_o\right) = sC_{gd}\left[V_{gs} - \left(-g_m R'_L V_{gs}\right)\right]$$

$$I_{gd} = sC_{gd}\left(1 + g_m R'_L\right)V_{gs}$$

CS – Miller Effect

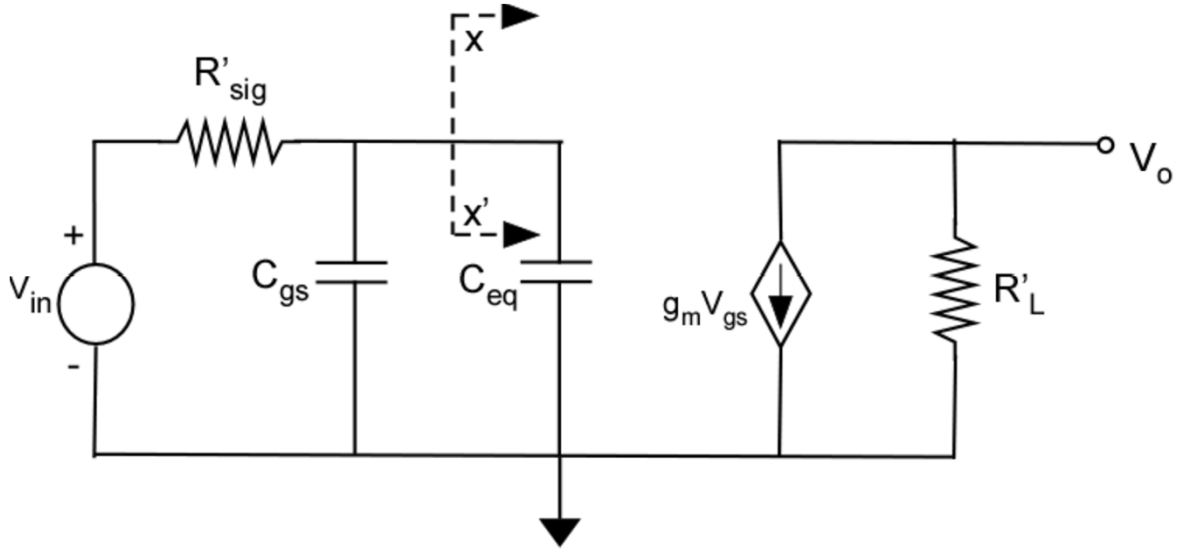
Define C_{eq} such that

$$sC_{eq}V_{gs} = sC_{gd}\left(1+g_m R_L^{'}\right)V_{gs}$$

$$V_o = -g_m R_L^{'} V_{gs}$$

$$C_{eq} = C_{gd}\left(1+g_m R_L^{'}\right) = \text{Miller Capacitance}$$

$$v_{in} = \frac{R_g V_{sig}}{R_g + R_{sig}}$$



CS – Miller Effect

$$V_{gs} = \left(\frac{R_G V_{sig}}{R_G + R_{sig}} \right) \frac{1}{1 + jf / f_o}$$

f_o is the corner frequency of the STC circuit

$$f_o = \frac{1}{2\pi C_{in} R'_{sig}}$$

$$C_{in} = C_{gs} + C_{eq} = C_{gs} + \overbrace{C_{gd}\left(1 + g_m R'_L\right)}^{Miller}$$

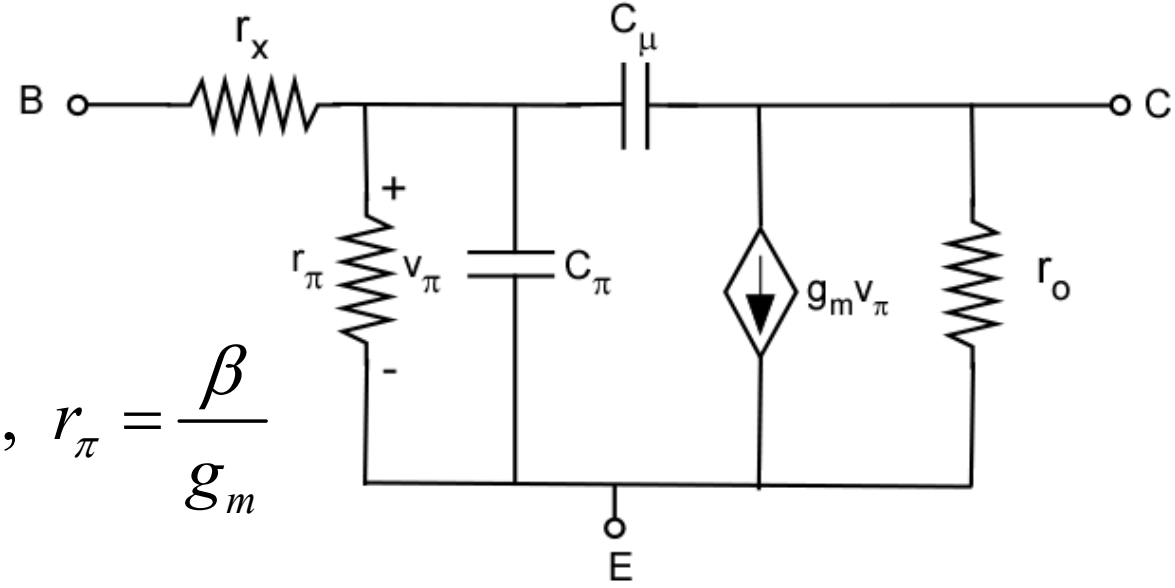
CS – Miller Effect

$$\frac{V_o}{V_{sig}} = -\left(\frac{R_G}{R_G + R_{sig}}\right) g_m R_L^{'} \frac{1}{1 + jf / f_o}$$

$$\frac{V_o}{V_{sig}} = \frac{A_M}{1 + jf / f_H}$$

$$f_H = f_o = \frac{1}{2\pi C_{in} R_{sig}^{'}}$$

High-Frequency Hybrid-π Model

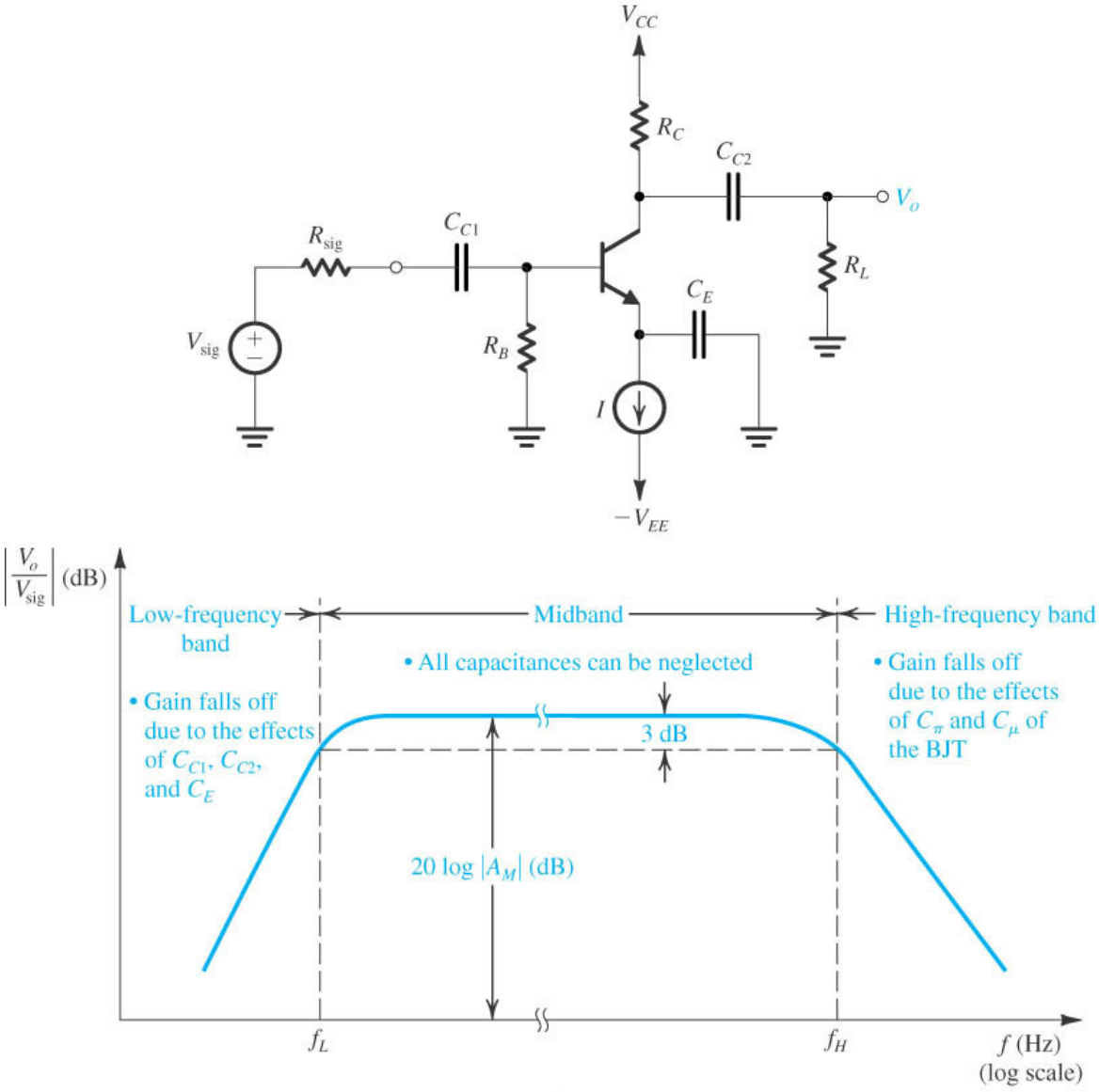


$$g_m = \frac{I_C}{V_T},\ r_o = \frac{|V_A|}{I_C},\ r_\pi = \frac{\beta}{g_m}$$

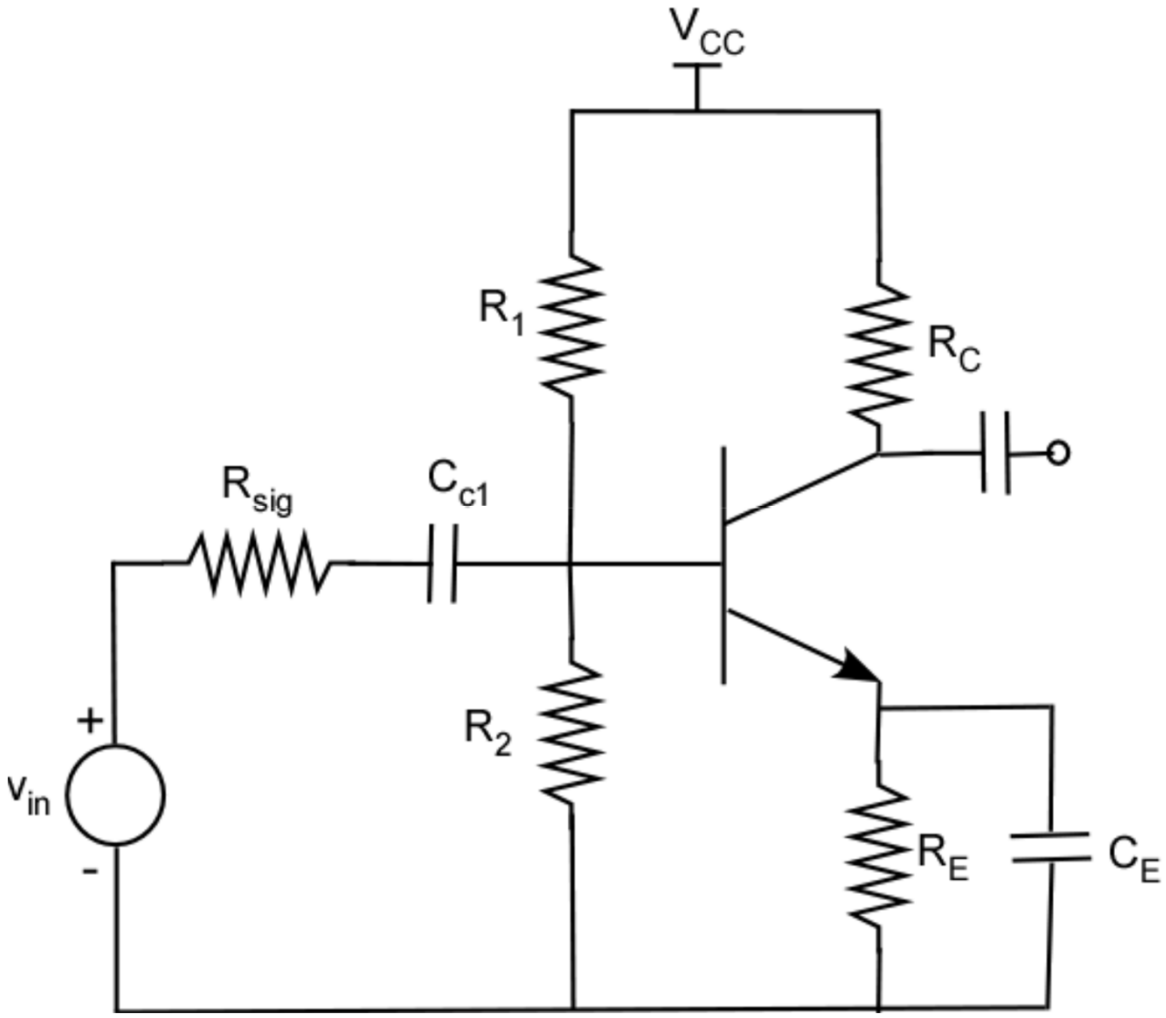
$$C_\pi + C_\mu = \frac{g_m}{2\pi f_T},\quad C_\pi = C_{de} + C_{je},\ C_{de} = \tau_F g_m$$

$$C_\mu = \frac{C_{jco}}{\left(1 + \frac{V_{CB}}{V_{oe}}\right)^m},\quad m = 0.3 - 0.5 \qquad f_T = \frac{g_m}{2\pi\left(C_\pi + C_\mu\right)}$$

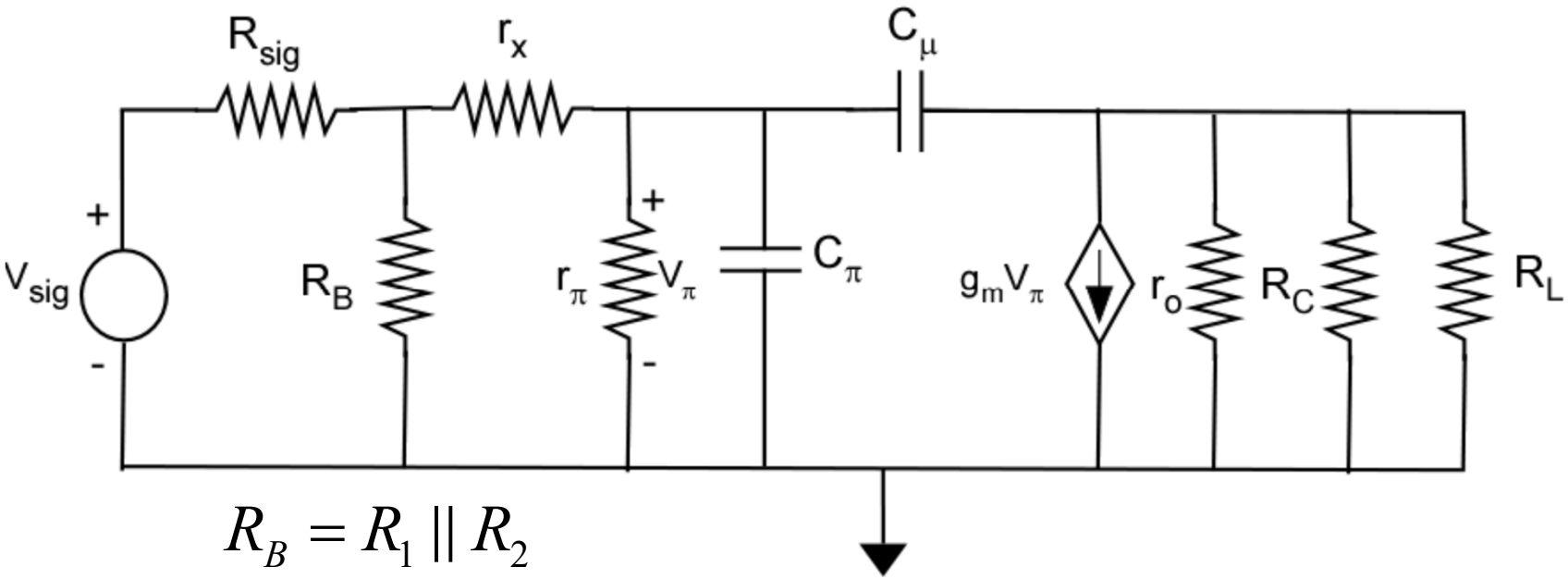
CE - Three Frequency Bands



CE High-Frequency Model

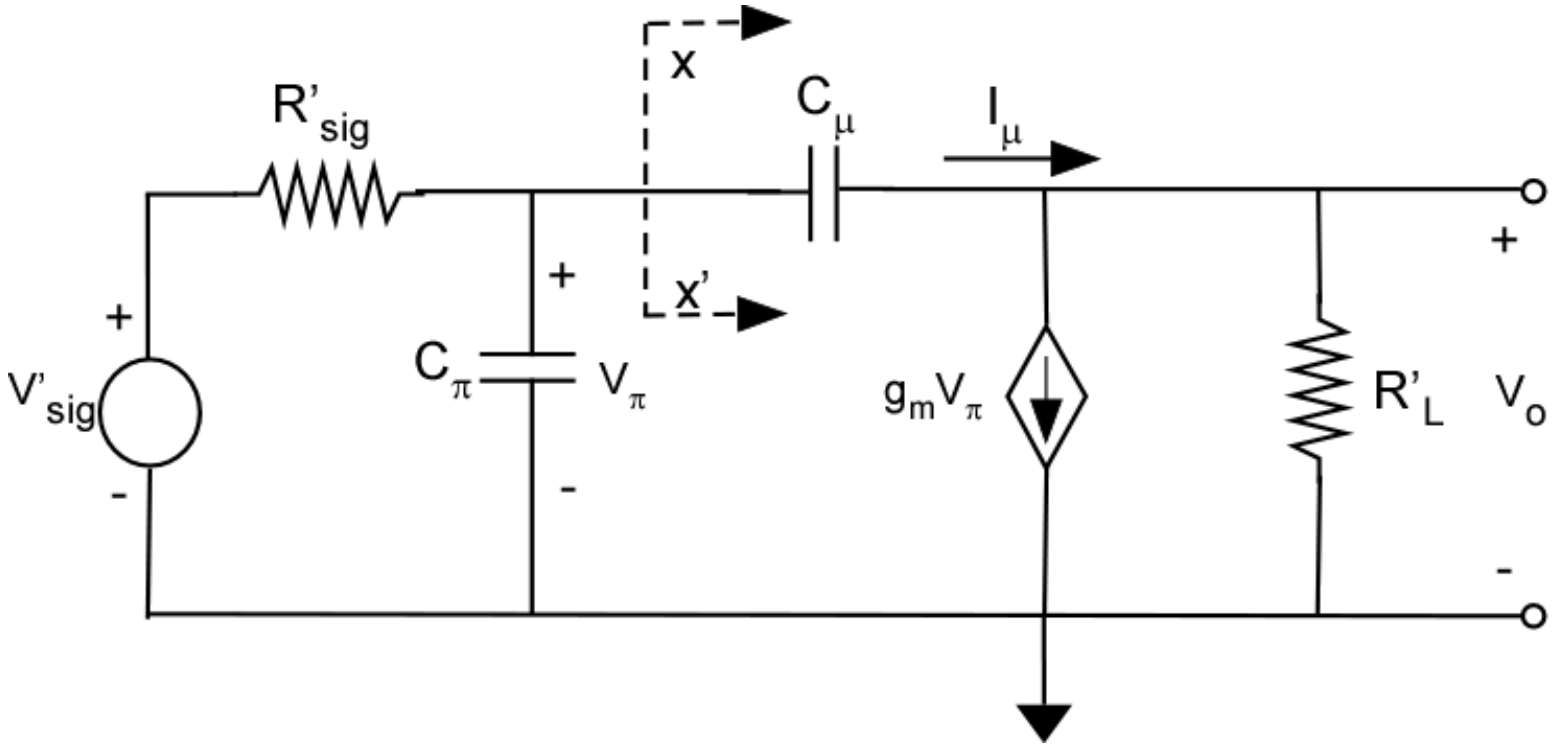


CE High-Frequency Model



$$R_B = R_1 \,||\, R_2$$

CE High-Frequency Model



$$V_{sig}^{'} = V_{sig} \cdot \frac{R_B}{R_B + R_{sig}} \cdot \frac{r_\pi}{r_\pi + r_x + \left(R_{sig} \,||\, R_B \right)}$$

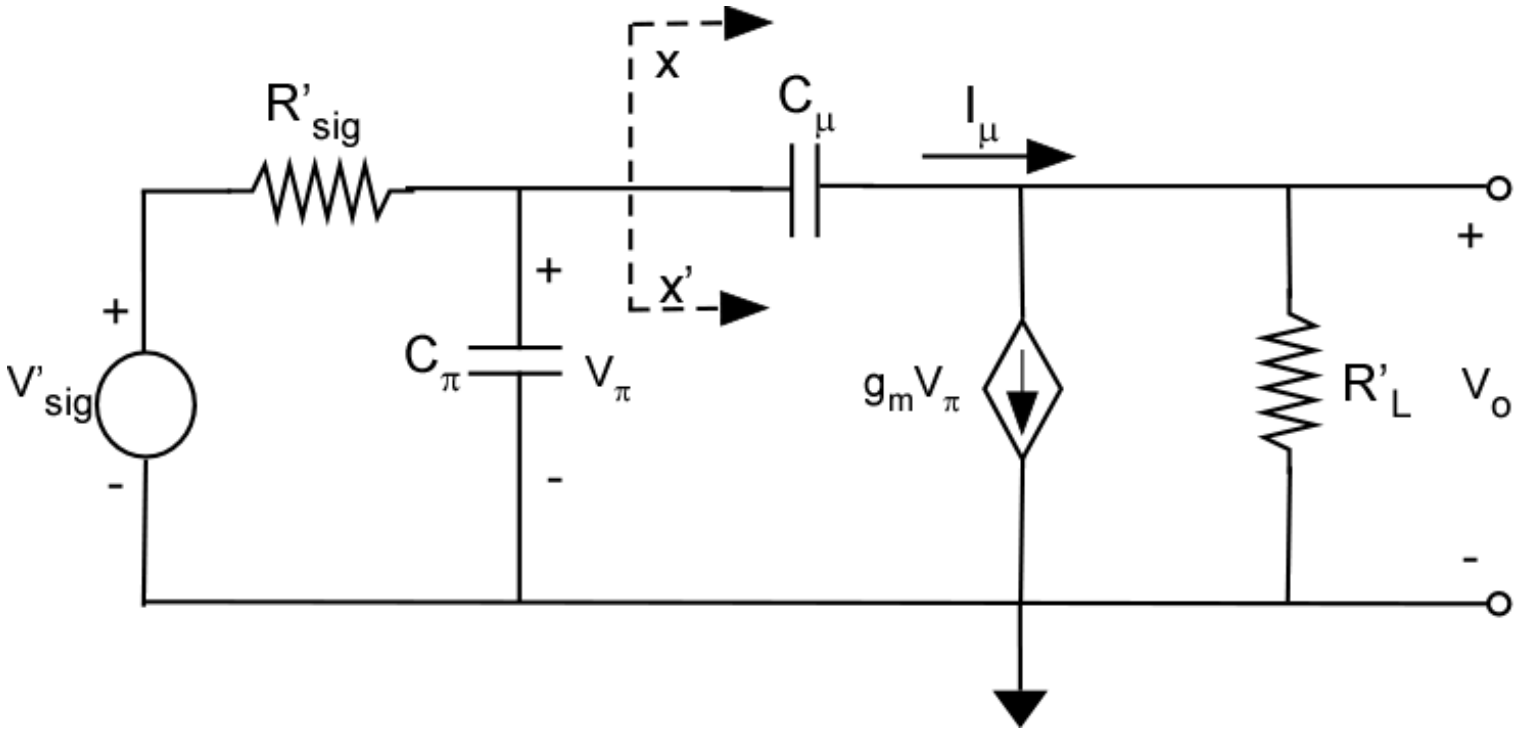
CE High-Frequency Model

$$R_{sig}^{'} = r_{\pi} \,||\left[r_x + \left(R_{sig} \,||\, R_B \right) \right]$$

$$R_L^{'} = r_o \,||\, R_C \,||\, R_L$$

$$V_o \simeq -g_m v_{\pi} R_L^{'}$$

Bipolar Miller Effect



The left hand side of the circuit at XX' knows the existence of C_μ only through the current I_μ ➔ replace C_μ with C_{eq} from base to ground

Bipolar Miller Effect

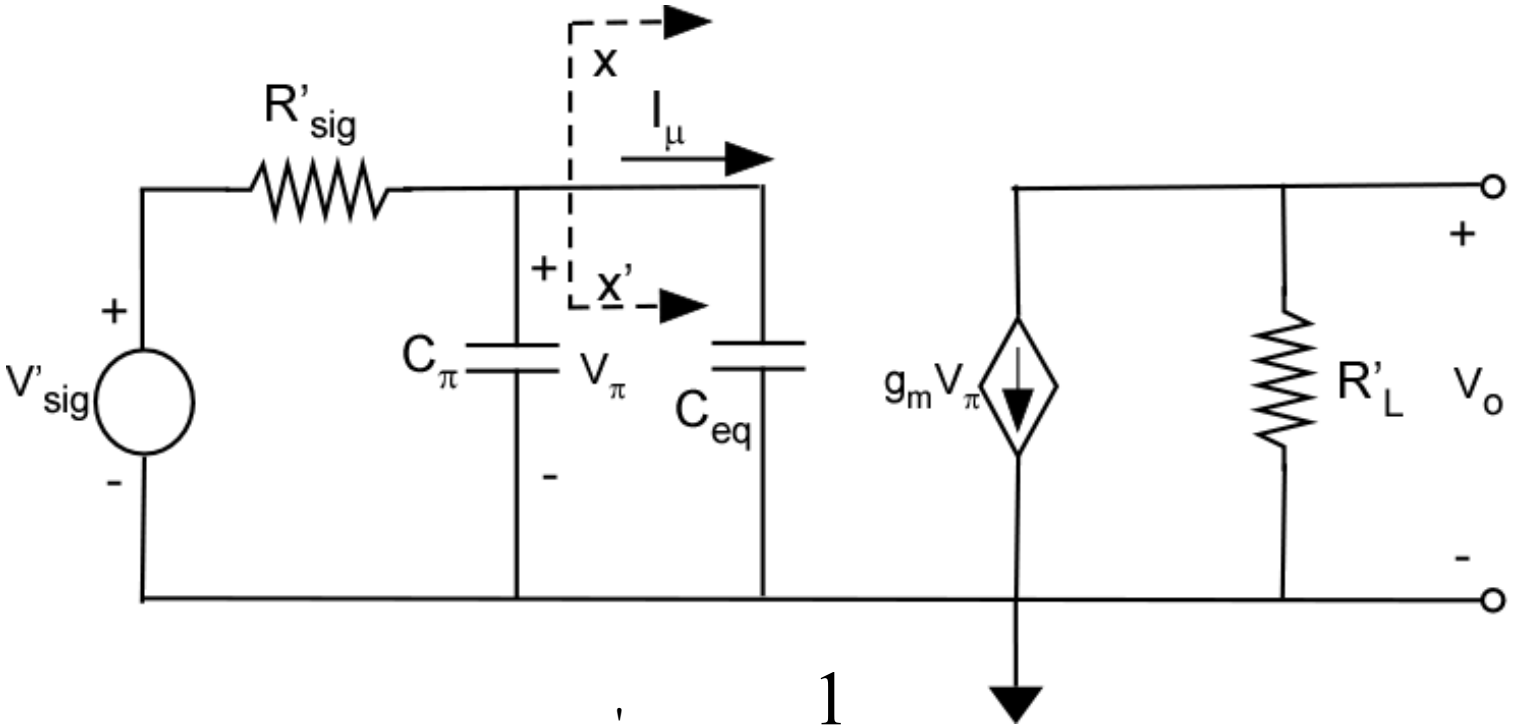
$$I_\mu = sC_\mu\left(v_\pi - v_o\right) = sC_\mu\left[v_\pi - \left(-g_m R_L^{'} v_\pi\right)\right]$$

$$I_\mu = sC_\mu\left(1 + g_m R_L^{'}\right)v_\pi$$

$$sC_{eq}v_\pi = I_\mu = sC_\mu\left(1 + g_m R_L^{'}\right)v_\pi$$

$$C_{eq} = C_\mu\left(1 + g_m R_L^{'}\right), \text{ Miller capacitance for BJT}$$

Bipolar Miller Effect



$$v_\pi = v'_{sig}\frac{1}{1+jf/f_o}$$

$$f_o = \frac{1}{2\pi C_{in} R'_{sig}}$$

Bipolar Miller Effect (cont')

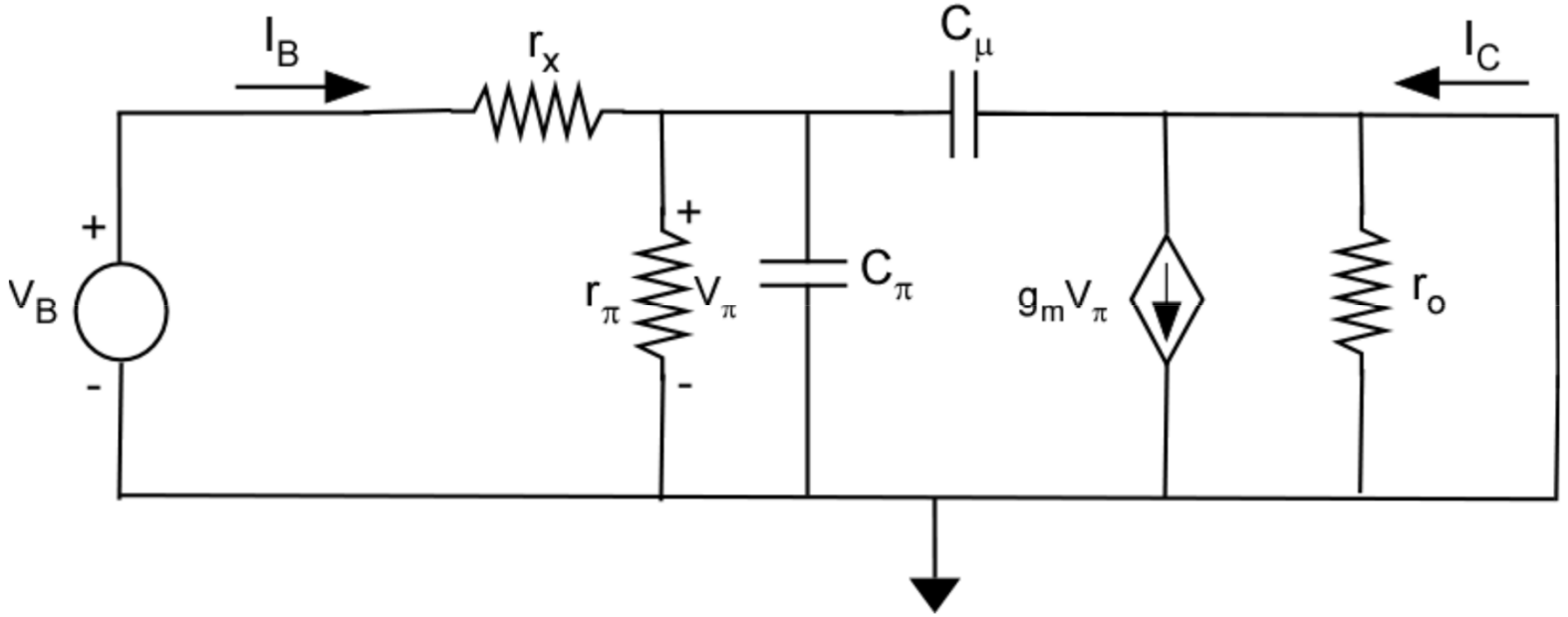
$$where\ C_{in} = C_{\pi} + C_{eq} = C_{\pi} + C_{\mu}\left(1 + g_m R_L^{'}\right)$$

$$\frac{V_o}{V_{sig}} = \left[\frac{R_B}{R_B + R_{sig}} \cdot \frac{r_{\pi} g_m R_L^{'}}{r_{\pi} + r_x + \left(R_{sig} \,||\, R_B\right)}\right]\left[\frac{1}{1 + jf / f_o}\right]$$

$$\frac{V_o}{V_{sig}} = A_M \frac{1}{1 + jf / f_o}$$

$$f_H = f_o = \frac{1}{2\pi C_{in} R_{sig}^{'}}$$

Short-Circuit Current Gain



$$I_C = \left(g_m - sC_\mu\right)v_\pi$$

$$v_\pi = \frac{I_B}{\frac{1}{r_\pi} + sC_\mu + sC_\pi}$$

Short-Circuit Current Gain (Cont')

Define h_{fe} as short-circuit current gain

$$h_{fe} = \frac{I_C}{I_B} = \frac{g_m - sC_\mu}{\frac{1}{r_\pi} + s\left(C_\pi + C_\mu\right)}$$

$$g_m \gg sC_\mu \text{ at freq. of interest}$$

$$h_{fe} = \frac{I_C}{I_B} = \frac{g_m r_\pi}{1 + s\left(C_\pi + C_\mu\right) r_\pi}$$

Short-Circuit Current Gain (con't)

$$h_{fe} = \frac{\beta_o}{1 + s\left(C_\pi + C_\mu\right) r_\pi}$$

Define h_{fe} has a single pole (or STC) response. Unity gain bandwidth is for:

$$h_{fe} = \frac{g_m r_\pi}{1 + s\left(C_\pi + C_\mu\right) r_\pi} = 1 \quad or \quad \frac{g_m}{2\pi f_T \left(C_\pi + C_\mu\right)} = 1$$

In some cases, if C_μ is known, then

Short-Circuit Current Gain (con't)

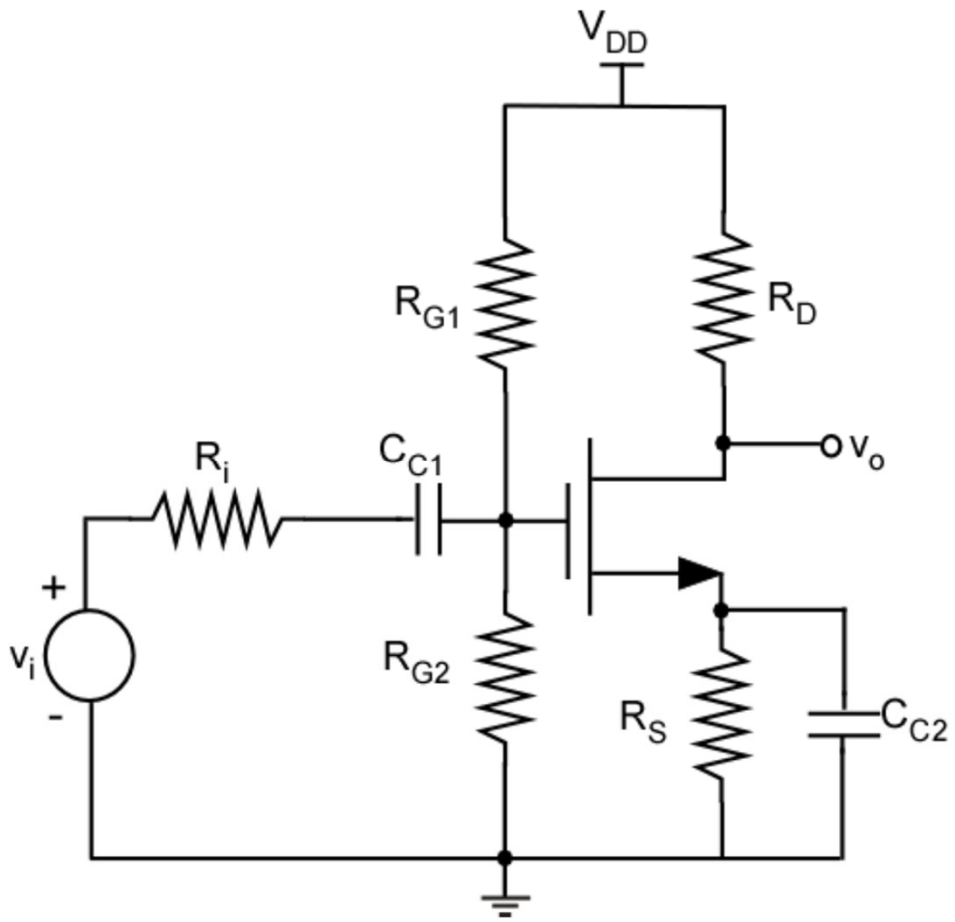
$$f_T = \frac{g_m}{2\pi\left(C_\pi + C_\mu\right)}$$

From which we get

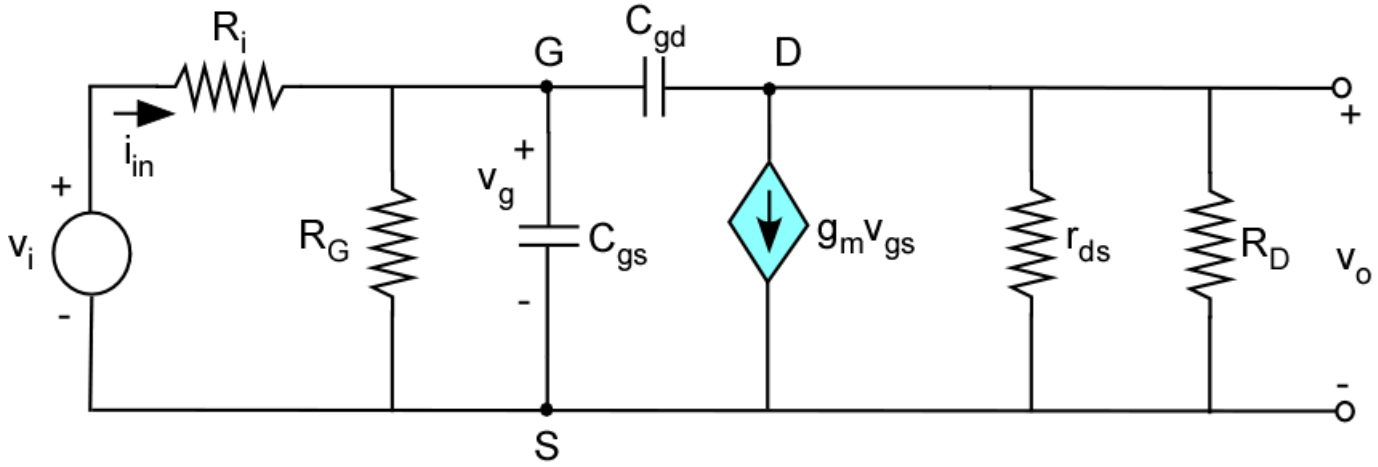
$$C_\pi + C_\mu = \frac{g_m}{2\pi f_T} = \frac{g_m}{\omega_T}$$

$$Thus,\ C_\pi + C_\mu = \frac{g_m}{\omega_T} \Rightarrow C_\pi = \frac{g_m}{\omega_T} - C_\mu$$

CS – Miller Effect – Exact Analysis



CS – Miller Effect – Exact Analysis



$$G_i = \frac{1}{R_i} \qquad G_D = \frac{1}{R_D} \qquad G_g = \frac{1}{R_g} \qquad g_{ds} = \frac{1}{r_{ds}}$$

$$R_D' = R_D \,//\, r_{ds} = \frac{1}{G_D + g_{ds}}$$

$$\frac{v_o}{v_i} = -\frac{G_i R_D' \left(g_m - sC_{gd} \right)}{G_i + G_g + s\left[C_{gs} + C_{gd} \right] + sC_{gd} R_D' \left[G_i + G_g \right] + sC_{gd} g_m R_D' + s^2 C_{gd} C_{gs} R_D'}$$

CS – Miller Effect – Exact Analysis

We neglect the terms in s^2 since

$$\left|s^2 C_{gd} C_{gs} R_D^{'}\right| \ll \left|sC_{gd} g_m R_D^{'}\right| \quad or \left|sC_{gs}\right| \ll \left|g_m\right|$$

$$\frac{v_o}{v_i} = -\frac{G_i R_D^{'}\left(g_m - sC_{gd}\right)}{G_i + G_g + s\left[C_{gs} + C_{gd}\left(1 + g_m R_D^{'}\right) + C_{gd} R_D^{'}\left(G_i + G_g\right)\right]}$$

If we multiply through by $R_i = \frac{1}{G_i}$

CS – Miller Effect – Exact Analysis

$$\frac{v_o}{v_i} = -\frac{R_D^{'}\left(g_m - sC_{gd}\right)}{1 + R_i G_g + s\left\{R_i\left[C_{gs} + C_{gd}\left(1 + g_m R_D^{'}\right)\right] + C_{gd} R_D^{'}\left(1 + R_s G_g\right)\right\}}$$

From which we extract the 3-dB frequency point

$$f_H = \frac{1 + R_i G_g}{2\pi\left\{R_i\left[C_{gs} + C_{gd}\left(1 + g_m R_D^{'}\right)\right] + C_{gd} R_D^{'}\left(1 + R_i G_g\right)\right\}}$$

CS – Miller Effect – Exact Analysis

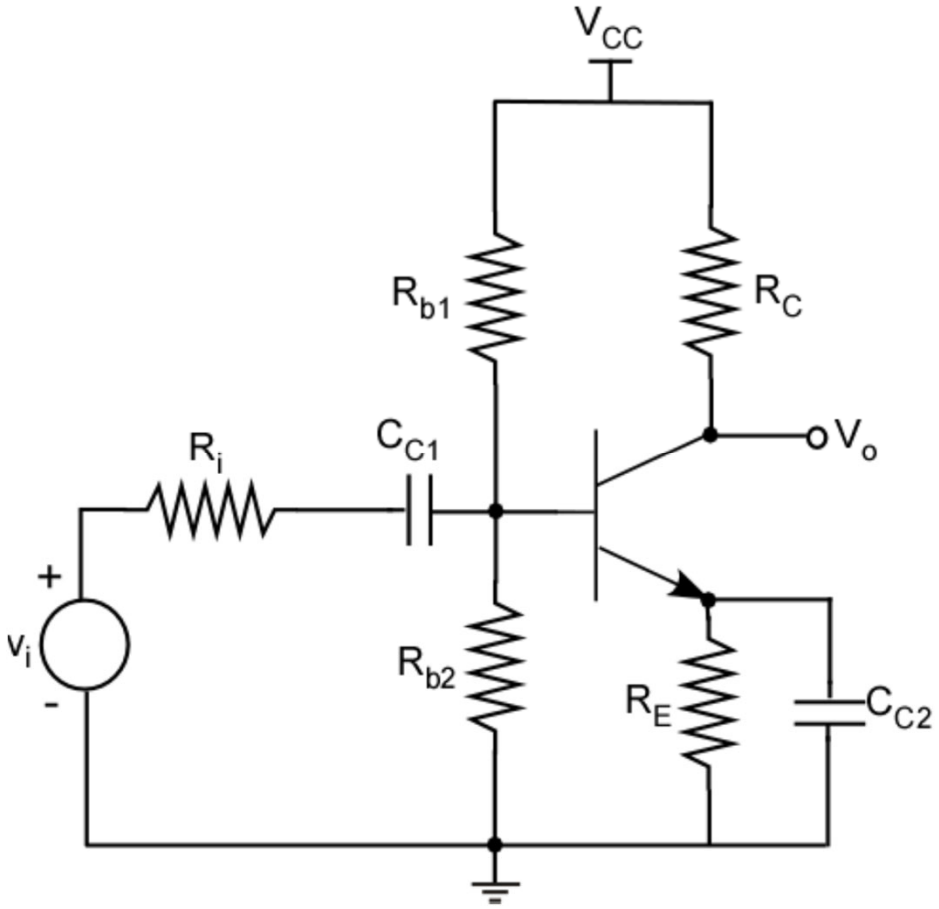
If G_g is negligible

$$f_H \simeq \frac{1}{2\pi\left\{R_i\left[C_{gs}+C_{gd}\left(1+g_m R_D^{'}\right)\right]+C_{gd}R_D^{'}\right\}}$$

If R_i =0

$$f_H \simeq \frac{1}{2\pi C_{gd}R_D^{'}}$$

BJT-CE – Miller Effect – Exact Analysis

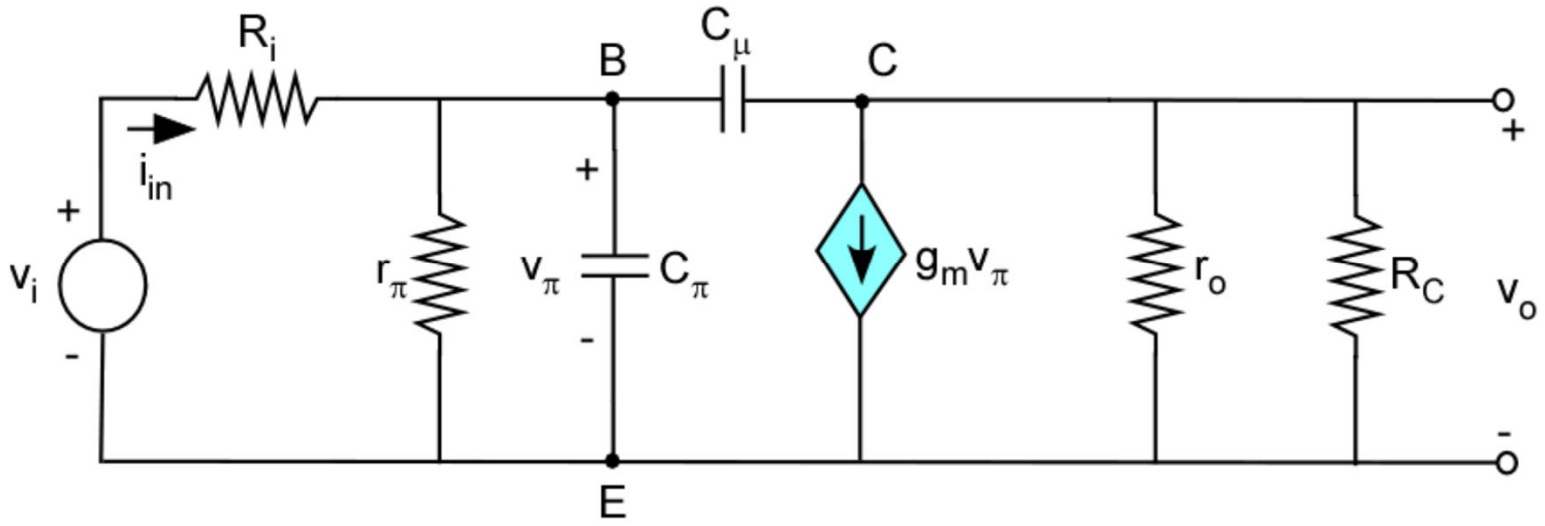


$$G_i = \frac{1}{R_i} \qquad G_C = \frac{1}{R_C}$$

$$g_\pi = \frac{1}{r_\pi} \qquad g_o = \frac{1}{r_o}$$

$$R_C' = R_C \,//\, r_o = \frac{1}{G_C + g_o}$$

BJT-CE – Miller Effect – Exact Analysis



$$\frac{v_o}{v_i} = -\frac{G_s R_C' \left(g_m - sC_\mu \right)}{G_i + g_\pi + s\left[C_\pi + C_\mu \right] + sC_\mu R_C' \left[G_i + g_\pi \right] + sC_\mu g_m R_C' + s^2 C_\mu C_\pi R_C'}$$

BJT-CE – Miller Effect – Exact Analysis

We neglect the terms in s^2 since

$$\left|s^2 C_\mu C_\pi R_C'\right| \ll \left|sC_\mu g_m R_C'\right| \quad or \left|sC_\pi\right| \ll \left|g_m\right|$$

$$\frac{v_o}{v_i} = -\frac{G_i R_C'\left(g_m - sC_\mu\right)}{G_i + g_\pi + s\left[C_\pi + C_\mu\left(1 + g_m R_C'\right) + C_\mu R_C'\left(G_i + g_\pi\right)\right]}$$

If we multiply through by $R_i = \frac{1}{G_i}$

$$\frac{v_o}{v_i} = -\frac{R_C'\left(g_m - sC_\mu\right)}{1 + R_i g_\pi + s\left\{R_i\left[C_\pi + C_\mu\left(1 + g_m R_D'\right)\right] + C_\mu R_C'\left(1 + R_i g_\pi\right)\right\}}$$

BJT-CE – Miller Effect – Exact Analysis

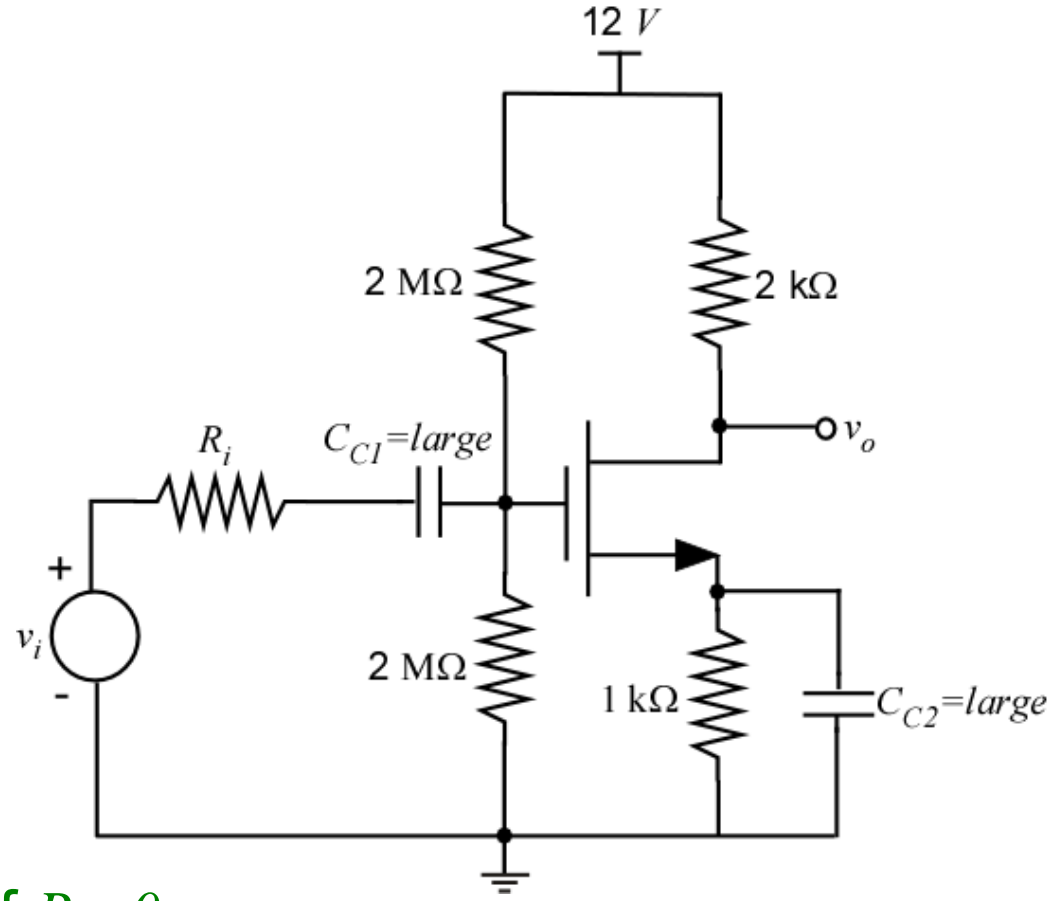
$$f_H = \frac{1 + R_i g_\pi}{2\pi \left\{ R_i \left[C_\pi + C_\mu \left(1 + g_m R_C' \right) \right] + C_\mu R_C' \left(1 + R_i g_\pi \right) \right\}}$$

If $R_i = 0$

$$f_H \simeq \frac{1}{2\pi C_\mu R_C'}$$

Example

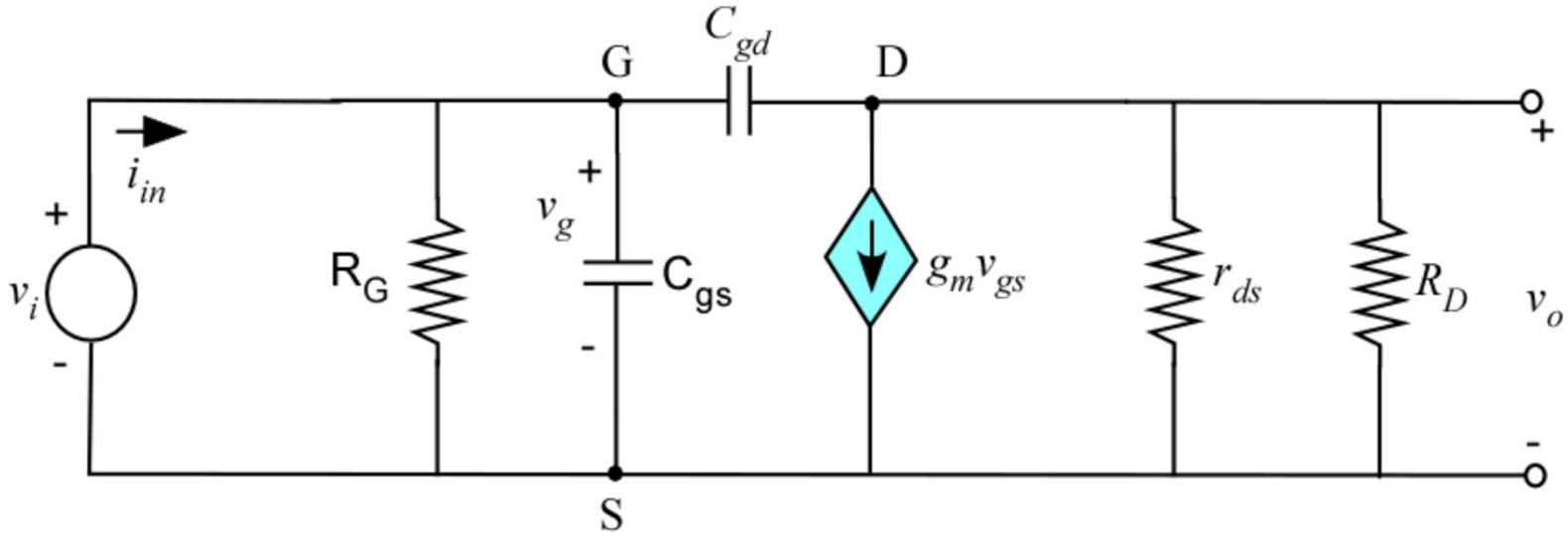
For the discrete common-source MOSFET amplifier shown, the transistor has V_T = 1V, $mC_{ox}(W/L)$ = 0.25 mA/V^2, I = 0, C_{gs} = 3 pF, C_{gd} = 2.7 pF and V_A = 20 V. Assume that the coupling capacitors are short circuits at midband and high frequencies.



(a)Find the 3dB bandwidth if R_i=0

(b) Find the 3dB bandwidth if R_i= 100 Ω

Example – Part (a)



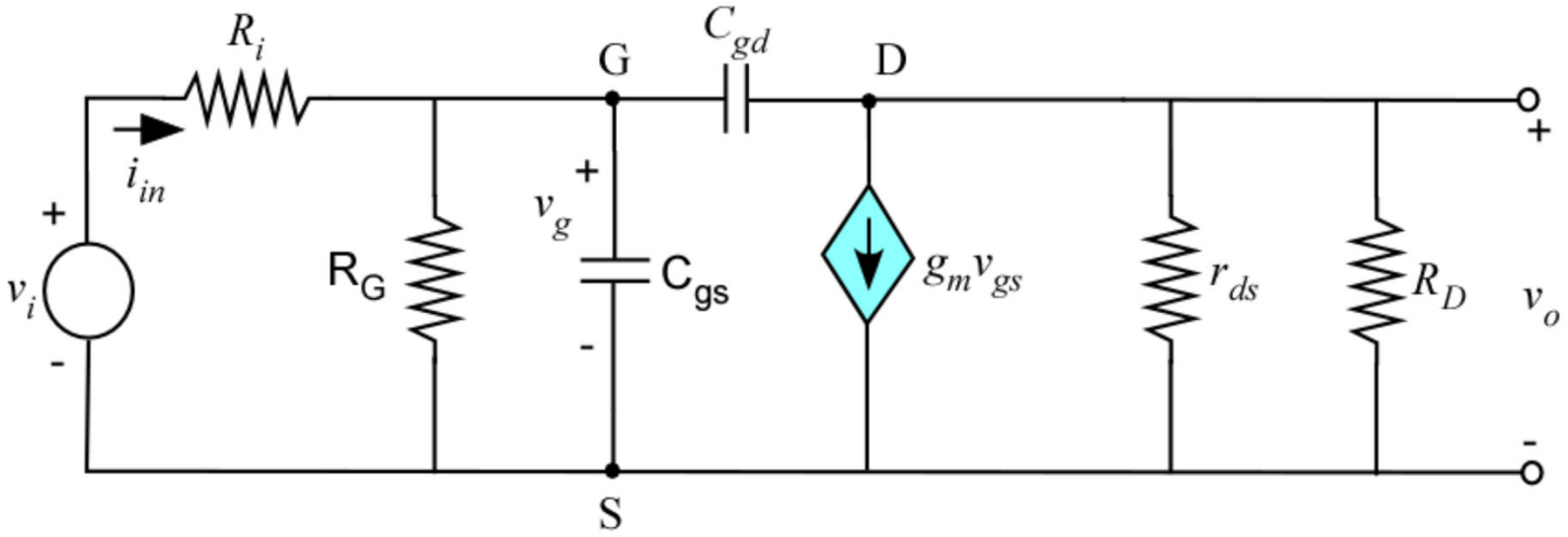
If R_i =0,

$$f_{3dB} = \frac{1}{2\pi C_{gd} R_D'} \qquad r_{ds} = \frac{|V_A|}{I_D} = \frac{20}{1.516} = 13\ k\Omega$$

$$R_D' = R_D \,||\, r_{ds} = 13 \,||\, 2 = 1.736\ k\Omega$$

$$f_{3dB} = \frac{1}{2\pi 2.7\times10^{-12}\times1.736\times10^{3}} = 33.95\ MHz$$

Example Part (b)



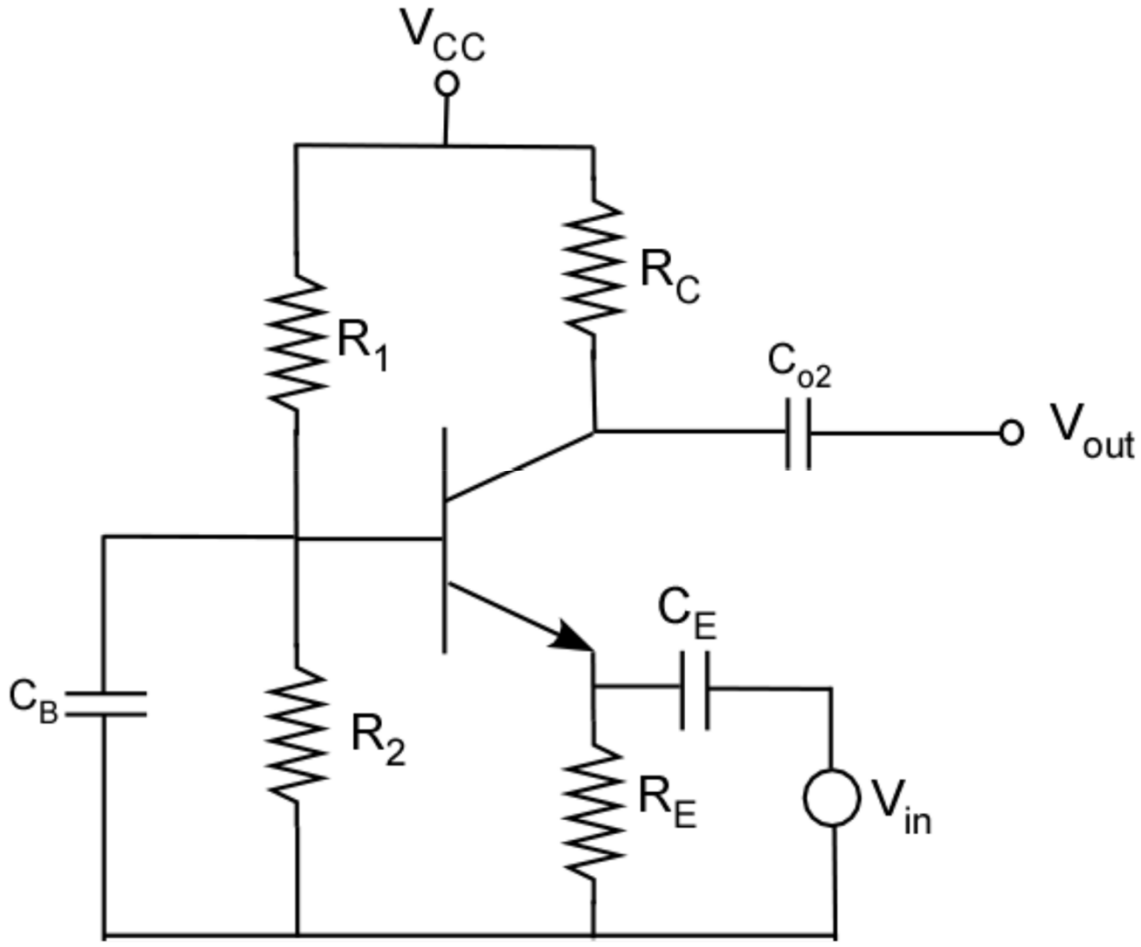
If R_i =100 Ω,

$$g_m R_D' = 0.870 \times 1.736 = 1.51$$

$$f_H \simeq \frac{1}{2\pi\left\{R_i\left[C_{gs} + C_{gd}\left(1 + g_m R_D'\right)\right] + C_{gd} R_D'\right\}}$$

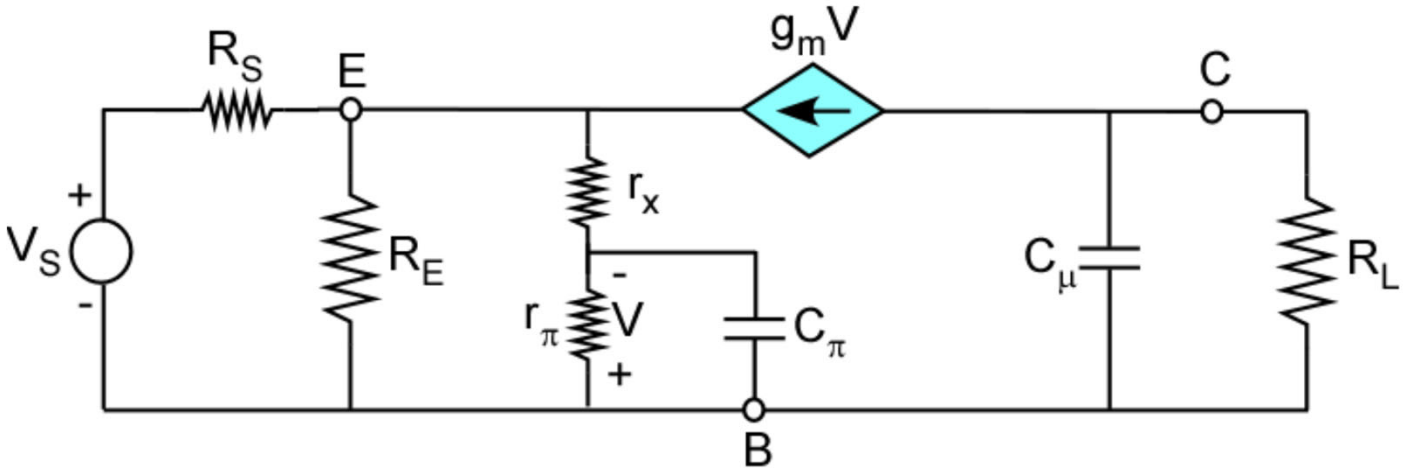
$$f_H \simeq \frac{1}{2\pi\left\{0.1\left[3 + 2.7\left(1 + 1.51\right)\right] + 2.7 \times 1.736\right\}} = 28\ MHz$$

Common Base (CB) Amplifier



High-Frequency Analysis of CB Amplifier

Exact analysis is too tedious ➔ approximate



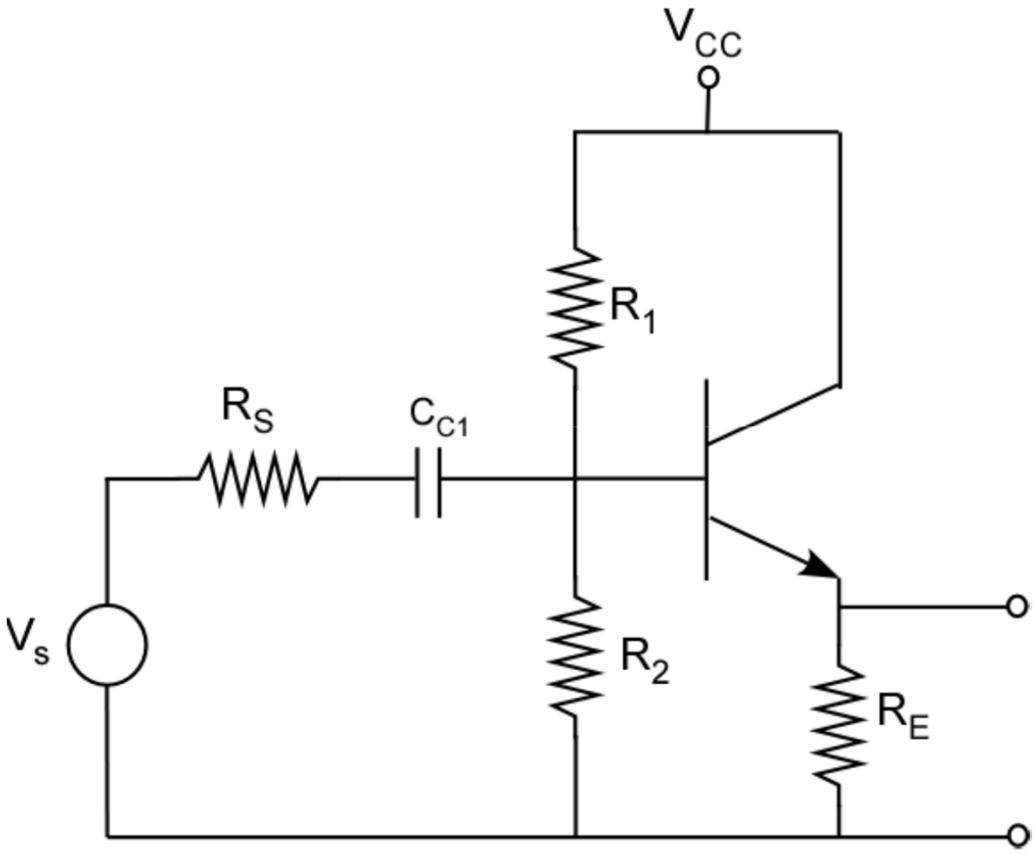
From current gain analysis

$$\omega_{in-3dB} = \frac{1}{C_\pi \left[R_S \,//\, R_E + \frac{r_x}{1+\beta} \right] // \left[\frac{r_\pi}{1+\beta} \right]}$$

$$\omega_{out-3dB} = \frac{1}{C_\mu R_L}$$

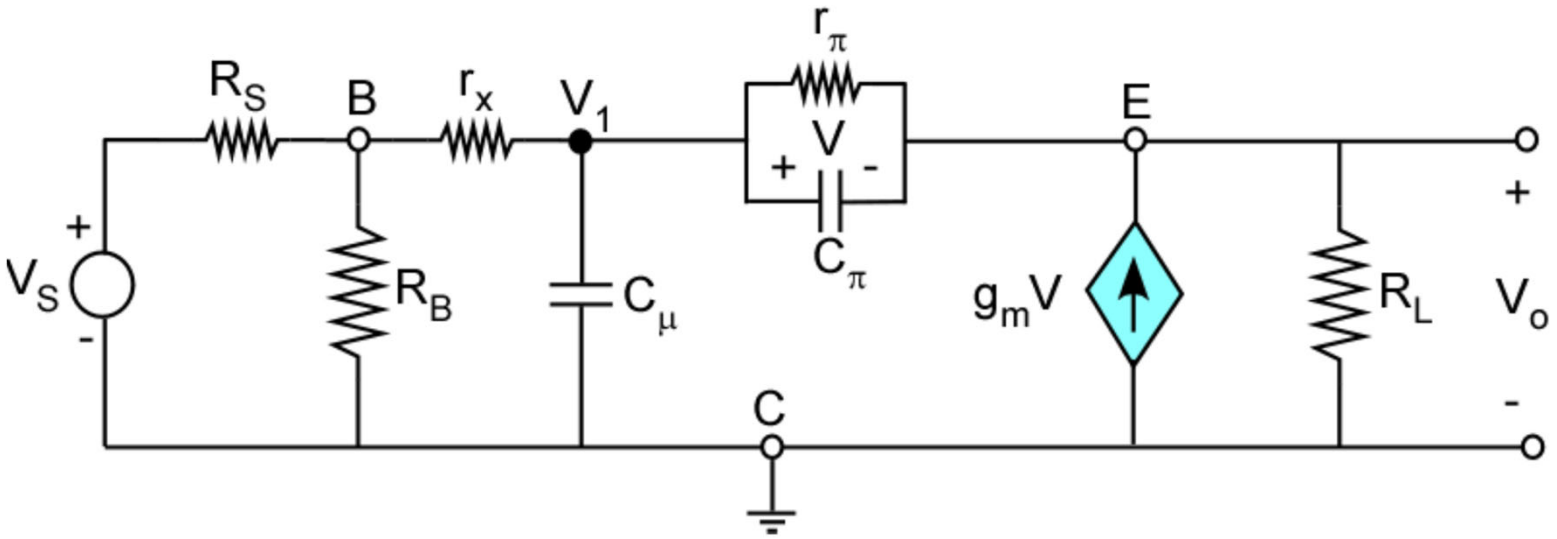
The amplifier's upper cutoff frequency will be the lower of these two poles.

Emitter Follower



Emitter Follower High-Frequency

Exact analysis is too tedious ➔ approximate



$$A_v'(s) = \frac{g_m R_L}{1 + g_m R_L} \frac{1 + \dfrac{sC_\pi}{g_m}}{1 + \dfrac{sC_\pi R_E}{(1 + g_m R_E)}}$$

$$\omega_{3dB} = \frac{1 + g_m R_E}{R_E C_\pi} \simeq \frac{g_m}{C_\pi + C_\mu} = \omega_T$$

Bandwidth of Multistage Amplifier

- The time constant τ_{io} is the product of the capacitance and the resistance seen across its terminals with:
  - All other internal capacitors open circuited
  - All independent voltage sources short circuited
  - All independent current sources opened

- The upper 3dB frequency point ω_{3dB} is then found by using :

$$\omega_{3dB} = \frac{1}{\sum \tau_{io}}$$

Open-Circuit Time Constant Method

- The time constant of each capacitor in the circuit is evaluated. It is the product of the capacitance and the resistance seen across its terminals with:
  - All other internal capacitors open circuited
  - All independent voltage sources short circuited
  - All independent current sources opened

- The value of b_1 is computed by summing the individual time constants

$$b_1 = \sum_{i=1}^{n} C_i R_{io}$$

Open-Circuit Time Constant Method

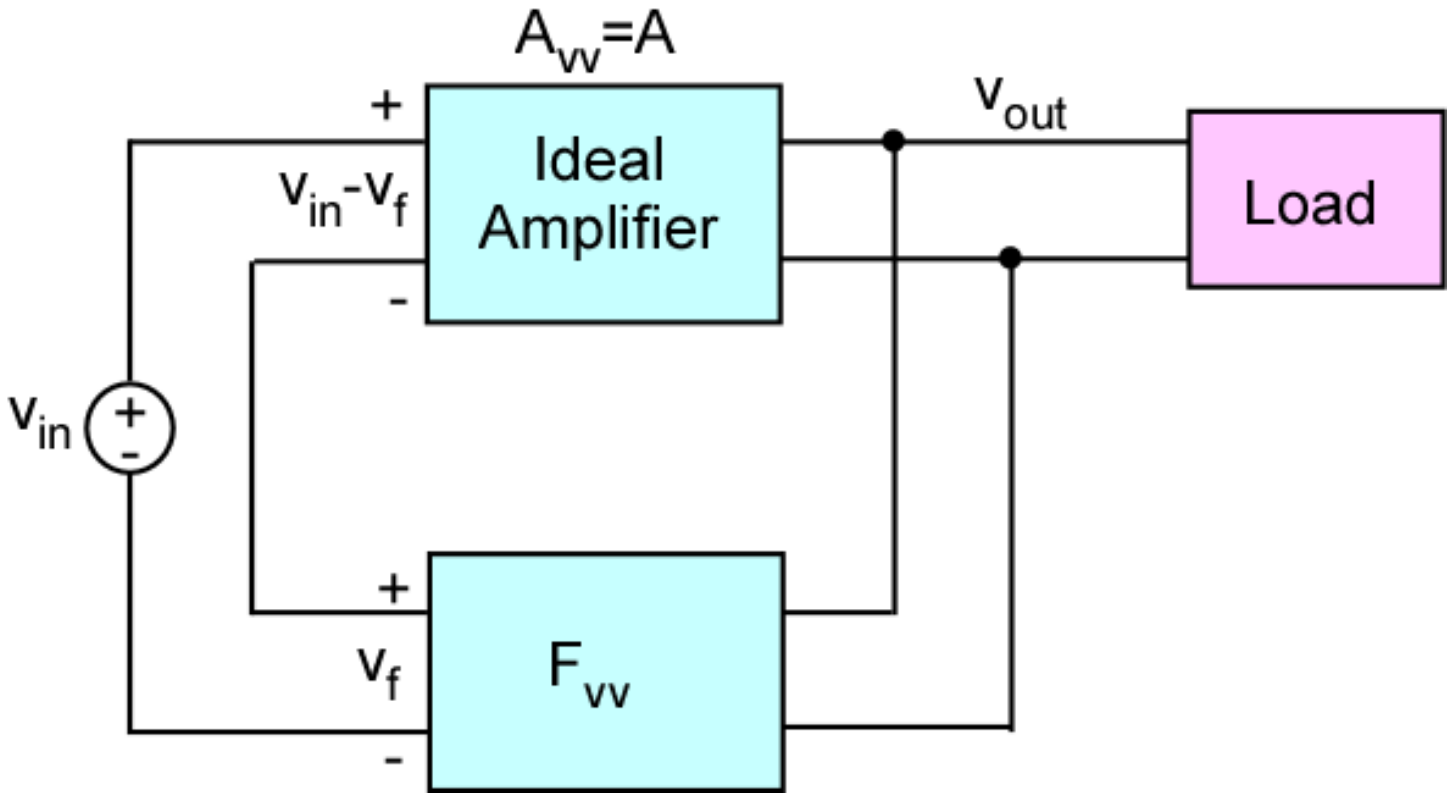
- An approximation can be made by using the value of b_1 to determine the 3dB upper frequency point ω_H
- If the zeros are not dominant and if one of the poles P1 is dominant, then

$$b_1 \simeq \frac{1}{\omega_{P1}}$$

Assuming that the 3-dB frequency will be approximately equal to ω_{P1}

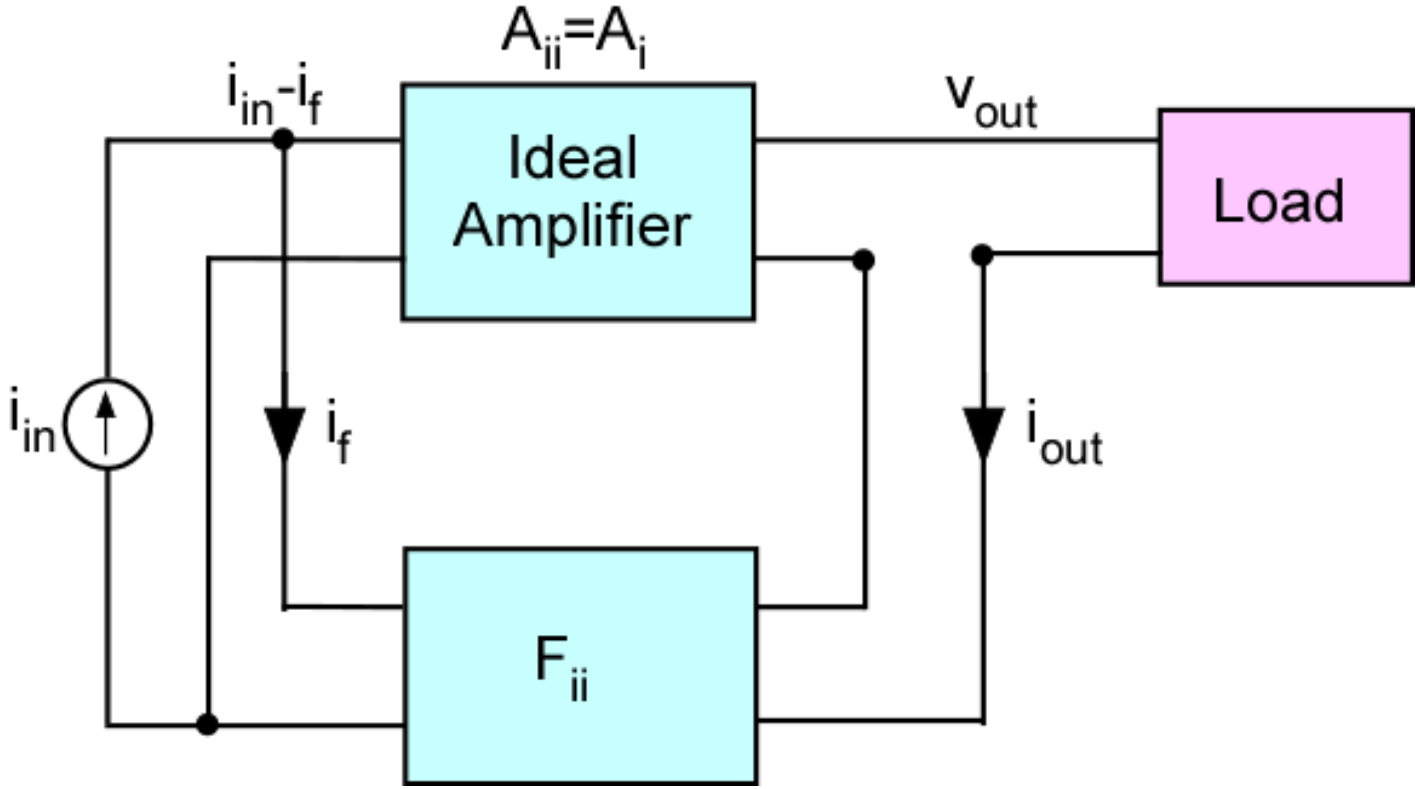
$$\omega_H \approx \frac{1}{b_1} = \frac{1}{\sum_i C_i R_{io}}$$

Series-Shunt Feedback



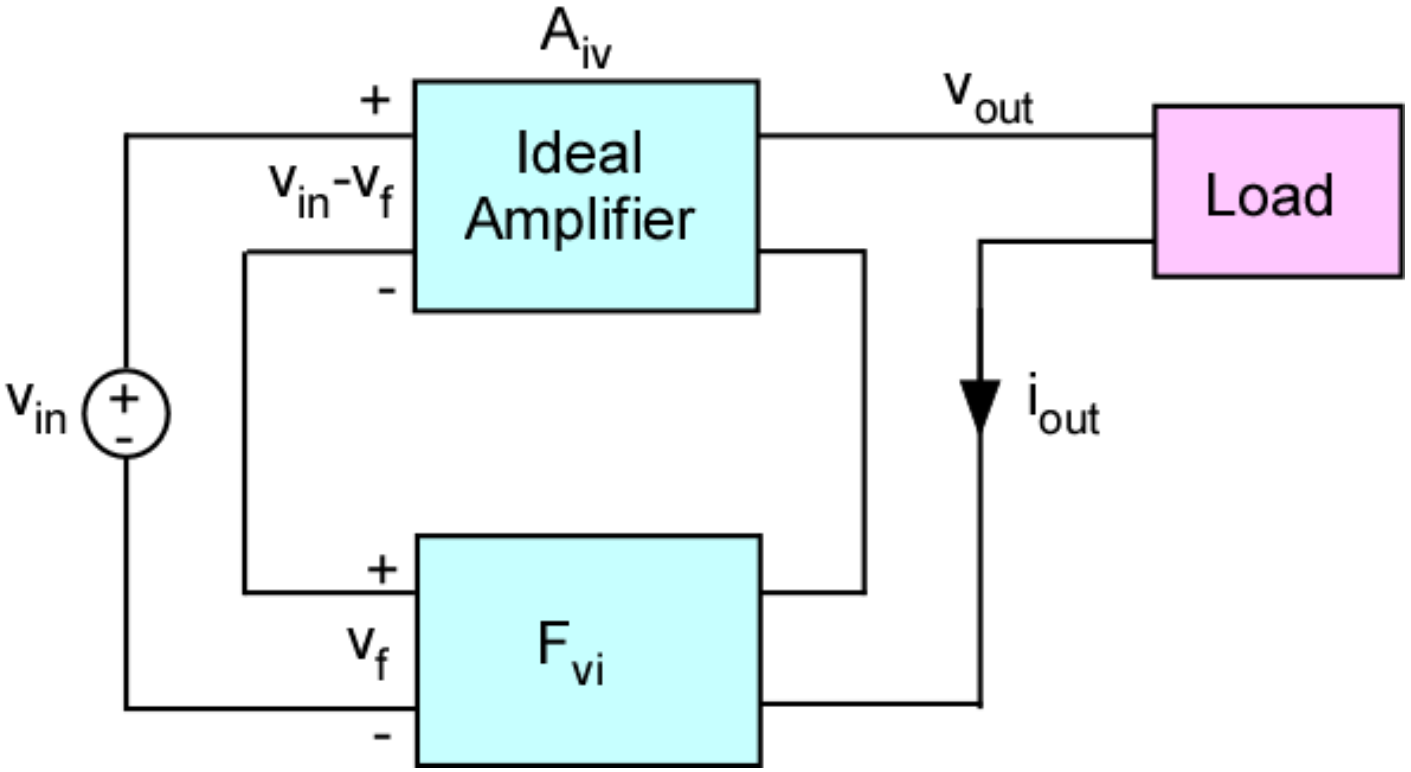
Voltage mixing-voltage sampling feedback

Shunt- Series Feedback



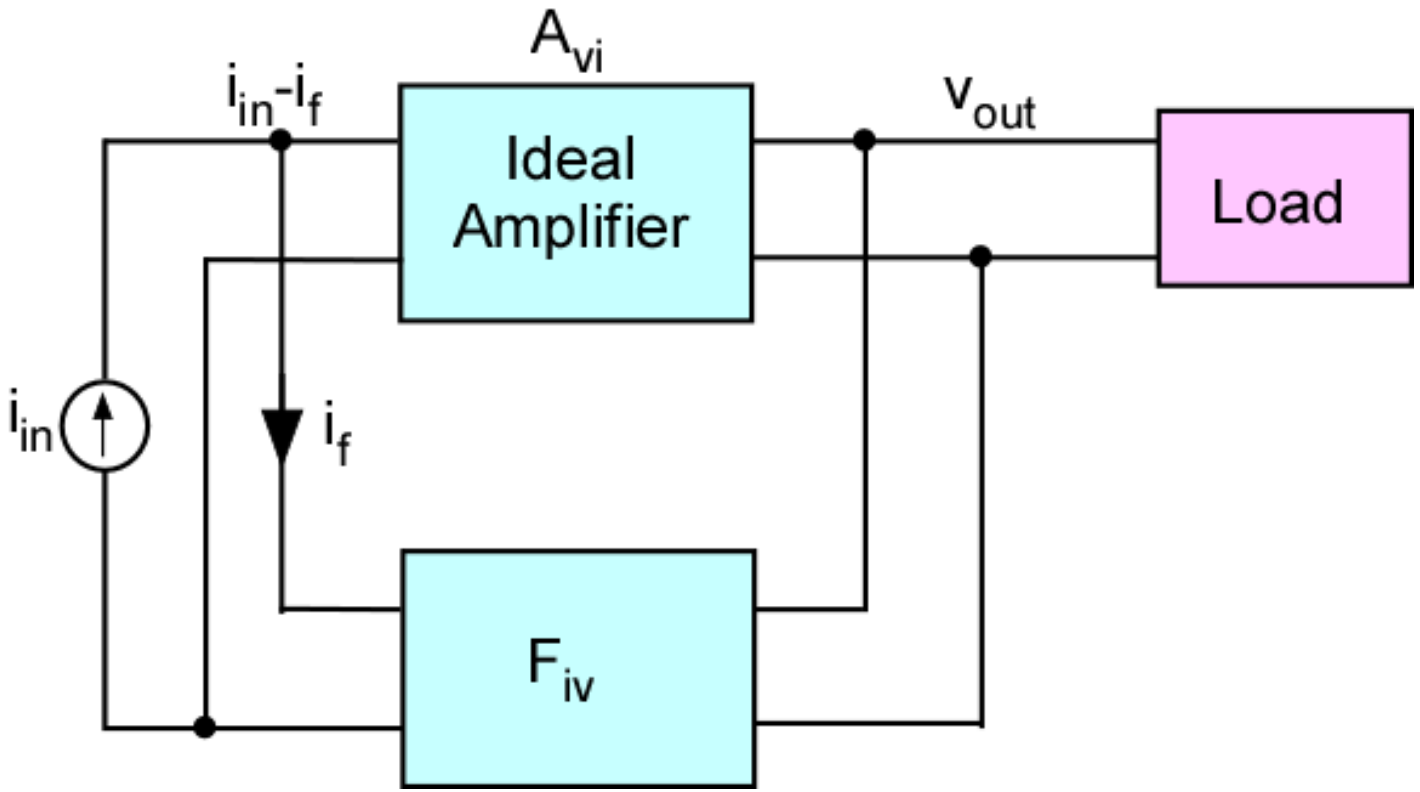
Current mixing-current sampling feedback

Series-Series Feedback



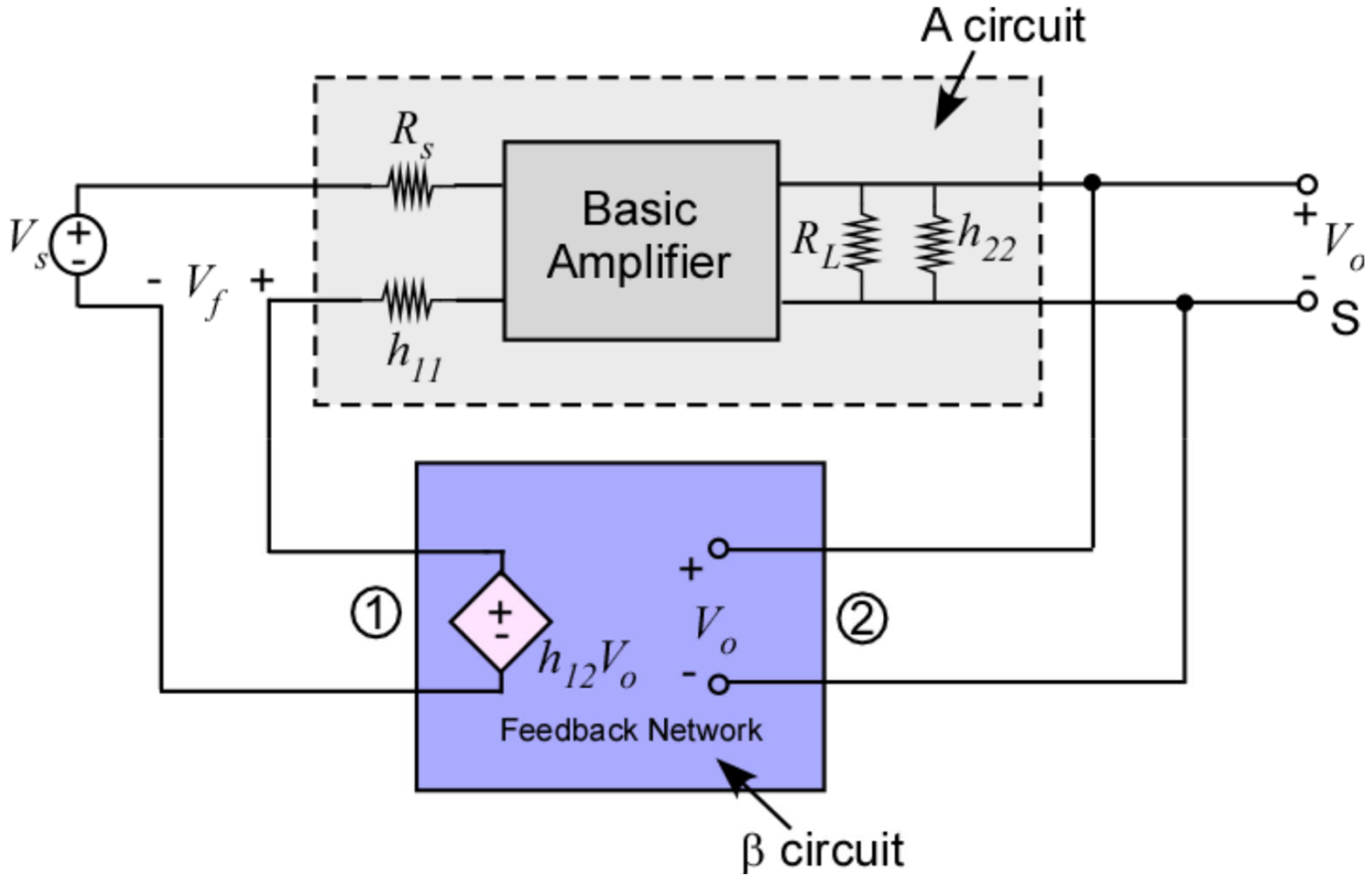
Voltage mixing-current sampling feedback

Shunt-Shunt Feedback



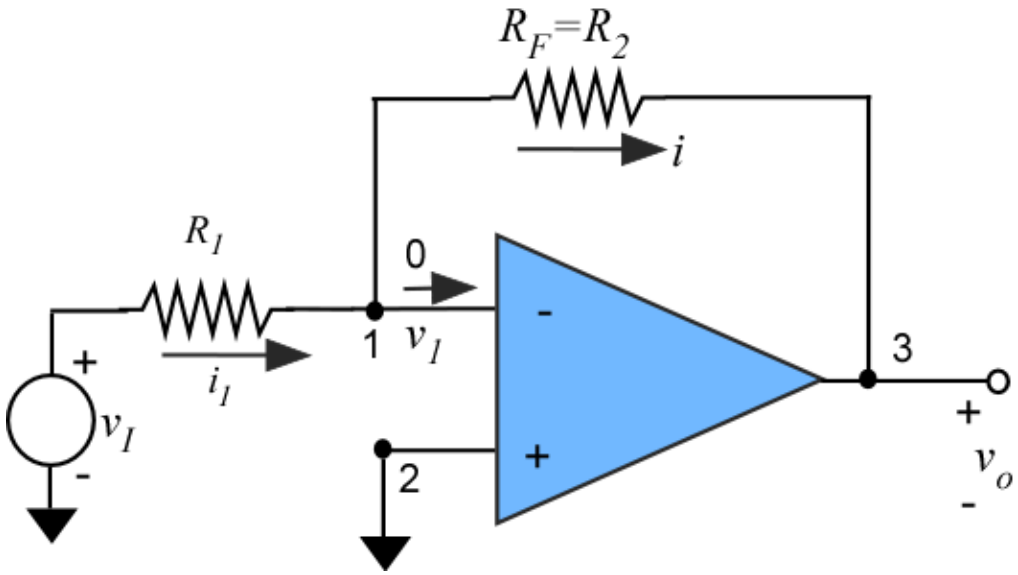
Current mixing-voltage sampling feedback

Series-Shunt Feedback : h-Parameters



$$|h_{12}|_{\substack{basic\\amplifier}} \ll |h_{12}|_{\substack{feedback\\network}} \qquad |h_{21}|_{\substack{feedback\\network}} \ll |h_{21}|_{\substack{basic\\amplifier}}$$

Inverting Configuration



Terminal 2 is tied to ground

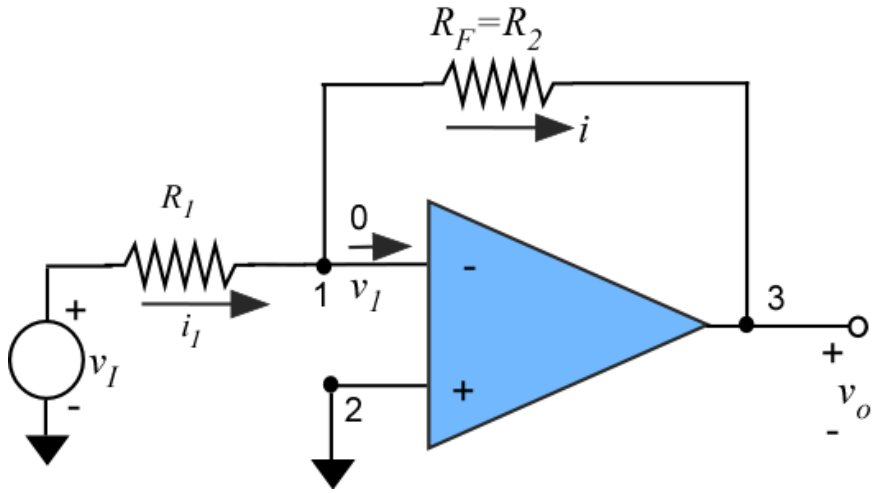
We introduce R_F (or R_2) to reduce gain (from inf)

- **When R_F is connected to terminal 1, we talk about negative feedback. If R_F is tied to terminal 2, we have positive feedback**

Inverting Configuration

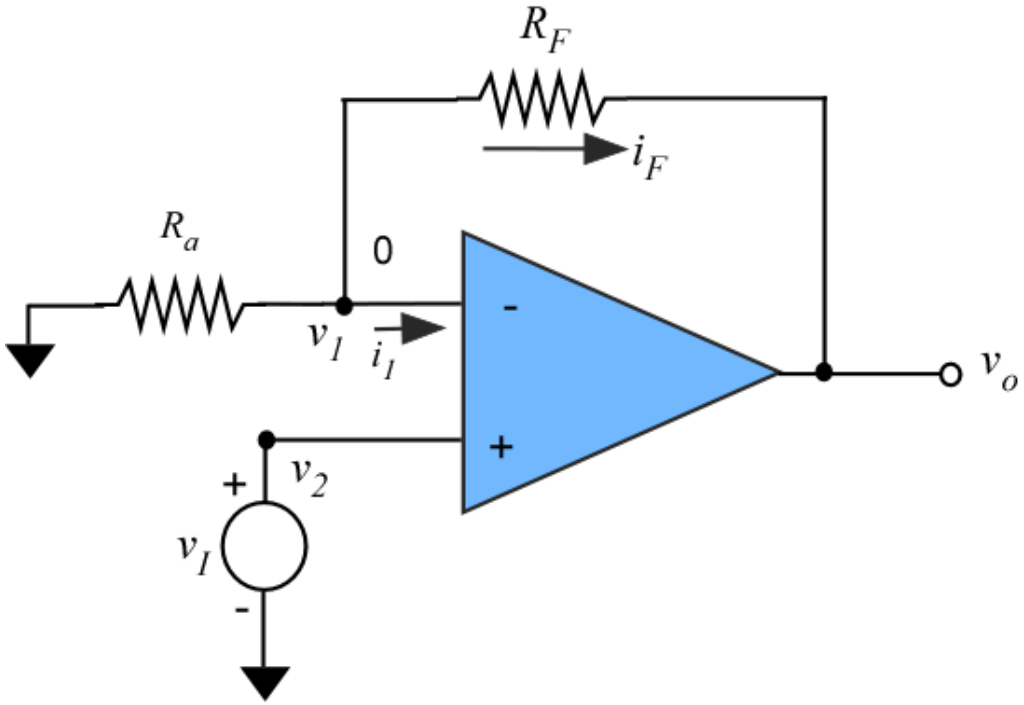
Closed-Loop gain

$$\frac{v_o}{v_I} = -\frac{R_F}{R_1} = G$$



Observe that the closed-loop gain is the ratio of external components ➔ we can make the closed-loop as accurate as we want. Gain is smaller but more accurate.

Non-Inverting Configuration



Assume gain is $\infty \Rightarrow v_{ID} = \frac{v_o}{A} \rightarrow 0$

Non-Inverting Configuration

Virtual short $\Rightarrow v_2 = v_I = v_1$

$$v_I \frac{\left(R_a + R_F\right)}{R_a} = v_o$$

$$G = \frac{v_o}{v_I} = 1 + \frac{R_F}{R_a}$$

$$\boxed{G = 1 + \frac{R_F}{R_a}}$$

Frequency Response – Non-Inverting

$$A_{ni}(f) = \frac{A_{MBni}}{1 + jf / f_{2ni}}$$

$$GBW_{ni} = A_{MBni} f_{2ni} = \frac{A_{MBoa}}{1 + A_{MBoa} F} \cdot f_{2oa} \left(1 + A_{MBoa} F\right)$$

$$GBW_{ni} = A_{MBni} f_{2ni} = A_{MBoa} f_{2oa} = GBW_{oa}$$

Gain-Bandwidth product is constant

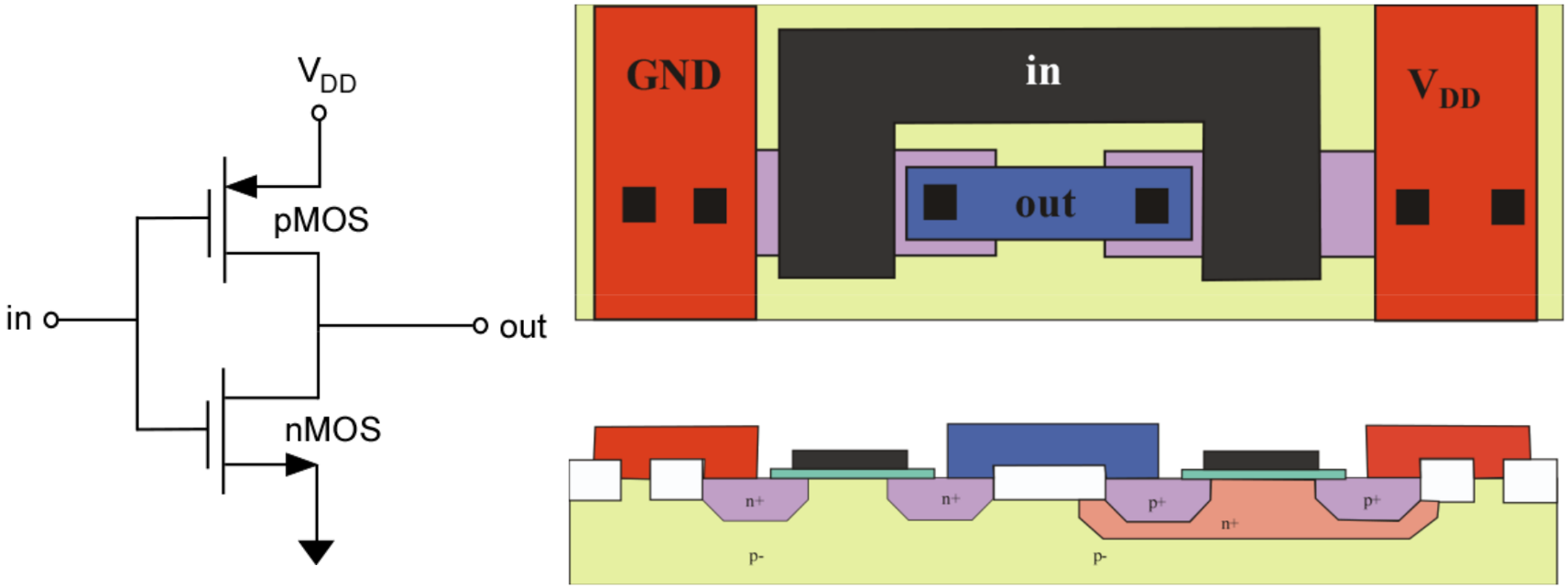
Frequency Response – Non-Inverting

Midband voltage gain is reduced from A_{MBoa} to A_{MBni}

The upper 3-dB frequency will be greater than that of the op amp by the same factor of gain reduction.

If the low-frequency gain of the op amp is A_{MBoa}= 200,000 and with resistors A_{MBni} = 40, the gain is reduced by a factor of 5,000. If the basic 3-db frequency is 5 Hz, the noninverting 3dB frequency will be 25 kHz.

Complementary MOS



- **CMOS Characteristics**
  - Combine nMOS and pMOS transistors
  - pMOS size is larger for electrical symmetry

Voltage Transfer Characteristics (VTC)

The static operation of a logic circuit is determined by its VTC

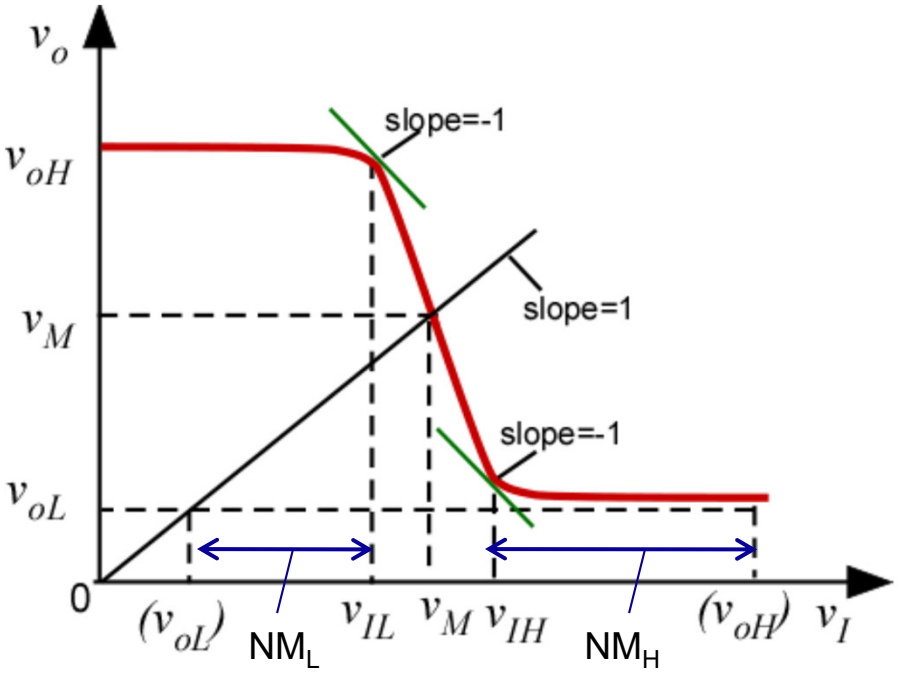
- **In low state: noise margin is *NM_L***

$$NM_L = V_{IL} - V_{OL}$$

- **In high state: noise margin is *NM_H***

$$NM_H = V_{OH} - V_{IH}$$

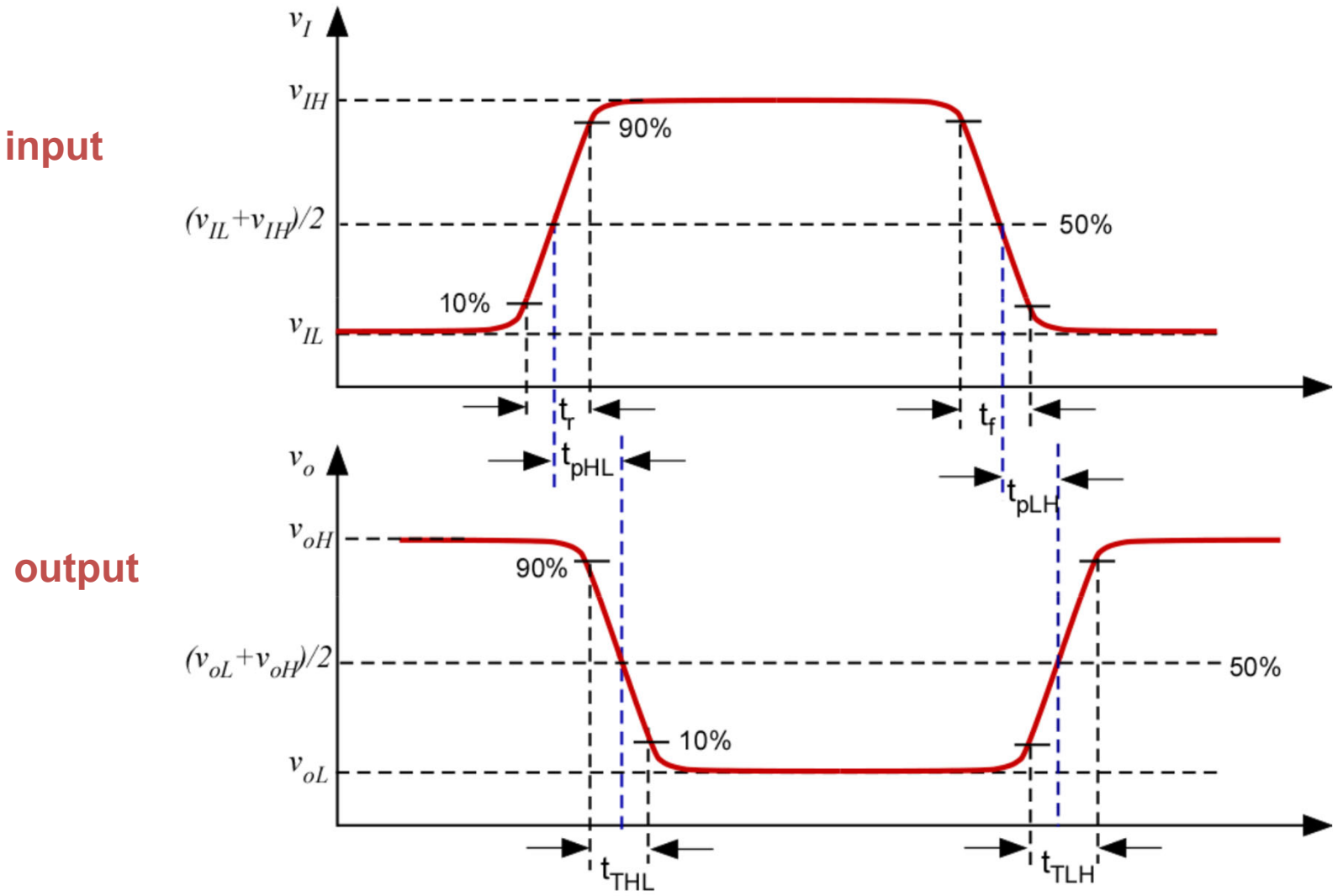
- **An ideal VTC will maximize noise margins**



V_{IL} and V_{IH} are the points where the slope of the VTC=-1

Optimum: $NM_L = NM_H = V_{DD}/2$

Switching Time & Propagation Delay



Switching Time & Propagation Delay

t_r=rise time (from 10% to 90%)
t_f=fall time (from 90% to 10%)
t_{pLH}=low-to-high propagation delay
t_{pHL}=high-to-low propagation delay

Inverter propagation delay:

$$t_p = \frac{1}{2}\left(t_{pLH} + t_{pHL}\right)$$

CMOS Noise Margins

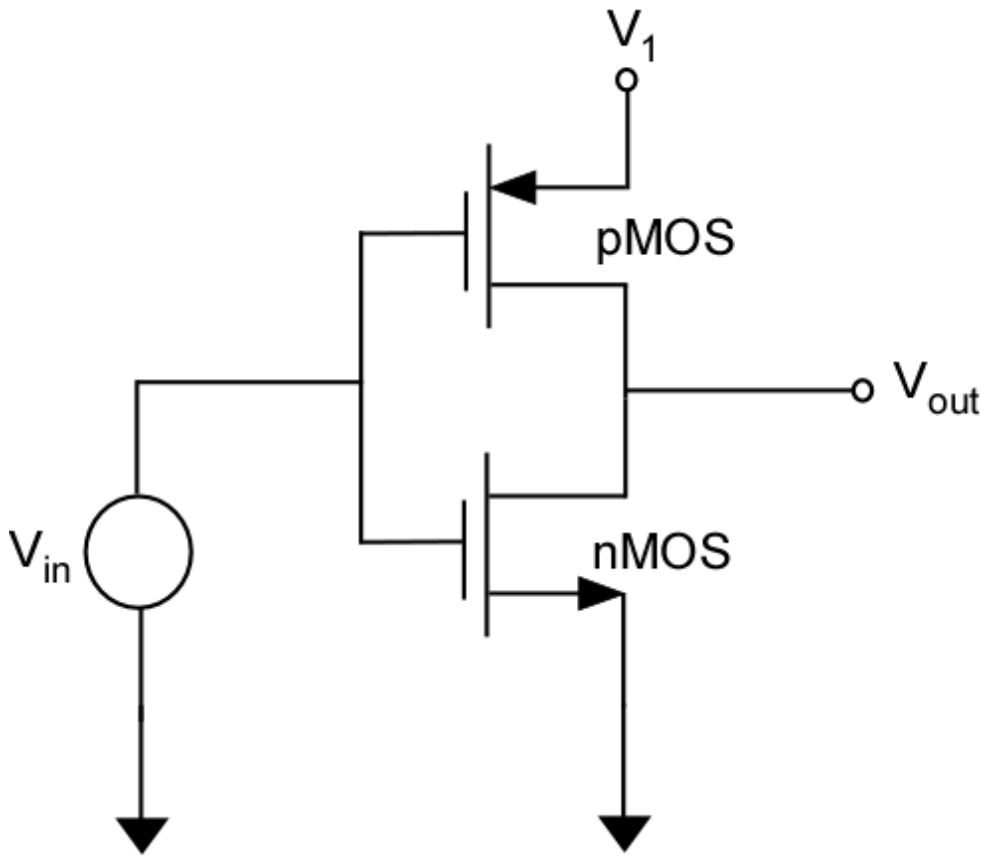
When inverter threshold is at $V_{DD}/2$, the noise margin NM_H and NM_L are equalized

$$NM_H = NM_L = \frac{3}{8}\left(V_{DD} + \frac{2}{3}V_{th}\right)$$

NM_H: noise margin for high input
NM_L: noise margin for low input
V_{th}: threshold voltage

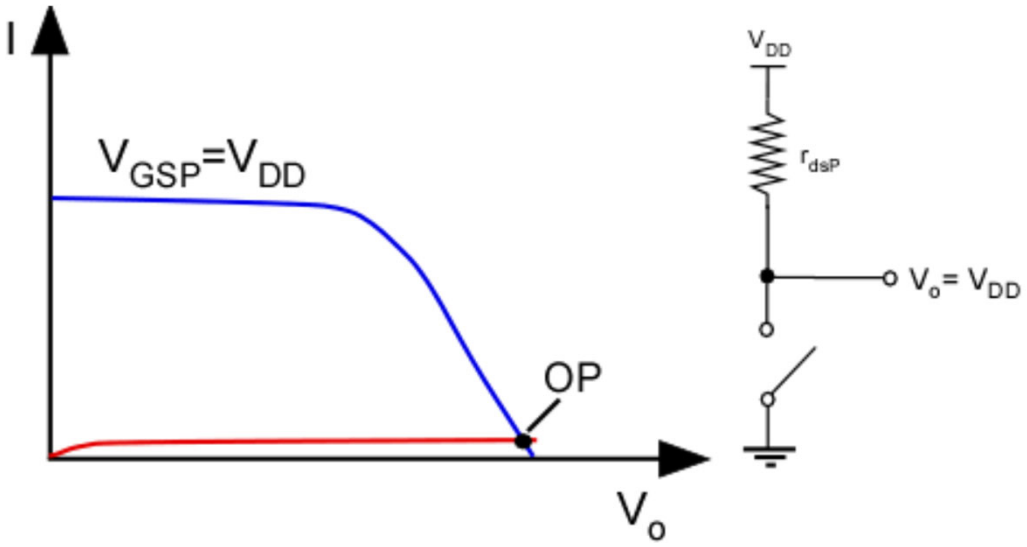
Noise margins are typically around 0.4 V_{DD}; close to half power-supply voltage ➔ CMOS ideal from noise-immunity standpoint

CMOS Switch



CMOS switch is called an inverter

CMOS Switch – Input Low



NMOS

$$V_{GSN} < V_{TN} \Rightarrow OFF$$

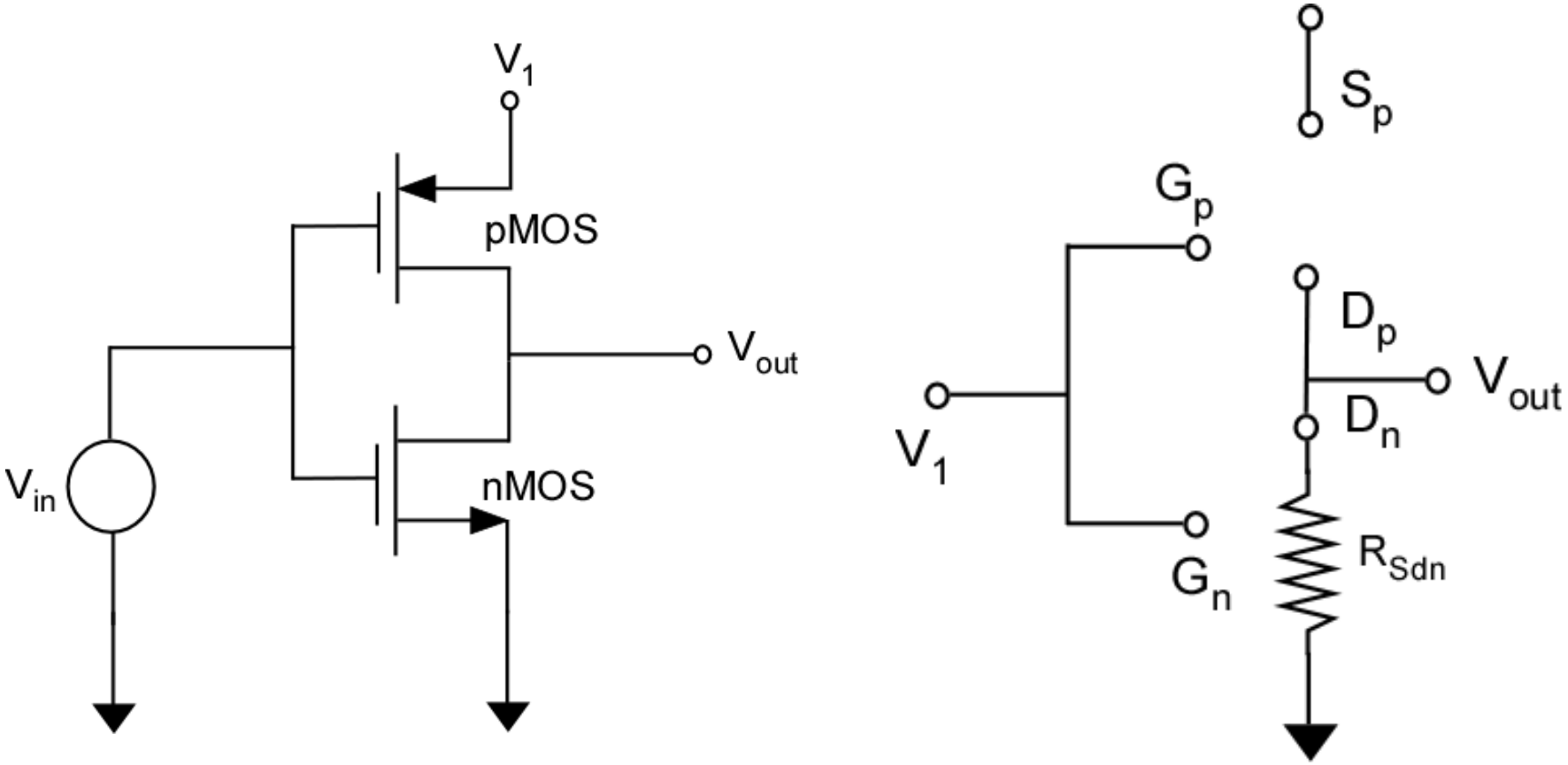
r_{dsn} high

PMOS

$$r_{dsp} = \frac{1}{k_p' \left(\frac{W}{L}\right)_p \left(V_{DD} - |V_{TP}|\right)}$$

r_{dsp} is low

CMOS Switch – On State



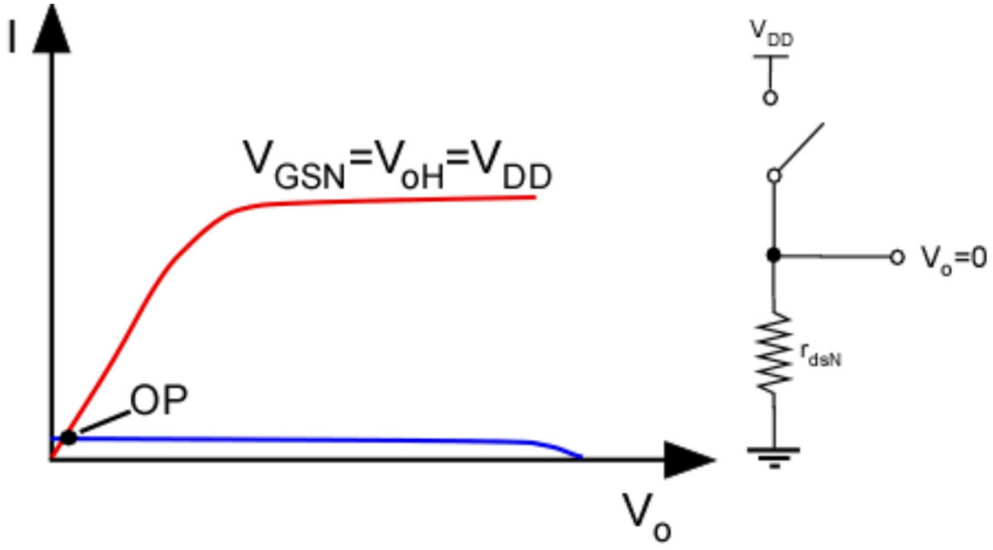
- **ON State (V_{in}: high)**
  - pMOS transistor is off
  - Path from V_{out} to ground is through nMOS ➔V_{out}: low

CMOS Switch – Input High

NMOS

$$r_{dsn} = \frac{1}{k_n'\left(\frac{W}{L}\right)_n \left(V_{DD} - V_{TN}\right)}$$

r_{dsn} is low



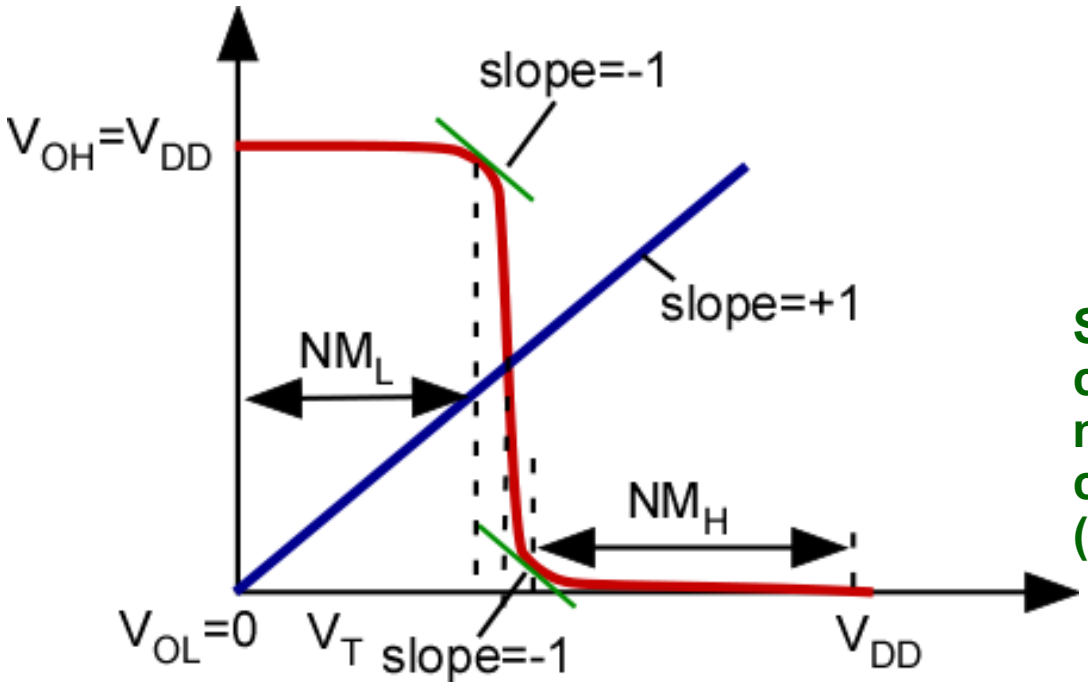
PMOS

$$V_{GSP} > V_{TP} \Rightarrow OFF$$

r_{dsp} high

Matched CMOS Inverter VTC

CMOS inverter can be made to switch at specific threshold voltage by appropriately sizing the transistors



$$\left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_n$$

Symmetrical transfer characteristics is obtained via matching ➔ equal current driving capabilities in both directions (pull-up and pull-down)

Digital Logic - Generalization

De Morgan's Law

$$\overline{A + B + C + \ldots} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \ldots$$

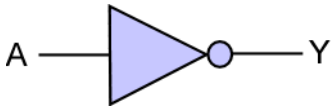
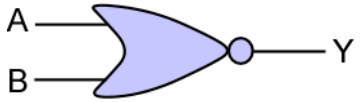
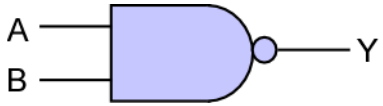
$$\overline{A \cdot B \cdot C \cdot \ldots} = \overline{A} + \overline{B} + \overline{C} + \ldots$$

Distributive Law

$$AB + AC + BC + BD = A(B + C) + B(C + D)$$

- **General Procedure**
  1. Design PDN to satisfy logic function
  2. Construct PUN to be complementary of PDN in every way
  3. Optimize using distributive rule

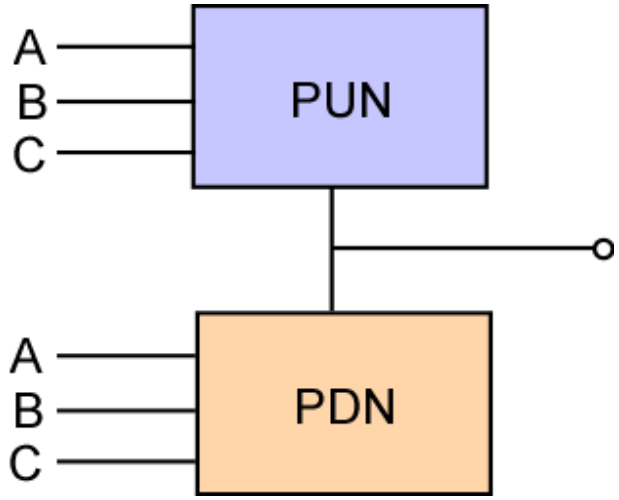
Basic Logic Function

Basic Function	INVERTER	NOR	NAND
Symbol			
# Devices PUN	1 PMOS	2 PMOS-Series	2 PMOS-Parallel
# Devices PDN	1 NMOS	2 NMOS-Parallel	2 NMOS-Series
Truth Table	A Y 0 1 1 0	A B Y 0 0 1 0 1 0 1 0 0 1 1 0	A B Y 0 0 1 0 1 1 1 0 1 1 1 0

Pull-Down and Pull-Up Functions

Pull-up network (PUN)

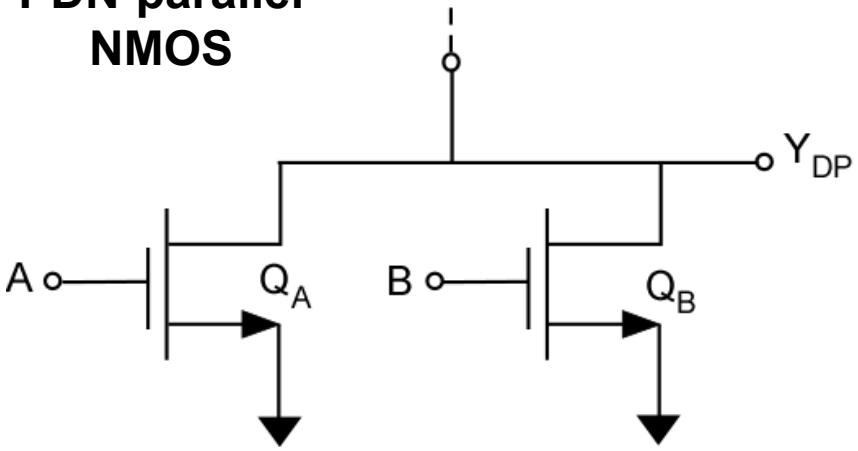
Pull-down network (PDN)



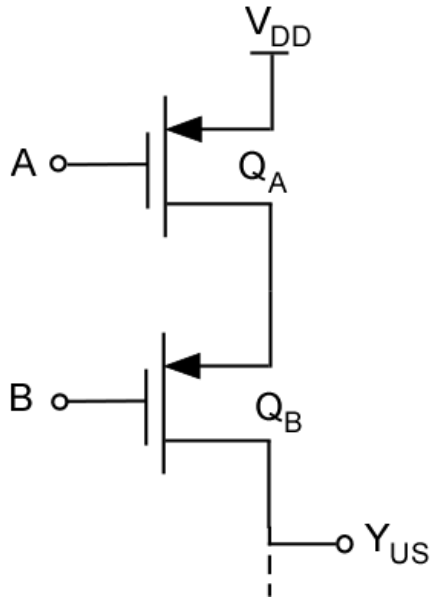
- **Key features**
  - When PDN switch is on, PUN switch is off and vice versa
  - Conditions for being on and off are complementary

Pull-Down and Pull-Up

PDN-parallel NMOS



PUN-series PMOS



$$Y_{DP} = \overline{A + B}$$

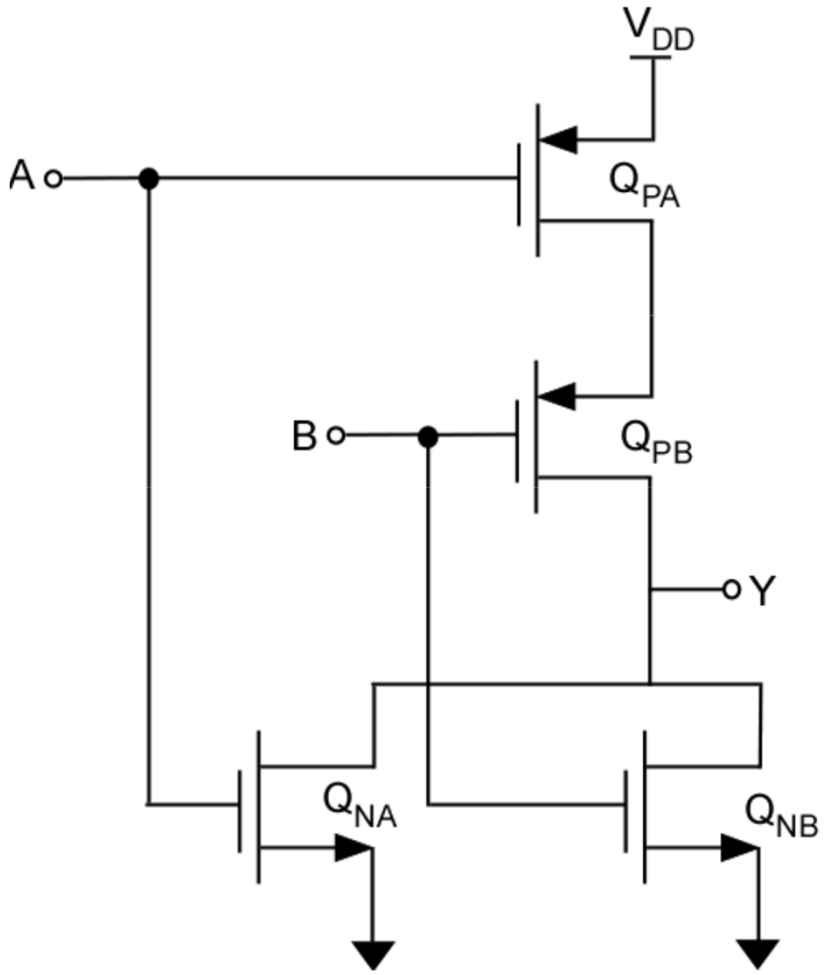
Truth Tables

A	B	Y_{DP}
0	0	1
0	1	0
1	0	0
1	1	0

$$Y_{US} = \overline{A}\,\overline{B}$$

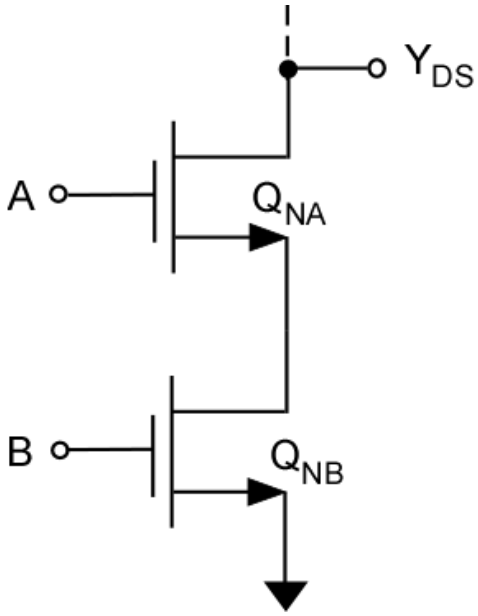
A	B	Y_{US}
0	0	1
0	1	0
1	0	0
1	1	0

Two-Input NOR Gate

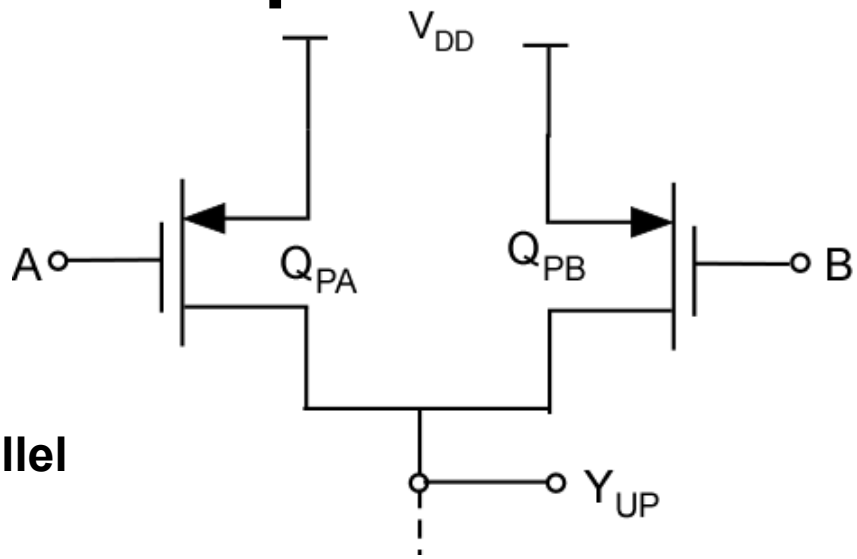


$$Y = \overline{A + B} = \overline{A}\,\overline{B}$$

Pull-Down and Pull-Up



PDN-Series NMOS



PUN-Parallel PMOS

Truth Tables

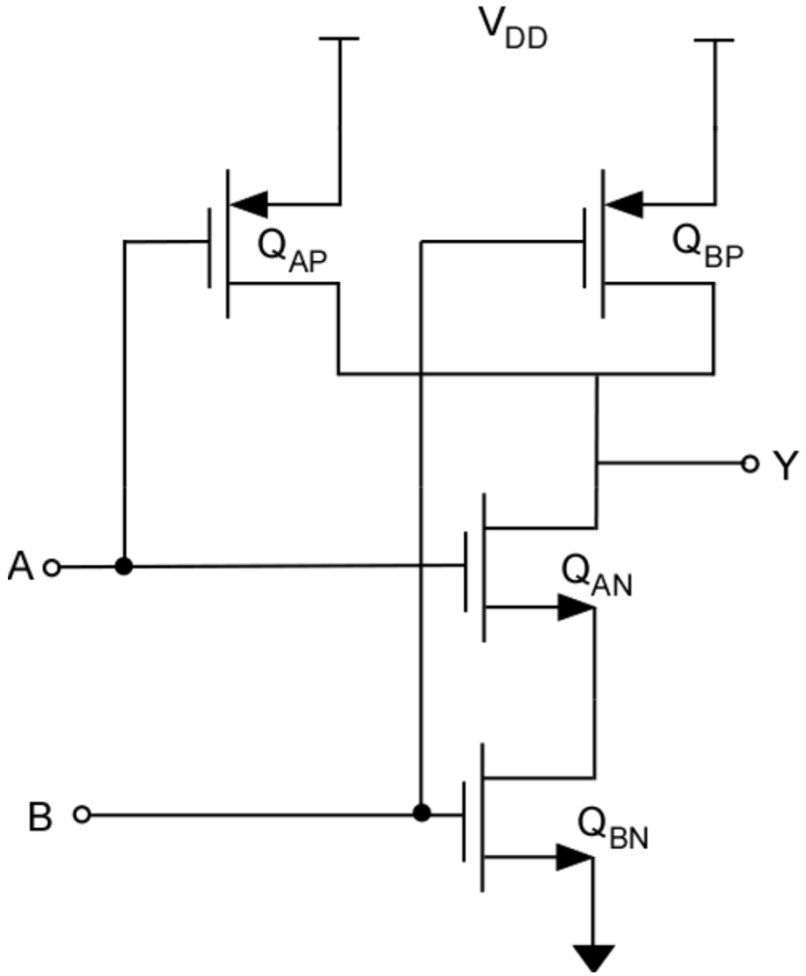
$$Y_{DS} = \overline{AB}$$

	A	B	Y_{DS}
	0	0	1
	0	1	1
	1	0	1
	1	1	0

$$Y_{UP} = \overline{A} + \overline{B}$$

	A	B	Y_{UP}
	0	0	1
	0	1	1
	1	0	1
	1	1	0

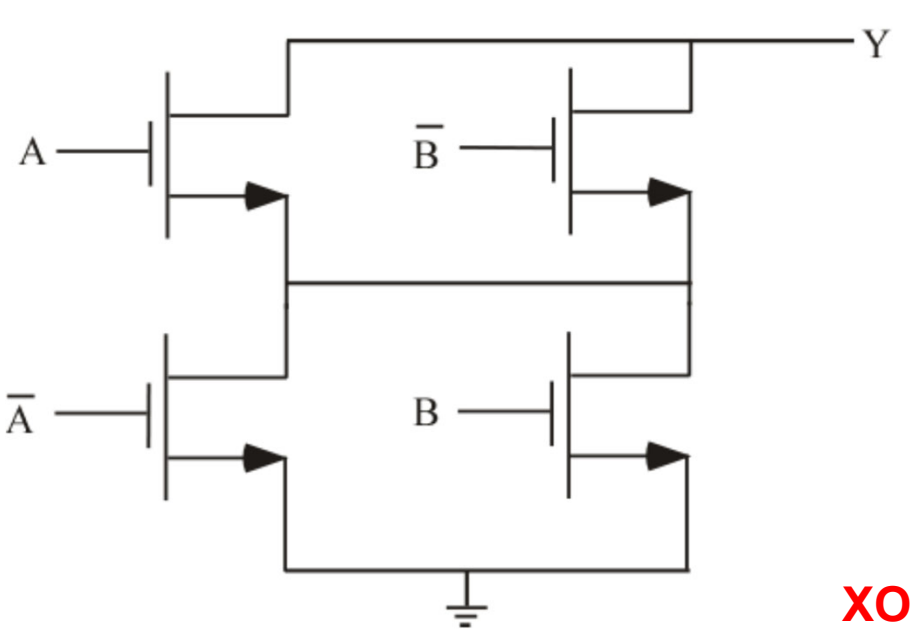
Two-Input NAND Gate

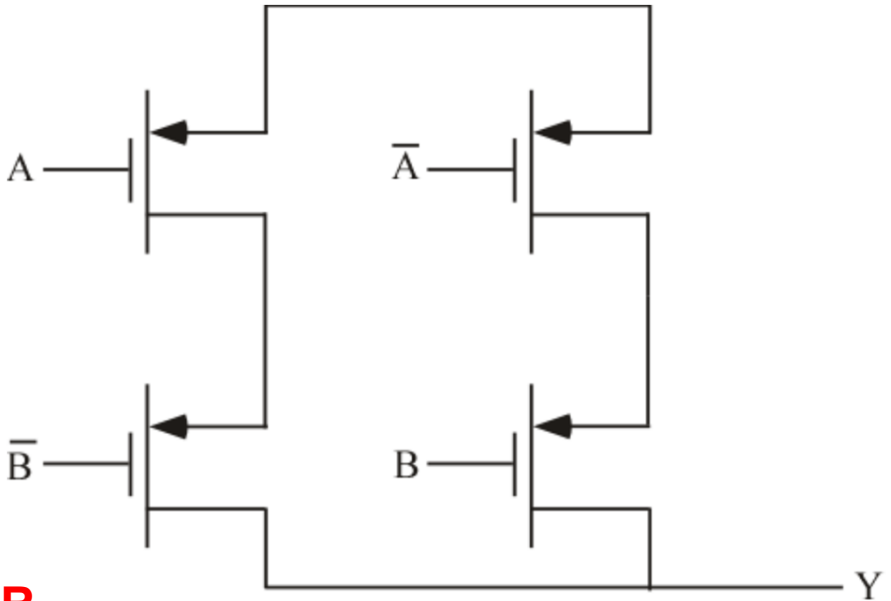


$$Y = \overline{AB} = \overline{A} + \overline{B}$$

Exclusive-OR (XOR) Function

$$Y = A\overline{B} + \overline{A}B \qquad \overline{Y} = (\overline{A} + B)(A + \overline{B})$$





pull down

pull up

XOR

	A	B	Y
	0	0	0
	0	1	1
	1	0	1
	1	1	0