

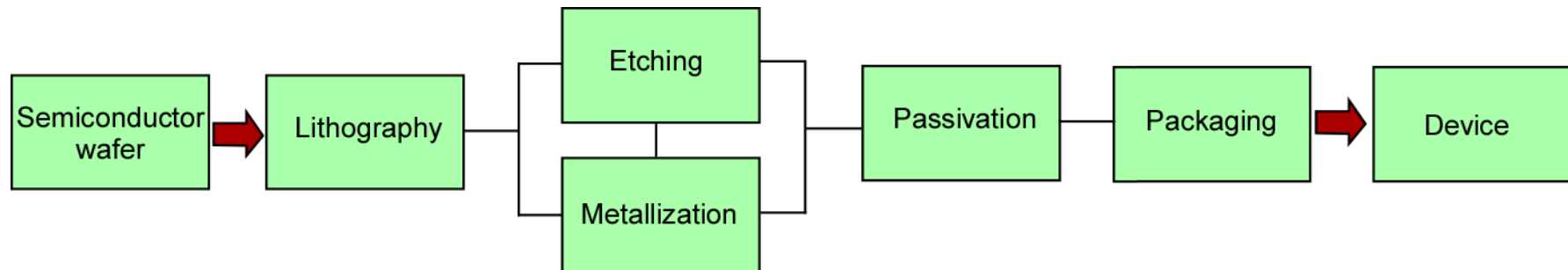
ECE 442

Solid-State Devices & Circuits

CMOS Process

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Basic Fabrication Process Chart



- **Clean Rooms**

- Semiconductor processing is performed in ultraclean facilities called clean rooms
- Sophisticated filtration to remove airborne particulates
- Workers must wear special uniforms to minimize introduction of contaminants

Clean Room Facility



CMOS Process Steps

- **Wafer Preparation**

- Crystal orientation, doping, polishing
- Typical wafers are 400 μm to 600 μm thick

- **Oxidation**

- Silicon reacts with oxygen to form silicon dioxide SiO_2
- Use high temperature ($>1000\text{ }^\circ\text{C}$) to speed up process
- SiO_2 is effective mask against impurities

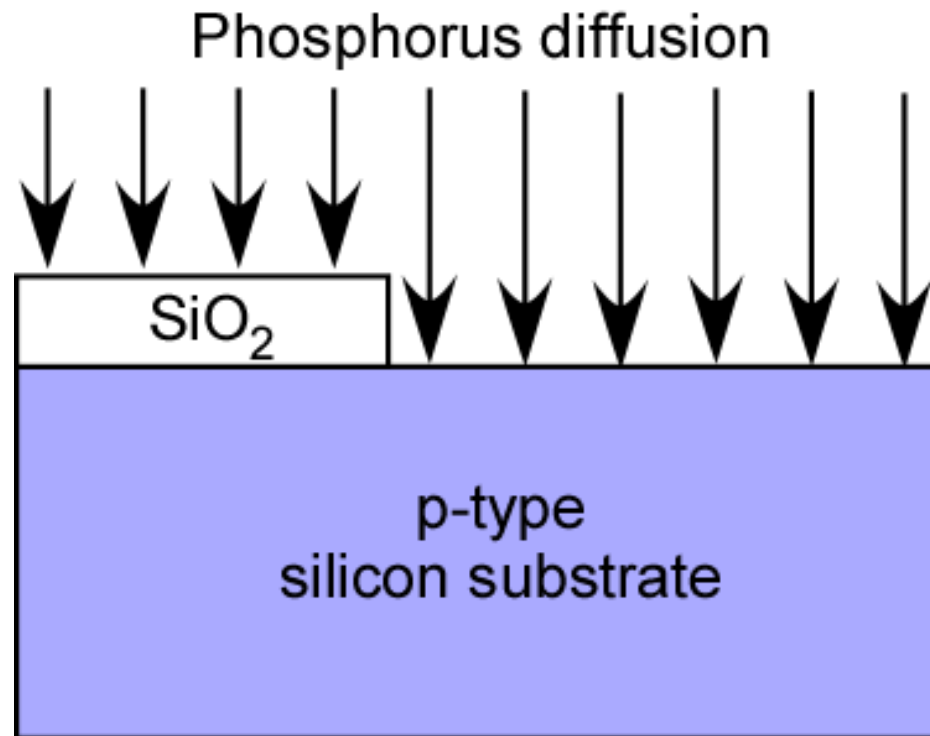
- **Diffusion**

- Atoms move from low to high concentration region in Si
- Performed at high temperature to obtain speed
- When wafer is cooled impurities are “frozen” in Si
- Boron, arsenic, phosphorus are common dopants

Process Steps

- **Ion Implantation**
 - Ions are accelerated by electric field
 - Produces more accurate and reproducible profiles than diffusion
- **Chemical Vapor Deposition**
 - Used to deposit various materials such as Si_3N_4 on Si
- **Metallization**
 - Metal layer deposited via sputtering process
- **Photolithography**
 - Wafer is coated with photoresist
 - Mask selectively exposes some regions to UV light
 - High precision is required
- **Dicing & Packaging**
 - IC's are separated from wafer
 - Die attach and wire bonding

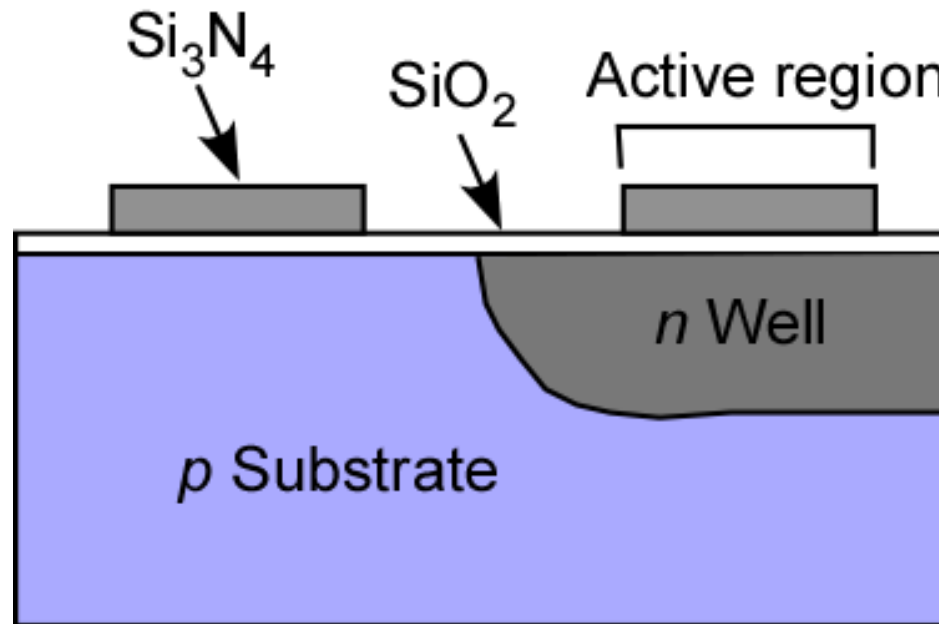
Step 1 – n-Well Diffusion



- **Diffusion Process**

- Regions for diffusion are exposed after oxide is etched
- Phosphorus diffuses faster than arsenic into substrate

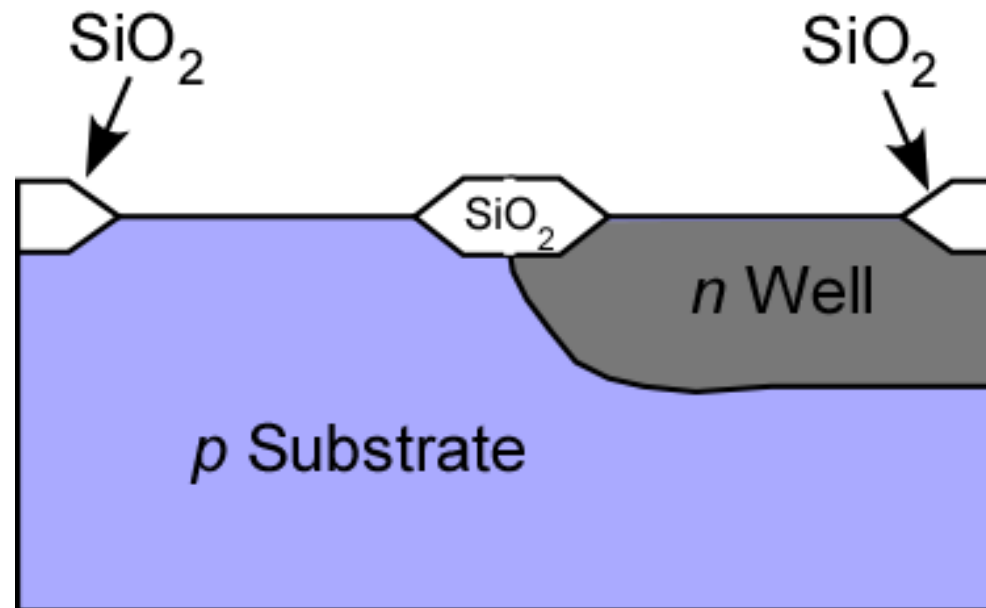
Step 2 – Define Active Regions



- **Process**

- Active regions are where transistors are to be placed
- Use silicon nitride (Si_3N_4) to mask oxidation

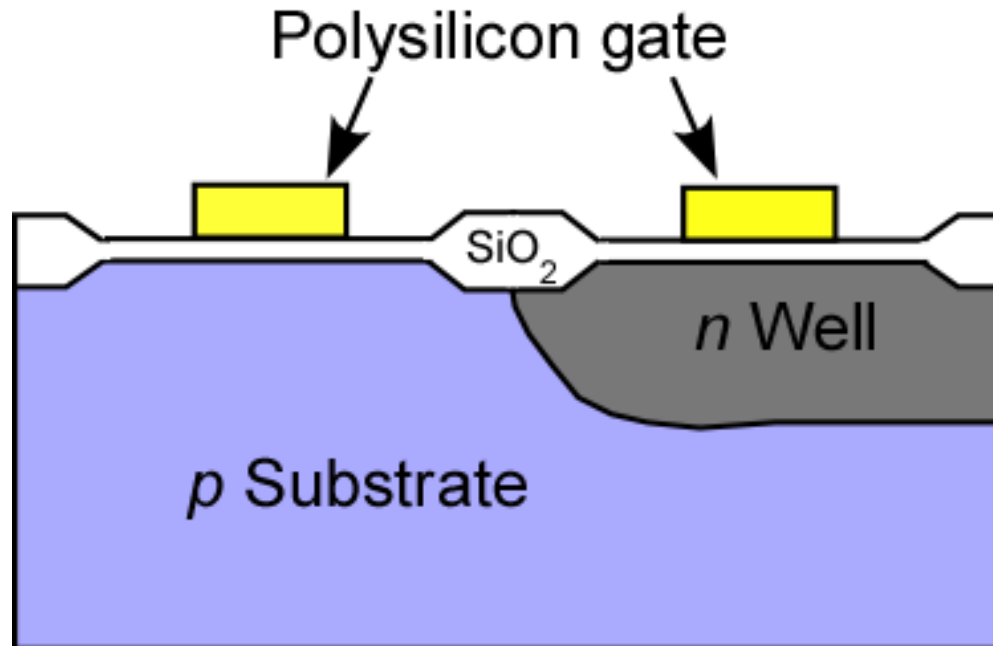
Step 3 – Local Oxidation (LOCOS)



- **Process**

- Thick field oxide appears in region between transistors
- Field oxide isolate transistors
- Allows interconnection layers to be routed to top

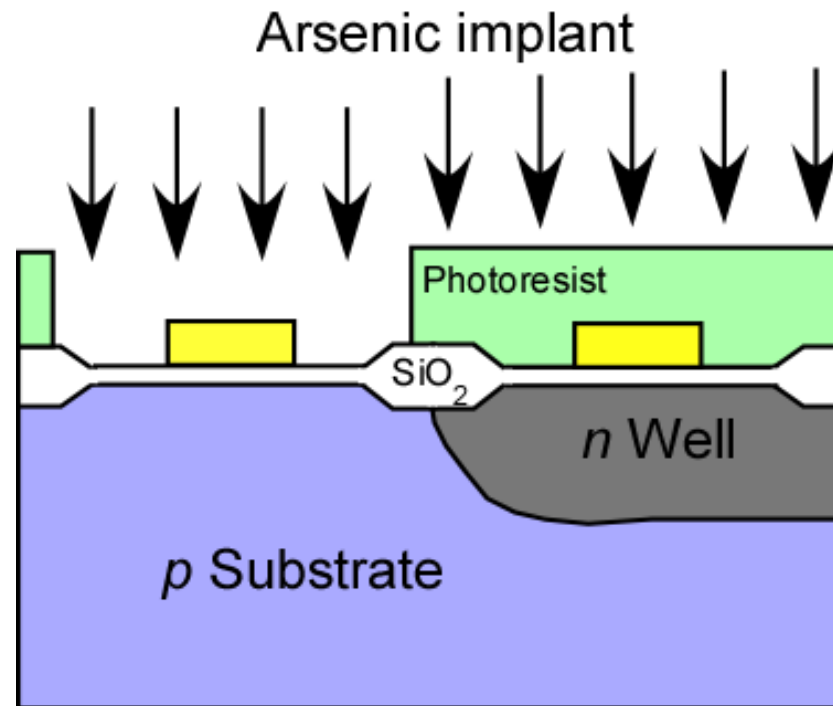
Step 4 – Gate Formation



- **Process**

- Most critical step in CMOS process
- Polysilicon layer is deposited and patterned
- Fine resolution produces short channel length

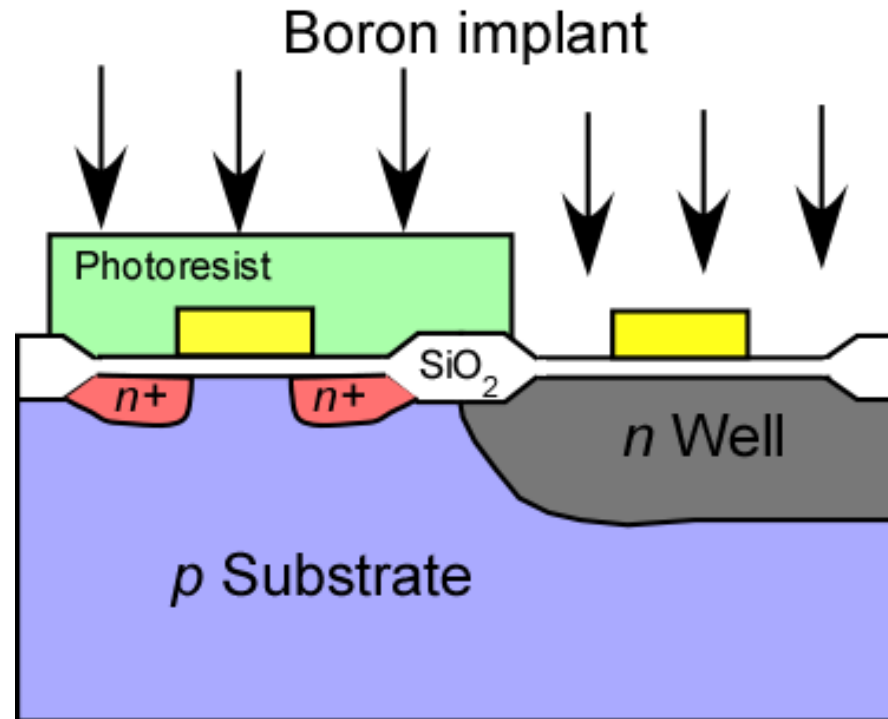
Step 5 – n+ Diffusion



- **Process**

- Photoresist protects p-MOSFET region
- Polysilicon gate acts as barrier for the implant
- Field oxide prevents formation of n+ from outside active region
- Polysilicon gate is self-aligned

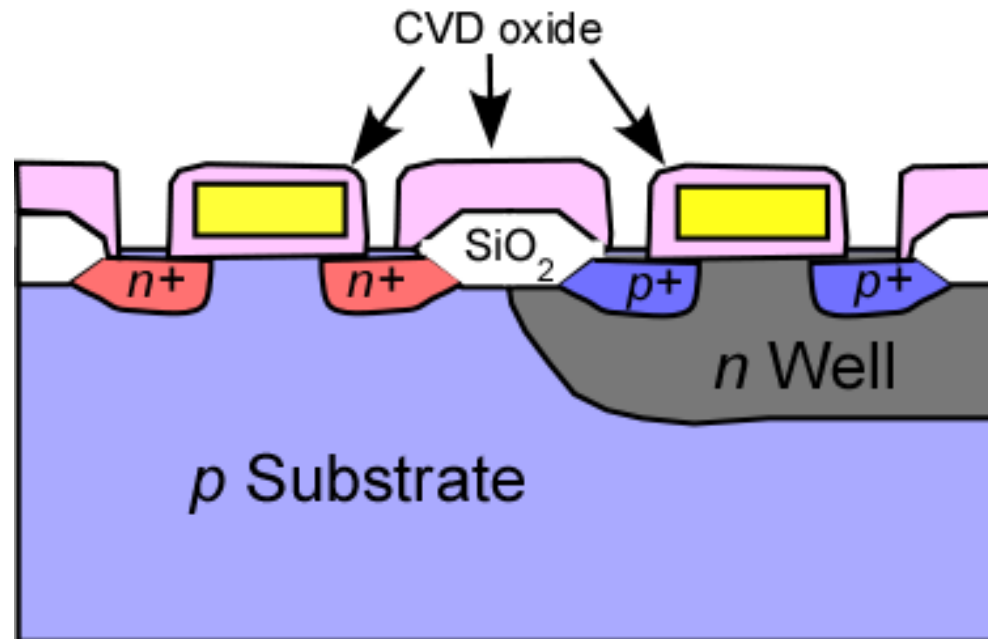
Step 6 – p+ Diffusion



- **Process**

- Channel length is defined by gate mask alone → self alignment
- Polysilicon gate acts as barrier for the implant
- Gate protects channel region

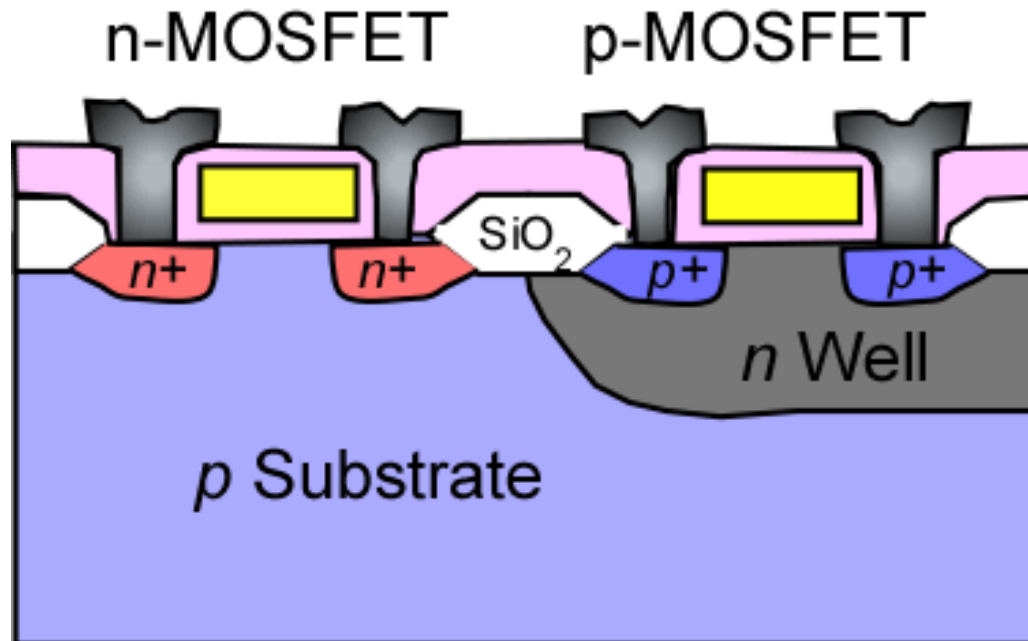
Step 7 – Contact Holes



- **Process**

- CVD oxide deposited
- Photomask is used to define contact window opening
- Etch oxide with wet or dry process

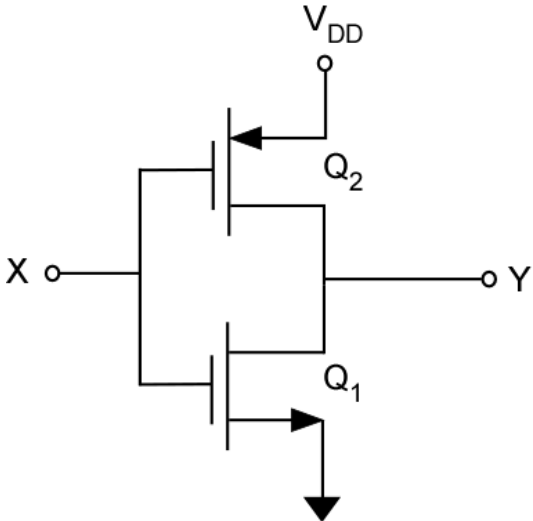
Step 8 – Metallization










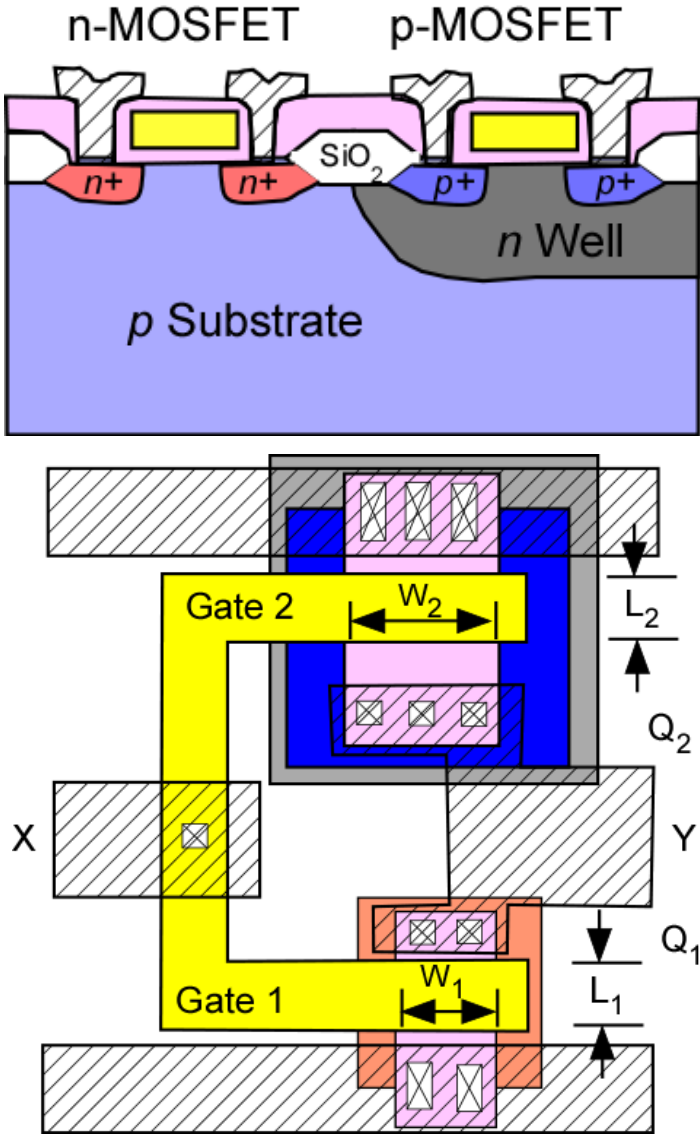
- **Process**

- Evaporate or sputter thin layer of aluminum
- Use masking to pattern interconnection
- Use CVD oxide for passivation as protective layer

CMOS Layout



-  n Well
-  Active region (LOCOS)
-  Poly 1 (poly-Si gate)
-  n+ diffusion
-  p+ diffusion
-  Contact hole
-  Metal 1



CMOS Layout

