ECE 451

Automated Microwave Measurements Laboratory

Experiment 5 - TRL calibration

1 Introduction

In previous experiments, you have been familiar with SOLT calibration method. The goal for this experiment is to get you hands-on experience with THRU-REFLECT-LINE (TRL) calibration method. This lab will take two weeks to finish. We strongly suggest you to read through the entire lab before the class, that way you have a better understanding on the lab structure. If you finish the work for week 1 early, feel free to work on week 2 materials.

In week 1, you will learn how to identify the proper LINE standard to use based on your measurements of THRU and REFLECT standards. Keep in mind that the TRL calibration set is not guaranteed to work over the frequency range of interests in this experiment even-though it shares the same effect of shifting your reference plane towards DUT. You will also perform SOLT calibration and make measurement on DUT 2: a embedded inductor which is kept from direct access by the REFLECT standard as shown in Figure 1. In week 2, you will implement your own TRL de-embedding code in Jupyter notebook. By manipulating the s-parameter data from week 1, you will be able to correctly identify the inductance of the embedded component in DUT 2.

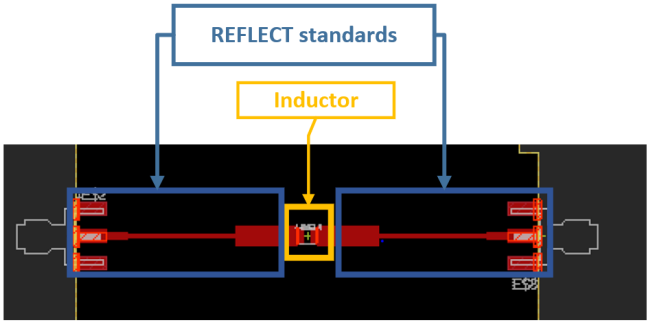

Figure 1: Inductor embedded between REFLECT standards (student board DUT 2)

2 Background

The SOLT vector error correction model was shown to be very effective in characterizing and removing systematic measurement errors. With this method, systematic errors are characterized through measurement of calibration standards, for which the actual responses are known. The accuracy obtainable is largely dependent upon the accuracy to which these actual responses are known. For coaxial measurements, suitable calibration standards with known impedance are readily available—short, open, and matched terminations are commonly used. In non-coaxial measurements, however, it is much more difficult to build standards with impedance which are easily characterized. This is particularly true in microstrip line, where short circuits are inductive, open circuits radiate energy, and purely resistive loads are hard to build.

Measuring a microstrip line based DUT is facing two potentially serious difficulties: (1) the coax-to-microstrip transition discontinuity, and (2) non-ideal transmission line characteristics of the microstrip line, such as attenuation and dispersion. Neither of these effects are characterized and removed by SOLT especially if the DUT is embedded between microstrip line traces.

The TRL calibration method uses transmission line standards instead of discrete impedance standards to obtain the terms of a two-port error model. Its math is more complicated but the result is elegant yet accurate.

Inductor Model RLC Extraction

In this lab, we are going to extract an equivalent circuit model based on the measurement data. Finding equivalent circuit is necessary due to unavoided parasitic effects in measurement or non-ideality of the component itself if we want to use the component in a larger circuit and correctly capture its effect. For example, an inductor measured in lab should be modelled using the circuit in Figure 2. First of all, all parasitic (non-ideal) effects on R should only happen at high frequency. Thus, the resistor value R should be read off directly from the impedance value (*real part of Z*) at lowest frequency possible. Then we may proceed to the extraction of C and L. Here are the two possible ways:

- **Method 1** : Notice that the parasitic ind is in series, at low frequency, the total impedance is then impedance of C (large) in parallel with series RL (small), which will be approximately same as the impedance of RL. So we could look at the imaginary part of the total impedance at lowest frequency to find:

$$L = \frac{imag(Z)}{2\pi f_{Low}} \tag{1}$$

  After L is determined, C can be calculated based on the resonant frequency: where the real impedance reaches peak or the imagery impedance reaches 0.

$$C = \frac{1}{(2\pi f_{Resonance})^2 \times L} \tag{2}$$

- **Method 2**: Notice that the parasitic cap is in shunt, at high frequency, the total impedance is then impedance of C (small) in parallel with series RL (large), which will be approximately same as the impedance of C. So we could look at the imaginary part of the total impedance at highest frequency to find:

$$C = \frac{-1}{imag(Z) \times 2\pi f_{High}} \tag{3}$$

  After C is determined, L can be calculated based on the resonant frequency: where the real impedance reaches peak or the imagery impedance reaches 0.

$$L = \frac{1}{(2\pi f_{Resonance})^2 \times C} \tag{4}$$

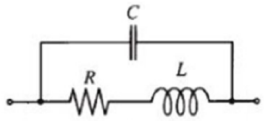

Figure 2: Inductor Model Circuit

3 Pre-lab

1. Is it required for the reflect standard to be a uniform 50 ohm transmission line? Why or why not?
2. What is the requirement of relative phase between LINE and THRU standards (HINT: TRL notes HERE)?
3. Give the S-parameters of LINE (S_{LINE}) and THRU (S_{THRU}), write the formula that calculates the relative phase between them (HINT: In Figure 3, $\frac{b_2}{c}$ could give the relative phase between LINE and THRU).
4. At a frequency f_0, S-parameter of a 2 port device is:

$$\begin{bmatrix} 0.1+0.1j & 0.8+0.2j \\ -0.8+0.2j & 0.1-0.1j \end{bmatrix}$$

   Find the corresponding R parameter where R is defined as in page 16 of the TRL lecture HERE.

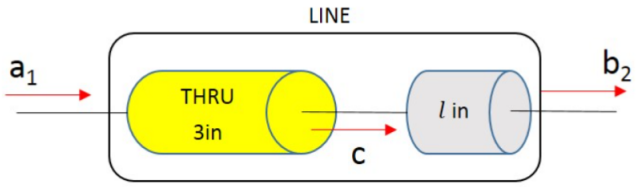

Figure 3: LINE standard break-down equivalent circuit

5. (Week 2) In ADS, plot S_{11} and S_{21} of a pure 50nH inductor on a smith chart from 100MHz to 3GHz. Put markers on the lowest and highest frequency ends (4 markers total). Explain the following items:

   - At low frequency, why S_{11} looks like a match?
   - At high frequency, why S_{21} looks like a match?

   HINT: the impedance of a pure inductor is $j\omega L$.

6. (Week 2) In ADS, draw the circuit as shown in Figure 4. Vary the value of R and C by setting up batch simulation. Make plots of real and imaginary impedance / Z-parameters (HINT: use ads function *stoz(S(1,1))*). Explain the following items with screen-shots of simulation results:

   - What happens when you tune the value of R higher? Did you see resonance frequency shifting? Did you see the real impedance peak rising? Also comment on any other phenomenons you observed.
   - What happens when you tune the value of C lower? Which way the resonance frequency is shifting? Did it make the real impedance peak higher? Also comment on any other phenomenons you observed.

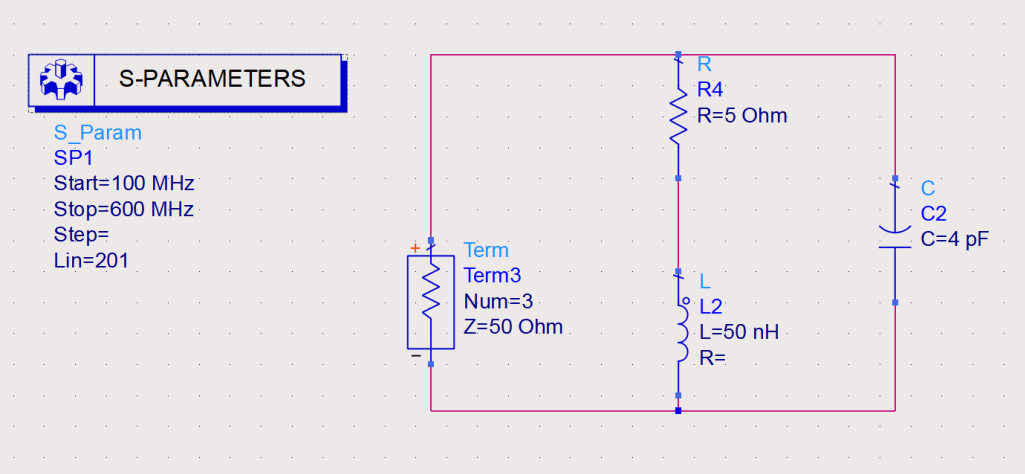

Figure 4: Schematic of inductor model circuit

4 Equipment

- Advanced Design System (ADS)
- JupyterLab
- S-A-A-2 NanoVNA
- 3.5mm SOLT calibration kit
- Student board: DUT 1, DUT 2, DUT 3, DUT 5, DUT 6 & DUT 7

5 Procedure

Part 1 (week 1) - Characterize TRL standards: 100MHz - 3GHz

In this part, you will measure THRU, REFLECT, LINE (3) with SOLT calibration to study their characteristics.

1. Calibrate NanoVNA with SOLT standards from 100MHz to 3GHz. Measure and save the following data:

   - THRU (DUT 1) as "thru.s2p"
   - REFLECT (DUT 3) as "refl.s1p"
   - LINE1 (DUT 5) as "line1.s2p"
   - LINE2 (DUT 6) as "line2.s2p"
   - LINE3 (DUT 7) as "line3.s2p"

   Note: NanoVNA only has one source on CH0. Thus, for each of the measurement only S_{11} and S_{21} are valid.

2. Create a new data display window in ADS. Import all s-parameter files (total 5) from the previous step. Be careful with naming so you don't mix up the files. Plot the phase of THRU, LINE1, LINE2 and LINE3. If your phase plot looks distorted, re-do calibration and measurement. Take a screenshot and show it to your TA before proceeding to the next step.

3. Next, you will identify the proper LINE standards to use for a certain frequency range. Plot out the relative phase of the LINEs with respect to the THRU (total 3). You may refer back to your pre-lab question 3 for the formula. One important aspect of using TRL calibration is that the relative phase of the LINE w.r.t the THRU should be maintained between singularity phase jumps..

4. Based on the plots you have, which LINE/ LINEs standard can be used for the following operating frequency? Explain your answer with screenshots and clear labelling:

   - from 100MHz to 1GHz
   - from 1GHz to 2.5GHz
   - from 10MHz to 3GHz

Part 2 (week 1) - Construct Framework for TRL De-embedding

1. Go to Jupyter Notebook and finish the coding blocks in "03-trl.ipynb". Show your work to TA before leaving. You will run the code next week.

Part 3 (week 2) - TRL De-embedding

1. Calibrate NanoVNA with SOLT standards from 100MHz to 3GHz. Measure EMBEDDED_DUT (DUT 2: inductor embedded between two REFLECT standards) and save the file as "embedded_dut.s2p".

2. Upload your measurement files (EMBEDDED_DUT, REFLECT, THRU and LINE) to Jupyter Notebook. Which LINE standard should you use in this case (operating frequency from 100MHz to 3GHz)? Run the code and plot out S_{11} and S_{21} of the de-embedded inductor on the smith chart. Confirm the plots with your TA. You might need to re-do calibration and measurement if the data is glitched. After that, plot the value of $|b|$ and $|\frac{a}{c}|$ verses frequency on the same chart. Theoretically you should have $|b| \ll |\frac{a}{c}|$.

3. Export and save your de-embedded result as "inductor.s1p" (S_{11} ONLY). In the next section, we will create an equivalent model for this inductor. There are several ways to get an equivalent model from the measured S-parameter, in this lab, we will simply use S_{11}.

4. In ADS, overlap "inductor.s1p" with the plot you have in pre-lab question 5. Compare to the ideal inductor simulation, your de-embedded value from measurement will have resonance at certain frequency. Where do you think these discrepancies come from (HINT: think of the physical reason for parasitic effects)?

Part 4 (week 2) - Identify the Embedded Component

1. Create a new data display window *"inductor_compare"*, import *"inductor.s1p"* with data file tool. Plot out its real and imaginary Z-parameters. Follow the RLC extraction process described in the Background section. You should have two sets of RLC values ready based on **Method 1** and **Method 2**.
2. Create a new schematic window *"model_1"*, draw the circuit as shown in Figure 5. The additional 50 ohm resistor resembles the VNA's internal impedance when measuring S_{11}. In other words, for any 1-port measurement, the signal sent out by the VNA will see this resistor and the entire inductor model circuit as if they are in series. Type in the RLC method you obtained from *Method 1*. Note that the R value you find from the equation is indeed the sum of NanoVNA internal impedance and inductor model impedance.

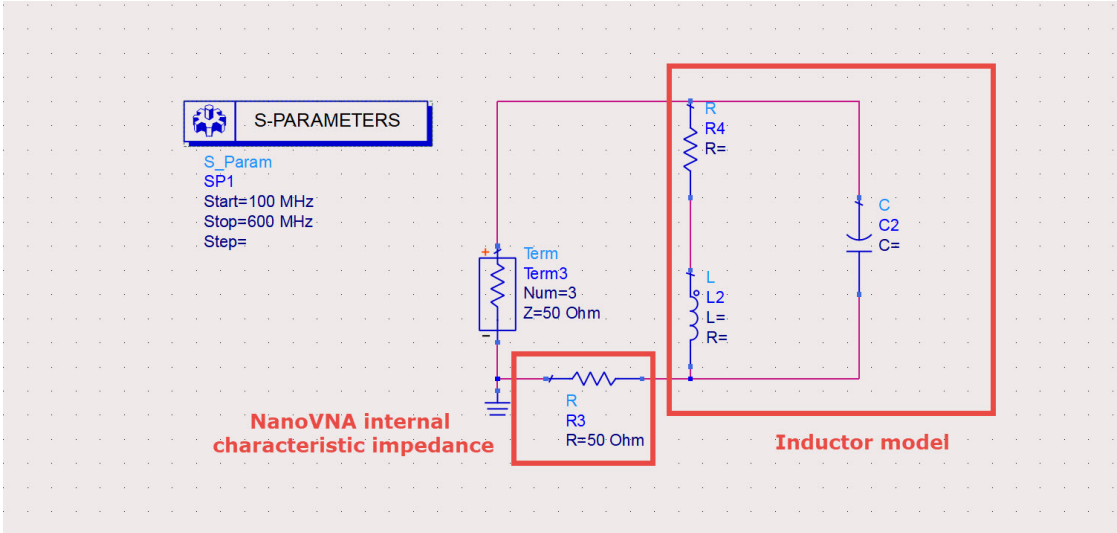

Figure 5: Inductor model with parasitic effects (VNA measurement)

3. Create a new schematic window *"model_2"*, same as in Figure 5. Type in the RLC method you obtained from *Method 2*. Again, the inductor model impedance is in series with NanoVNA internal impedance.
4. Run the two simulations above. Add both results to *"inductor_compare"* plots and change the x-axis scale to fit from 100MHz to 600MHz. Then create a smith chart with all 3 sets of data (method 1, method 2, s1p). Inspect the plots and make comments on which method fits the original data better. Why do you think the other method failed to predict the model?

6 Conclusion

1. In what scenario is TRL relatively more useful compared to SOLT?
2. For a 2-port TRL calibration, we normally need to measure 2 REFLECT standard as shown in Figure 6. Does REFLECT_A (for port 1) have to be the same as REFLECT_B (for port 2)? Explain why or why not.

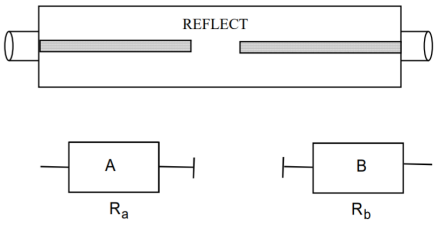

Figure 6: REFLECT standard for 2-port TRL calibration