ECE 451

Automated Microwave Measurements Laboratory

Experiment 6 - Advanced Technique

1 Introduction

In many S-parameter measurements, one wishes to obtain data for only a subsecion of the entire system under test. A a test fixture may be required between the normal coaxial calibration planes and the DUT; it may be useful to see the DUT performance with a certain matching network in place, it may be desired to see what the subsystem performance would be when the given DUT is inserted, etc.. In such cases, direct measurements of the DUT can not be performed. Figure 1 shows a simple yet concise illustration of the scenario. Here is an interesting work, measuring and modeling an on-wafer CMOS inductor, closely related to what is described in this Experiment: `http://ieeexplore.ieee.org/document/5498302/`

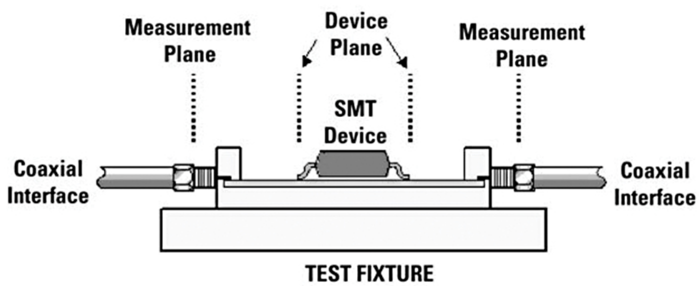

Figure 1: In-fixture measurement. Image originally from [**in-fixture-meas**]

In the previous Experiment, you learned to use TRL calibration to remove the effects of all discontinuities between the so-called *measurement plane* and the *device plane* shown in Figure 1. In this Experiment, we will investigate more techniques that allows to separate and extract the data. The first technique is *port extension.* The second technique you will learn is, in fact, the general problem of which port extension is only a simplified case, provide more accurate result for measurements with a fixture included, the *de-embedding* technique.

You will practice with these techniques on the microstrip student unknowns, which you are much familiar with by now. DUT 4 (1 port) is an impedance transformer embedded with a 50 ohm trace with certain delay shown in Figure 2. DUT 2 (2 port) is a inductor embedded between 2 discontinued traces shown in Figure 3.

2 Background

Port-extension

The classical de-embedding problem is the removal of the effects of a fixture or wafer probe. If one can treat the fixture/probe as a simple length of 50 ohm transmission line, then the problem reduces to one of shifting the reference planes, known as port extension. The familiar SOLT calibration is performed with coaxial standards, an *electrical delay* is then added to effectively extend the measurement plane through the connector and out to the desired point on the microstrip line where the device plane is, thereby obviating the need for difficult-to-build microstrip standards. This has two potentially serious drawbacks: (1) the coax-to-microstrip transition discontinuity, and (2) non ideal transmission line characteristics of the microstrip line, such as attenuation and dispersion. Neither of these effects are characterized and removed by this technique. Hence, this simple technique usually works best in measurements where the frequencies involved are not too high.

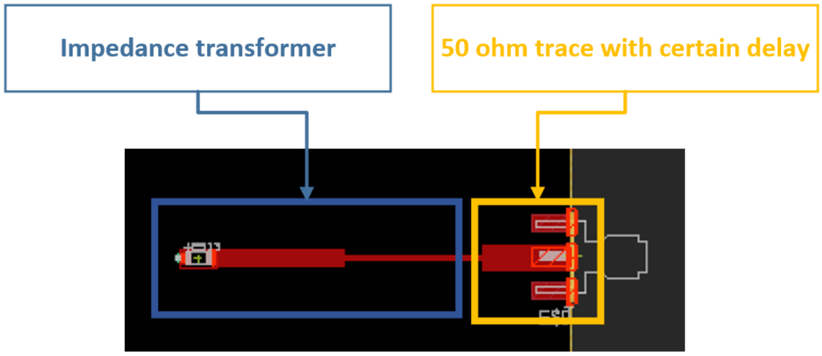

Figure 2: Embedded impedance transformer (DUT 4)

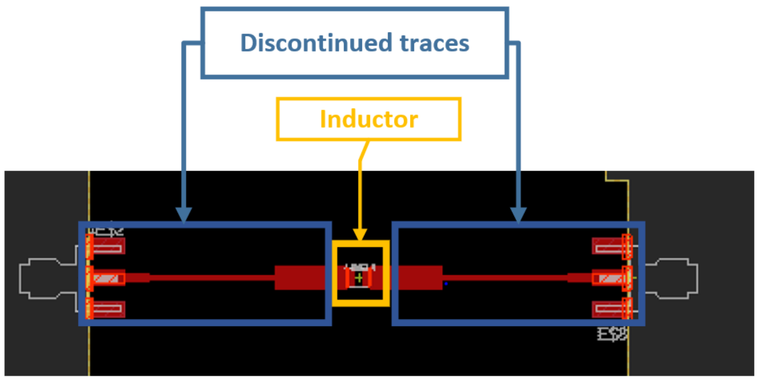

Figure 3: Embedded inductor (DUT 2)

Electrical Delay Setup on NanoVNA

After calibration on NanoVNA (not the software), disable all other traces and leave only Trace 0 available in Smith Chart format. Then go to *Display* → *Scale* → *Electrical Delay*. Insert the value of electrical delay and close the window. You can double check the value by looking at the top of the display where it says "Edelay xx ns".

2X-THRU De-embedding [1]

Previous de-embedding procedures such as Thru-Reflect-Line (TRL) and SOLT require the measurement of multiple standards. Alternatively, 2X-thru method only need measurement of one standard (Thru) with simple computation of up to four error correction terms. The other advantage of this de-embedding technique is that **no** assumptions are made for the fixtures' symmetry or reciprocity.

The measurement setup for 2X-thru is shown in Figure 4. S-parameters of Fixture A & B are obtained by solving the terms e_{ij} in the signal flow graph (Figure 5). Calculation details are beyond this course's scope and hence, will not be elaborated here.

For this course we will be using *AICC De-embedding Utility*, a Matlab Toolbox that implements 2X-thru algorithms. You can download the free beta-release here: `https://www.amphenol-icc.com/software`. Unzip the file to view the user manual and install the package to your local drive. If you are interested in learning more, here is the Gitlab page of the software's source code: `https://gitlab.com/IEEE-SA/ElecChar/P370`.

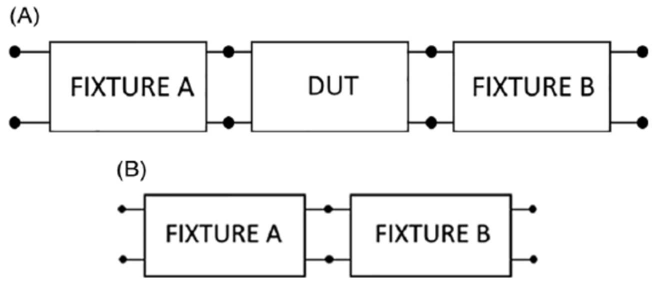

Figure 4: A, de-embedding challenge for a two-port system and B, the 2x-thru measurement setup [1]

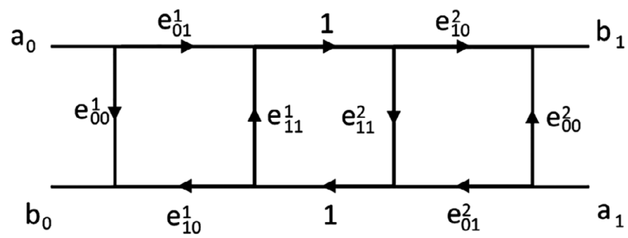

Figure 5: Signal flow graph of a 2x-thru [1]

Cascading S-parameters

De-embedding technique is based on cascading different blocks of S-parameters. It is known from the nature of S-parameter that it can **not** be cascaded directly. The most common way to deal with cascaded blocks of S-parameters is to convert them to T-parameter (derivation of S to T can be found in page 34 of s-parameter lecture notes HERE). T-parameter of the DUT is then computed and converted back to S-parameter as shown in Figure 6. Multi-port de-embedding techniques make use of more complicated formulas and hence, will not be discussed here.

3 Pre-lab

1. If the microstrip student unknown were embedded after a 1.5 inch 100Ω microstrip line, would the port extension method be able to shift the reference plane? Why or why not?

2. Given center frequency = 2.5GHz, physical length = 343 mil and dielectric constant (ϵ_r) = 4.29, calculate the **phase shift (degree)** and **electrical delay (ps)** for the extended 50Ω trace of DUT 4 (the part with yellow box in Figure 2). You may use the following equations:

$$\text{Velocity of propagation factor } (V_f) \ = 1/\sqrt{\epsilon_r} \tag{1}$$

$$\text{Wavelength } (\lambda) = (1/\text{frequency}) * (V_f \times 3 \times 10^8) \tag{2}$$

$$\text{Trace physical length} = (\text{phase shift}/360) \times \lambda \tag{3}$$

$$\text{Electrical delay} = \text{phase shift}/(360 \times \text{frequency}) \tag{4}$$

3. Open a schematic window in ADS and draw the circuits shown in Figure 7. Tune the variable X (phase of TL3) to let S_{22} match with S_{11}. Plot them on the same smith chart and include the screenshot in your report. Note that the concept of negative phase is not universal among commercial softwares (e.g SPICE). What is the physical meaning of using a TL with a negative phase shift?

4. Download *AICC De-embedding Utility Here* and read the user manual.

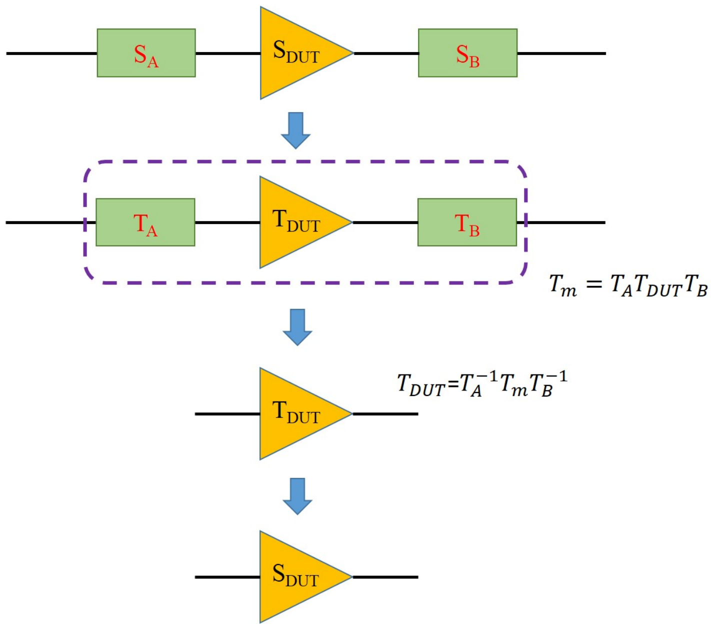

Figure 6: 2-port de-embedding formulation

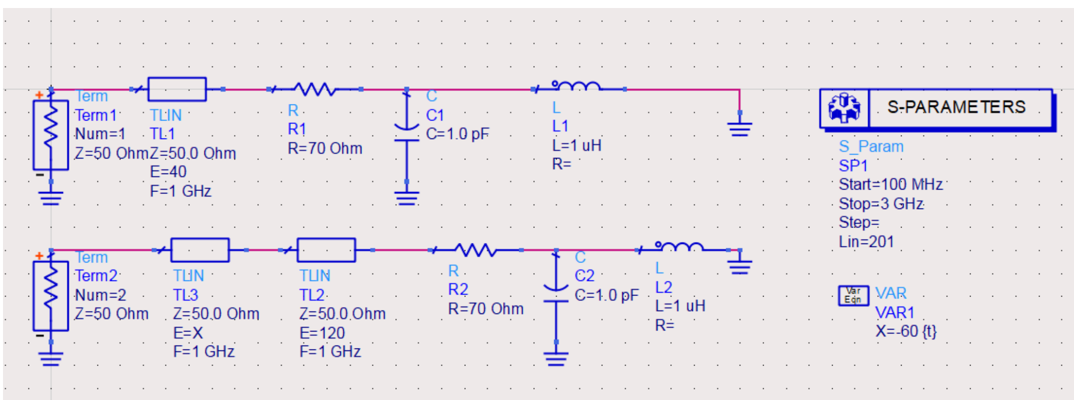

Figure 7: Pre-lab port extension exercise (negative phase delay)

4 Equipment

- Advanced Design System (ADS)
- JupyterLab
- AICC De-embedding Utility
- S-A-A-2 NanoVNA
- 3.5mm SOLT calibration kit
- Student board: DUT 1, DUT 2 & DUT 4

5 Procedure

Part I - Port extension: 100MHz - 3GHz

The microstrip student unknown (DUT 4) will be measured first. In order to bypass the 50Ω line embedded between the actual DUT and the SMA port, we need to figure out the electrical delay corresponding to that line.

1. Calibrate the VNA from 100MHz to 3GHz using SOLT. Measure DUT 4 and save the data.

2. Open ADS and construct the circuit shown in Figure 8. Import your measured data of DUT 4 to component *S1P*. Open LineCalc and send the MLIN for **Analyze**. What is the phase shift (E_Eff) given by LineCalc? What is the electrical delay in this case? Explain why are these values different from your calculation in Prelab Q2 (**HINT**: look out for K_Eff in *Calculated Results*, which is the effective dielectric constant). Out of these two phase shift values, which one should you use for port-extension and why?

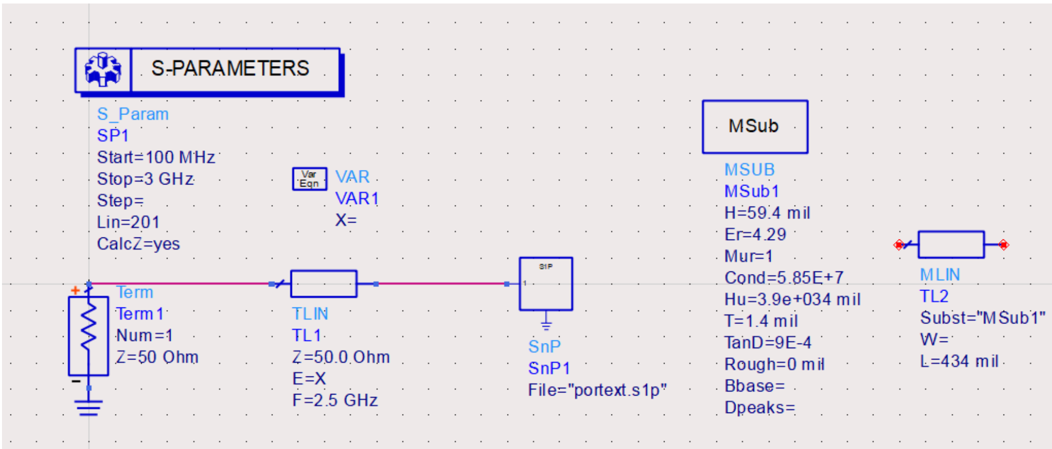

Figure 8: Schematic for port-extension (not complete)

3. Replace the variable value X with your choice of **negative** phase shift. Run simulation and plot Z_{11} in Magnitude (NOT dB) plot and S_{11} on smith chart. At center frequency (2.5GHz), what is the impedance of this transformer?

4. Calculate the electrical delay (ps) based on your choice of phase shift (degree) from the previous step. On NanoVNA (not the software), calibrate from 100MHz to 3GHz. Connect DUT 4 and follow the instructions in Background section: Electrical delay setup. Take a picture of the display and compare it with the de-embedded result from step 3. Do they match with each other? If not, what could be the problem?

Part II - 2X-THRU De-embedding: 50kHz - 3GHz

In this part, we will encounter with a more general case of embedding DUT where the "obstacles" are no longer a simple piece of 50-ohm transmission line. As shown in Figure 3, the inductor (DUT) is embedded between 2 traces. As depicted in Figure 6, we need to obtain knowledge of the 2 fixtures (S_A & S_B) between the DUT and SMA first.

1. Calibrate the VNA with SOLT calibration from 50kHz to 3GHz. Measure DUT 1 (s2p) and DUT 2 (s2p).

2. Open *AICC De-embedding Utility*, import your 2X-thru measurement (DUT 1) and the embedded DUT (DUT 2). Change Bandwidth Limit to 3GHz and Pullback to 0ns (Figure 9). Click *De-embed DUT* to kick off the calculation. Three .s2p files will be added to the folder where you stored the measurement data. Two of them are the s-parameters of the fixture models (S_A & S_B), the other one is the result after de-embedding.

3. Open ADS and draw the schematic shown in Figure 10. Notice that there are two *De_Embed2* blocks which correspond to S_A & S_B accordingly. Double click on the *De_Embed2* blocks to import the to import the fixture models you obtained from the previous step. Do NOT mix the order of these two blocks (fixture 1 must be on the left and fixture 2 on the right). For sanity check, your S_A should be very similar to the parameters shown in Figure 11. Import your embedded DUT measurement (DUT 2) to component *S2P*.

4. Click on simulation. This setup will automatically start the de-embedding procedure so the s_{ij} in the data display window should match the result given by *AICC De-embedding Utility*. To verify that, import the de-embedding result from *AICC* and plot its s_{21} on the same smith chart with your simulation. Take a screenshot and explain if the comparison meets your expectation.

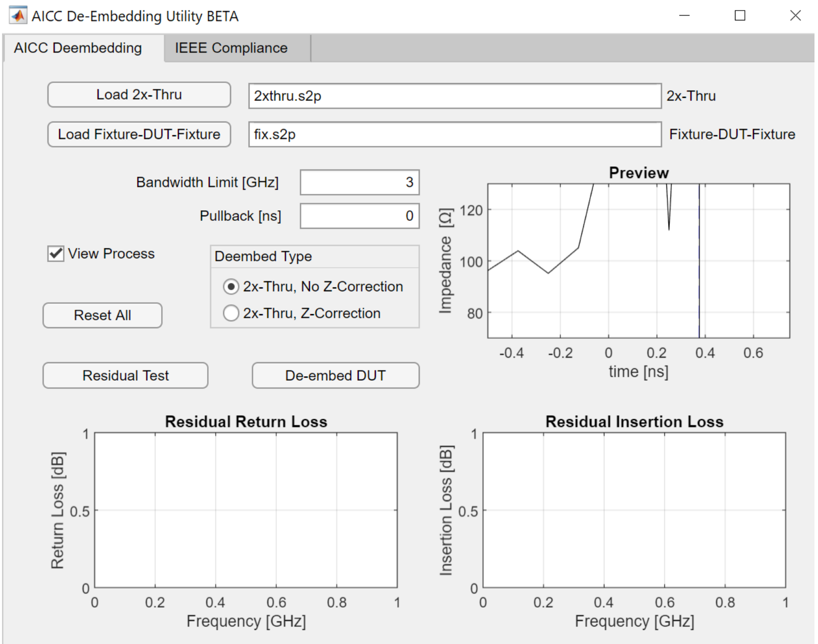

Figure 9: Schematic for port-extension (not complete)

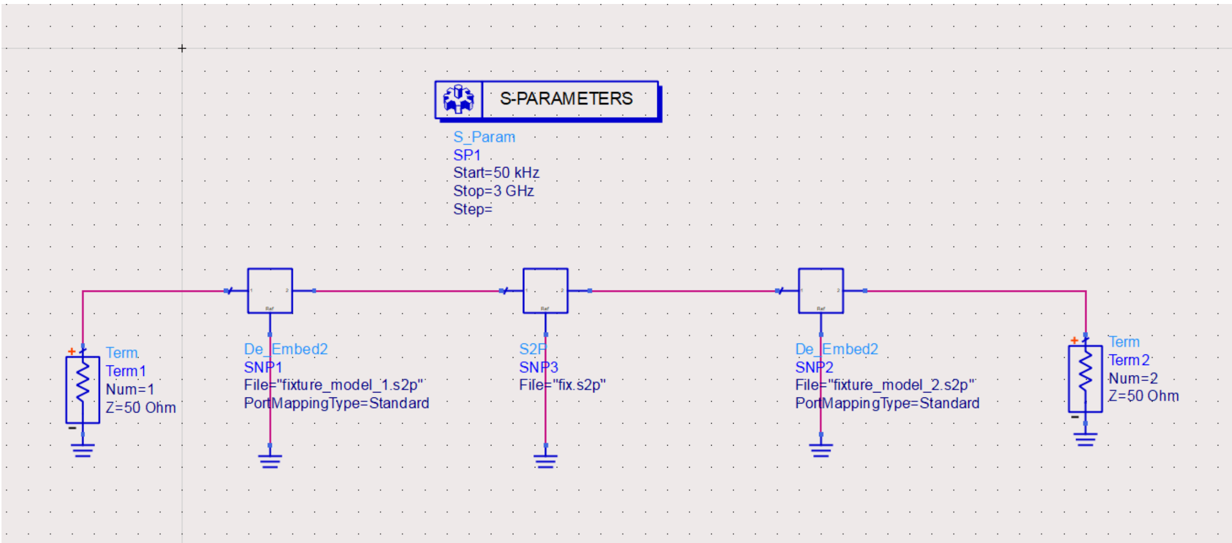

Figure 10: Schematic for port-extension (not complete)

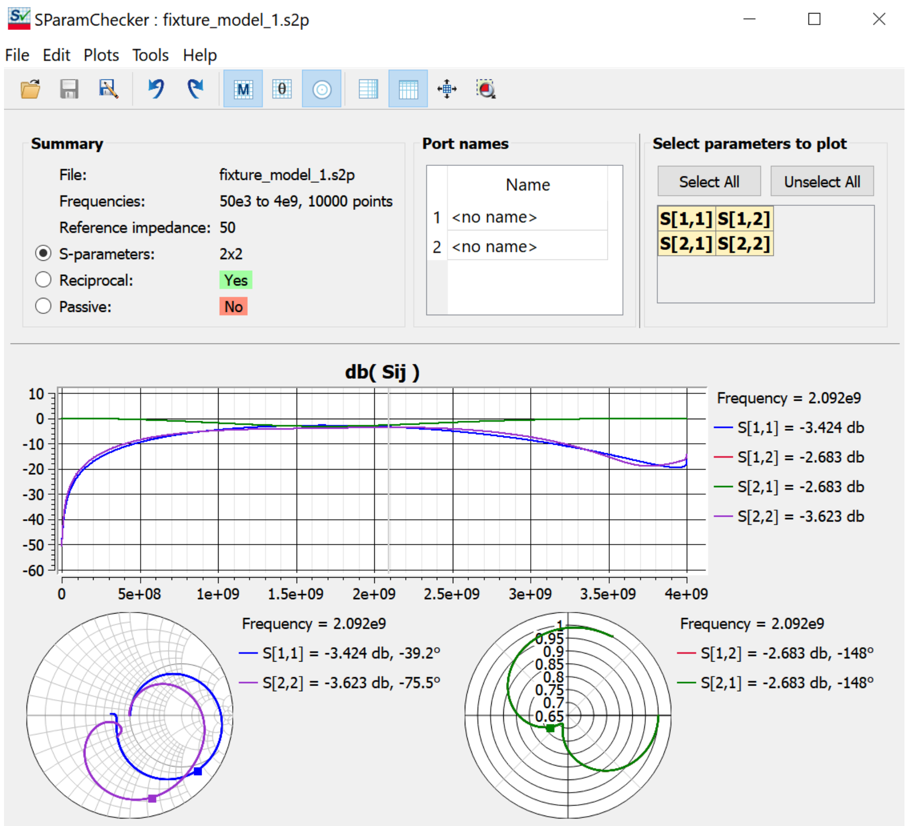

Figure 11: S-parameter of fixture_model_1 (S_A)

5. Open JupyterLab, import all your measurement data and s-parameter files generated by *AICC*. Careful with the naming to not mix up the data-sets. Create a new python3 file and follow the guidelines below:
   (a) Use s2t, transfer s-parameters of the fixture models (S_A & S_B) to t-parameters T_A & T_B.
   (b) Use s2t, transfer s-parameter of DUT 2 measurement to t-parameter T_m.
   (c) Use matrix multiplication, obtain t-parameter of the embedded inductor as $T_{DUT} = T_A^{-1} T_m T_B^{-1}$.
   (d) Use t2s, transfer t-parameter of the embedded inductor to s-parameter S_{DUT}.
   (e) On the same smith chart, plot s_{21} of S_{DUT} and the de-embedding result from *AICC*.
   (f) Take a screen shot of the smith chart (clearly labeled). Explain if the comparison meets your expectation.

   Compare to the TRL method, what is the advantages of using 2X-Thru?

6 Conclusion

1. What are pros and cons of the port extension technique?
2. So far you have learnt three methods to de-embed the inductor from DUT 2 (ADS de-embedding block, T matrix in Jupyter Notebook and TRL). Comments on the pros and cons. Which method do you prefer?

References

[1] Jason Ellison, Stephen Smith, and Sedig Agili. "Using a 2x–thru standard to achieve accurate deâembedding of measurements". In: *Microwave and Optical Technology Letters* 62 (Oct. 2019). DOI: 10.1002/mop.32098.