High-speed digital IC package characterization, using microwave probing and fixturing techniques

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Introduction

Digital VLSI packages are now required to operate at clock rates of 50-250 MHz and beyond. This requires analog bandwidths of 500 to 2500 MHz for good edge definition (see Appendix A for a discussion of how analog bandwidth relates to digital bandwidth). At these frequencies, typical digital packages will exhibit electrical behavior completely unpredicted from low frequency measurements and models. Complicating the issue, typical digital packages have metal pattern dimensions that resonate, and/or couple to the outside environment-they can act as antennas and resonators. This is the microwave region, where open lines may appear as short circuits and shorted lines as opens, depending on the frequency. Microwave designers have been successfully working with these issues for years, and now these techniques need to be adapted to the high-speed digital design environment.

The focus of this paper is to demonstrate techniques to fixture and accurately measure the high-frequency characteristics of digital IC packages. Microwave wafer probes are used to accurately measure a 169-pin PGA through the use of a special interface fixture that adapts the package to microwave probe requirements. The interface fixture is designed to duplicate the ECB environment the package will be mounted in, because the ECB has an effect on high frequency performance.

All package measurements are aimed at developing an accurate package model which a designer can use with confidence. This requires accurate measurements and a frequency limit (beyond the limit the model is not valid). The implication is that packages must be measured well beyond the maximum frequency of interest, so as to demonstrate at what frequency the model is valid.

Background

Digital IC designers and IC-package designers are now encountering high-frequency package limitations. These limitations typically appear as one of the following problems, after the IC has been designed and packaged:

a. Ground bounce (common-ground inductance)
b. Crosstalk (common-ground inductance and capacitive/inductive coupling between signal traces)
c. Power supply decoupling (series inductive elements in decoupling components and in supply lines)

Ground bounce is currently the biggest electrical problem in the silicon digital packaging industry. This is because it is often assumed that “ground” is everywhere at a constant zero volt potential. This not true in the real world. Ground bounce is caused by an inductance in the ground return path of the package[1] (fig. 1). The voltage drop across L_g is $L_g(di/dt)$, where i is the current flowing through L_g. L_g will resonate with parasitic capacitance C_p, resulting in a typical damped second-order response shown in figure 2 (the assumption is that the output driver turns on faster than the ringing frequency of the LC circuit). This results in risetime degradations and failure to meet VOH and VOL timing specifications when the IC is mounted in the package.

An additional problem related to the ground inductance is that L_g is common to all circuits on the IC (in this example). Whatever voltage drop appears across L_g due to one or more outputs switching, will affect all other circuits on the IC. So all VOLs will be compromised and all input noise margins, for example, will be adversely affected. In microwave circuits, this is simply another form of crosstalk and is modeled by including all ground inductances.

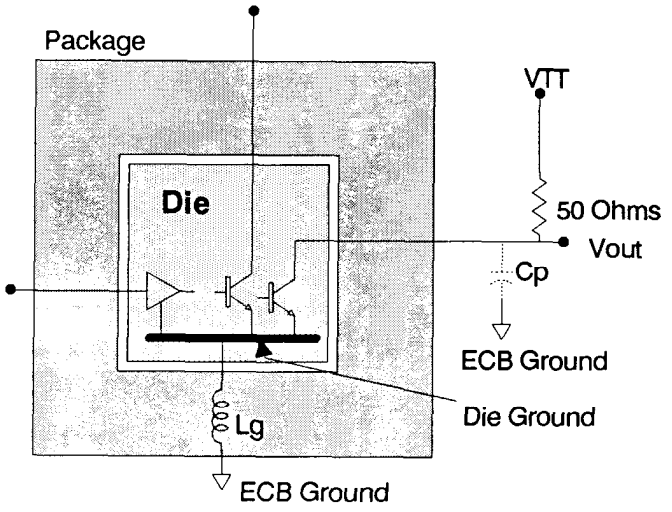


Figure 1 Simplified ground bounce model. L_g is the package common-around inductance.

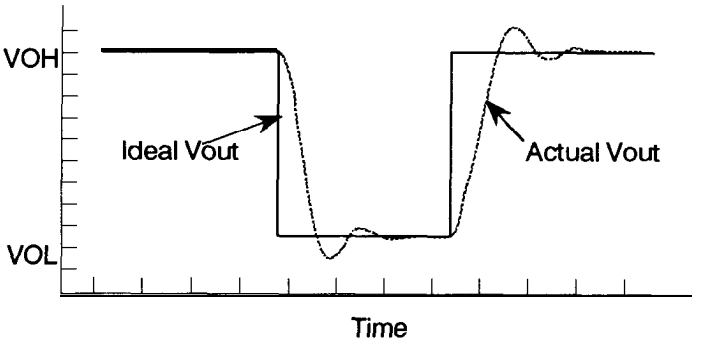


Figure 2 Degradation of rise and fall times due to common-ground inductance. Resonance of L_g with parasitic capacitance causes ringing.

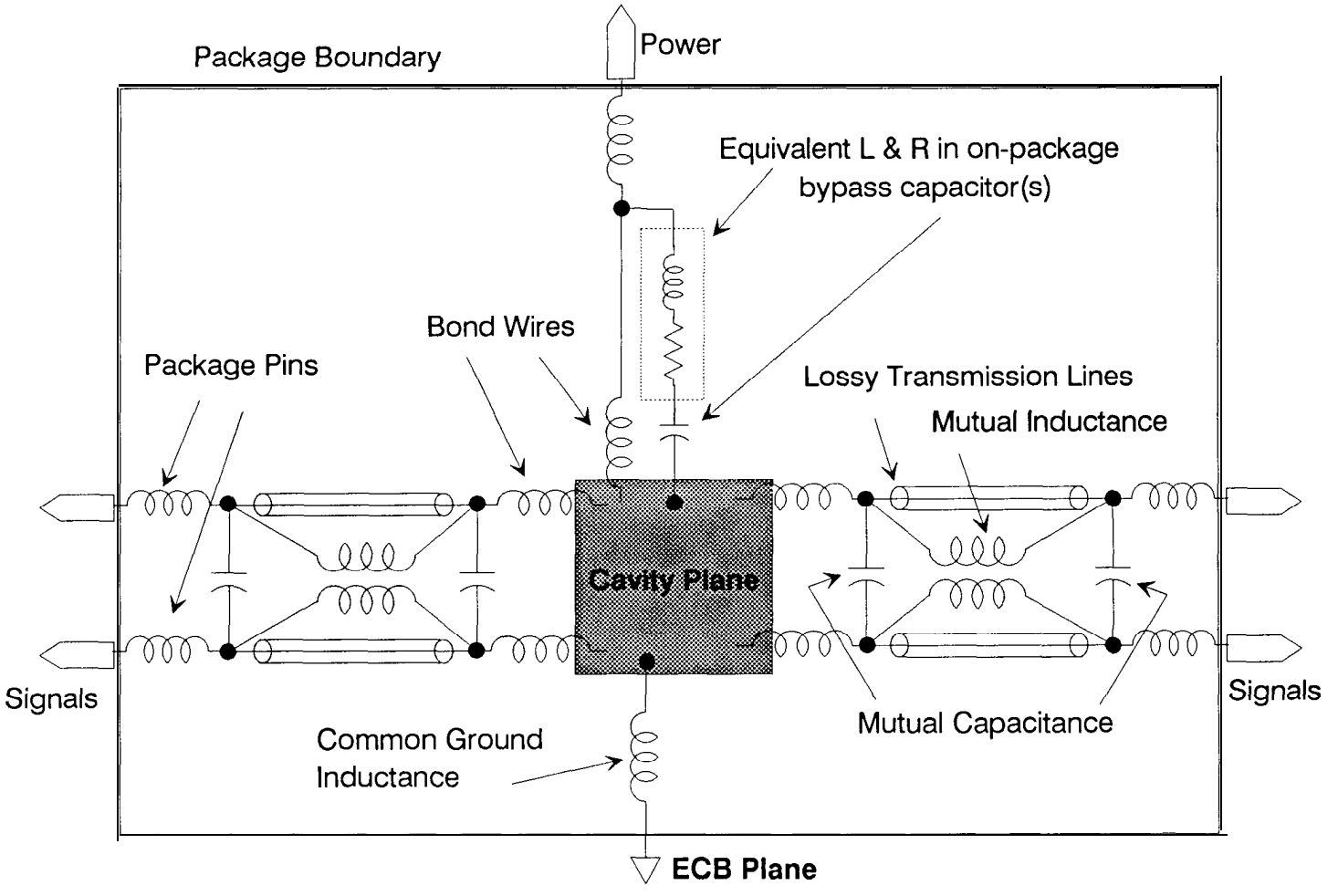


Figure 3 First-order equivalent circuit of a digital IC package.

Crosstalk is comprised of two sources: distributed capacitive and inductive coupling between the package signal lines, and common-ground inductance in the package, as discussed above. The distributed capacitive and inductive coupling, generally termed cross coupling, is usually modeled in microwave packages as coupled transmission lines. However, current SPICE software does not support coupled transmission lines and at the typical digital IC operational frequencies lumped equivalent circuits are acceptable, leading to a first-order equivalent circuit shown in figure 3. In this circuit the cross-coupling terms are the lumped mutual capacitance and mutual inductance between signal traces. In general, for most digital IC applications, the common-ground inductance contribution to crosstalk is more important than the contribution due to cross coupling, and shows up as ground bounce.

Decoupling problems are relatively well understood compared with the above problems. Decoupling describes placing lumped capacitors near the device (from supply rails to ground) to supply rapidly changing currents, thereby preventing the local voltages from changing due to series inductances in the ECB supply lines.' The problems encountered usually are related to ignoring or not knowing the inductance of the package supply lines. An additional problem occurs when it is assumed that capacitors are perfect, when in fact at high frequencies they have LRC components.

Inclusion of the three major types of parasitic relationships results in a first-order equivalent circuit (fig. 3). In this circuit there are two reference points, one being the cavity plane and the other the ECB plane. The two planes are connected by the equivalent common-ground inductance. Each signal trace contains inductors that represent the bond wire inductance and the package pin inductance. The signal traces are modeled as lossy transmission lines, which may have one or more sections with different impedances for modelling trace impedance variations. The cross coupling term is modeled as lumped mutual capacitors and mutual inductors.

Current package characterization techniques

Having identified the elements of a digital IC package model, these values need to be determined. There are several analytical and empirical methods currently being used to arrive at these values:

1. Compute all the inductance, mutual inductance, and capacitance values of a package from physical dimensions.

2. Compute the electric and magnetic fields using 2-D or 3-D field-solver programs.

3. Compute specific characteristics with in-house developed software.

4. Measure all inductances, mutual inductances, and capacitances of a package.

5. Measure the TDR response of package using TDR techniques and equipment.

The first three methods are used primarily by package designers in an attempt to design packages with specific characteristics.[2,3,4] In-house software typically requires 14 engineering years of effort and are impractical for small and medium users. Methods 4 and 5 are typically used by package users to characterize packages for specific uses.[1,5,6]

Each of these methods has significant problems at this time. Package characterization which involves calculating or measuring low-frequency (1 MHz typical) inductance and capacitance will not reflect the high-frequency resonances which actually occur. While package models using simple inductances and capacitances are accurate at low frequencies, there is no indication at what frequency these models break down due to distributed effects. If this upper frequency limit were measured and provided, this type of model could be used with much more confidence over the frequency range (see Appendix A for a discussion relating bandwidth to risetime).

The complex field-solver and in-house software programs currently are used only by the very largest companies, and generally require one or more full-time engineers dedicated to this activity. This level of commitment is generally beyond most package users. Additionally, the models produced by these programs are just now beginning to be verified by direct measurements. Also, it is not clear if these programs can yet model self-resonant structures, such as ring-shaped ground planes and antenna (radiation) effects.

Most digital engineers are familiar with using time-domain reflectometry (TDR) data. It is easy to interpret because it directly relates to physical dimensions, and preliminary models are easy to "pull of the screen." There are, however, two basic problems with TDR. One is that there is currently no quantitative way to use TDR data to optimize a model, so that the resultant hand-optimized models are more qualitative than quantitative. Secondly, until now there has been no accurate way to repeatably connect the TDR to the package under test.

A variety of fixtures have been constructed to connect TDRs to various structures, but all generally have poor repeatability.[7] Current TDRs, such as the HP 54120, can calibrate out the effects of a fixture, but the calibration is only as good as the repeatability of the fixture. Additionally, the problem is even worse because several standards must be contacted, with uncertain repeatability each time. If the fixture repeatability is 10% (a typical number), then this error is now included as part of the calibration constants. Depending on the direction of the errors during calibration, the subsequent measurements could be as much as 20% in error. The use of microwave probes to overcome this problem is discussed in the paper by Carlton, D. E., et al, "Accurate measurement of high-speed package and interconnect parasitics."[8]

Accurate high-frequency equipment and fix-bring for package characterization

High-frequency equipment for measuring small structures is readily available. A typical equipment list:

. **Microwave probe station**	Cascade Microtech Summit 9000™ Analytical Probe Station
. **Coplanar probes**	**Cascade** Microtech WPH series
. **Package interface to microwave probes**	PASlFx board, GigaTest Labs
. **Network analyzer, TDR**	HP 85106
. **Surrogate Chip and misc. cables**	Cascade Microtech

These measurement systems are comprised of mature test technology, with well understood and traceable accuracy. The PASlFx board and Surrogate Chip'" test substrate are the new pieces which adapt this measurement system for package measurements.

Ultra-high frequency wafer probes (fig. 4) were developed by Cascade Microtech seven years ago for quickly assessing how process changes would affect GaAs FET parameters. Cascade Microtech now offers probes through 75 GHz. Because these probes are much more precisely made than fixtures and can be positioned with 1-2 micron accuracy, they offer repeatability of 0.1% (-60 dB) through 10 GHz,[9] compared with 10% repeatability for fixtures. This level of repeatability is necessary to develop accurate models, otherwise the resultant model will inadvertently include the fixture errors, in addition to the desired model.

When used with automatic network analyzers (HP 8510 for example), and TDRs such as the HP 54120, the probe response can be calibrated out by using the Cascade Microtech impedance standard substrate (ISS) shown in figure 5. This substrate contains various precision elements (0.1% resistors, transmission lines, shorts, through-connections, etc.) that are necessary to calibrate the measurement system up to the probe tips. After calibration the measurement system will measure only what is beyond the probe tips. In microwave terms, the reference plane is set at the probe tips,

The GigaTest Labs Package Adapter Socket Interface Fixture (PASIFx) was developed to allow the user to easily and quickly use microwave wafer probes to contact virtually any package for electrical measurements. The PASlFx board is shown in figures 6 and 7. The board is designed for a 169-pin PGA, and has the same characteristics as the board in which the package will be used-same thickness, same material, same plating process, and same design rules. The adapter must have the same characteristics as the board because at high frequencies the package and the board may interact, and this interaction will be included in the measurements, Additionally, for packages with multiple ground pins with no internal planes, these pins need to be connected together.

The Cascade Microtech Surrogate Chip is used to furnish an internal "standard termination" for the package. These components are a new group of products designed to assist package measurements. Each Surrogate Chip has an array of test reference plane adjusters, and also has calibration elements on each chip. For this application, this thin-film chip is used to replicate a linear load of the package signal traces on the inside of the package. A Surrogate Chip photo is shown in figure 31.

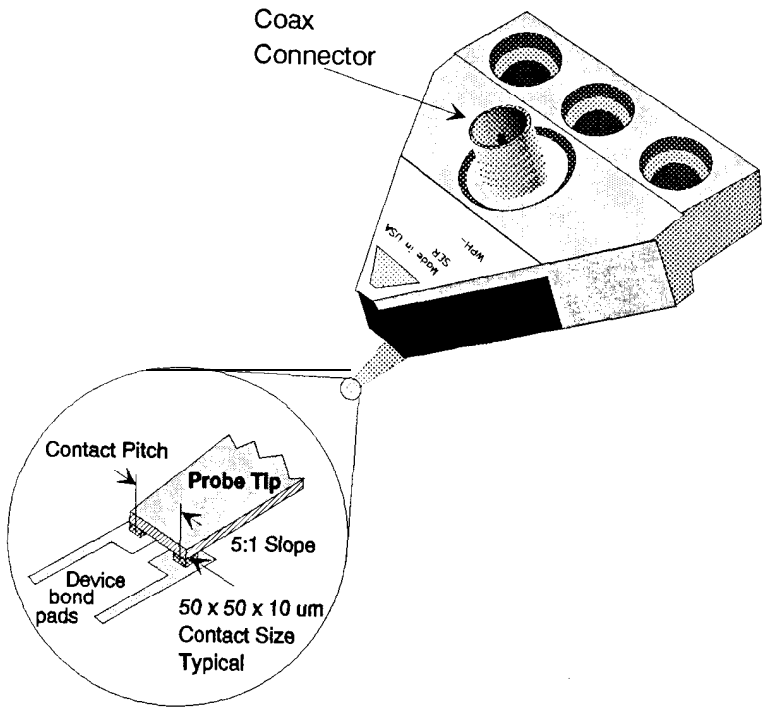


Figure 4 **Details of Cascade Microtech coplanar wafer probes.**

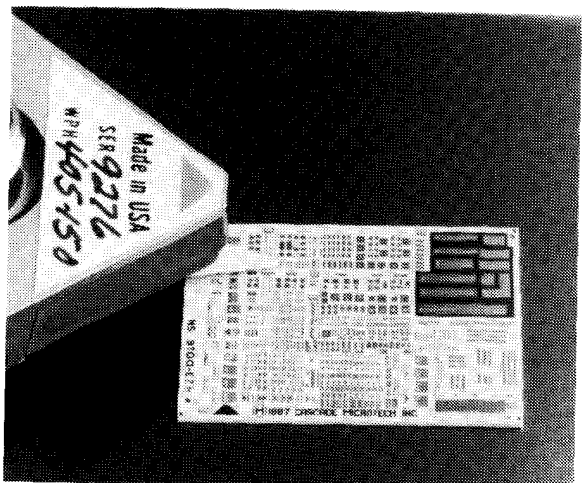


Figure 5 **Cascade Microtech Impedance Standard Substrate contains precision calibration standards for use through 75 GHz.**

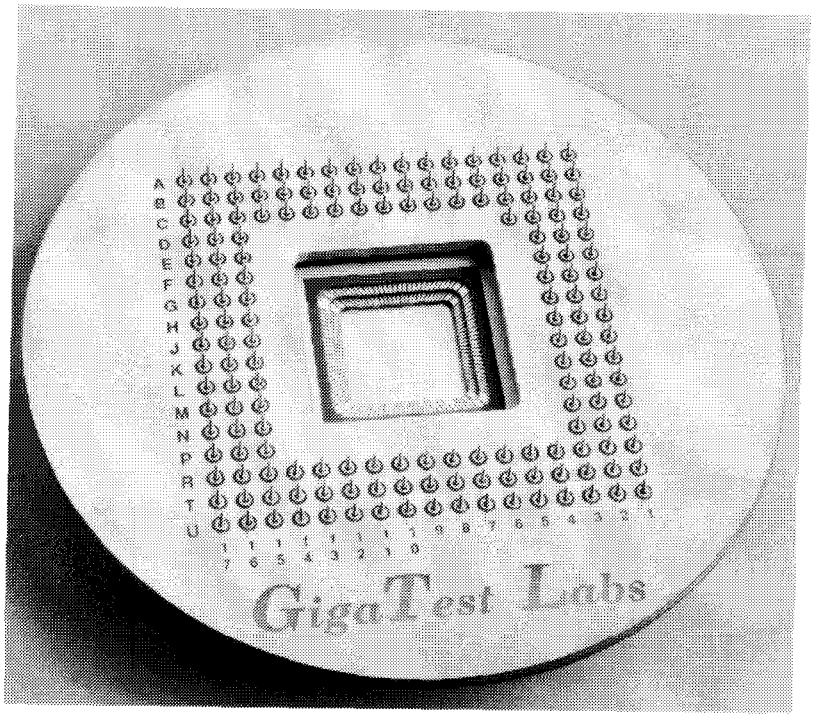


Figure 6 **GigaTest Labs PASIFx board with 169-pin PGA package.**

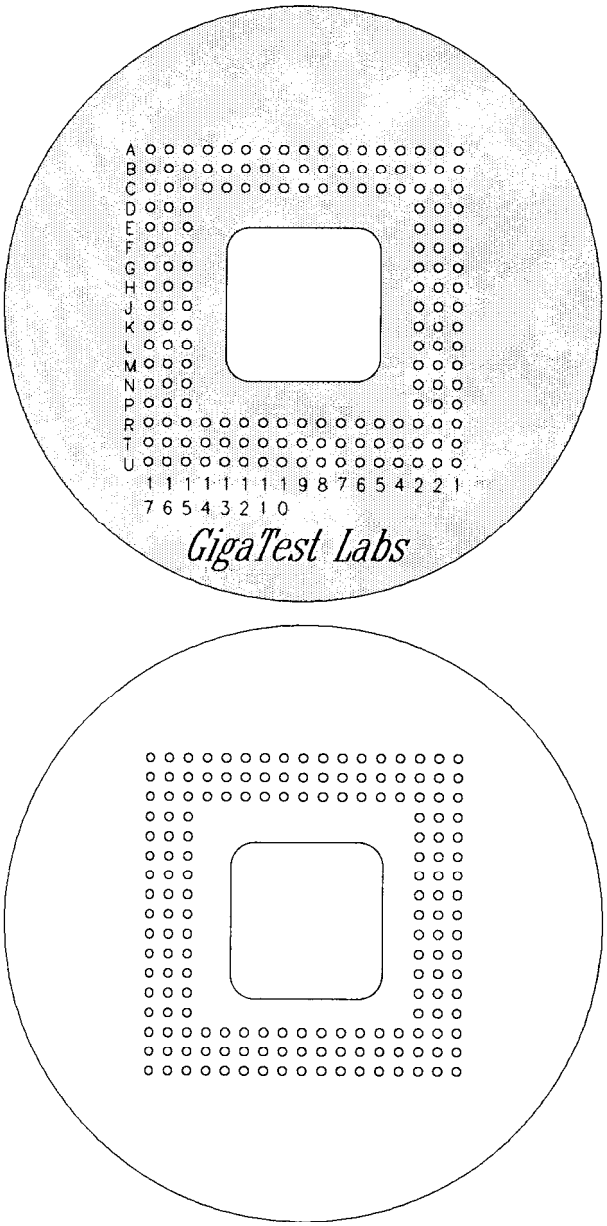


Figure 7 Front and back views of PASIFx board.

The HP 8510B network analyzer is ideal for high-frequency measurements, both from its ease of use and from the built-in TDR option. The TDR option allows the user to acquire both the frequency domain data as well as the time-domain response. Particularly useful for package designers is a feature which allows the user to gate out a particular section of time-domain response and then see the equivalent frequency-domain result. One can, in effect, alter the characteristics of a package “on-the-fly.”

The package, a 169-pin PGA (fig. 8), is mounted in the board as shown in figure 9, and the probes contact the board as shown in figure 10. This illustrates that any combination of pins can be easily contacted. Note that the cavity in this package is downward facing, and the PASIFx board has been routed to accommodate this.

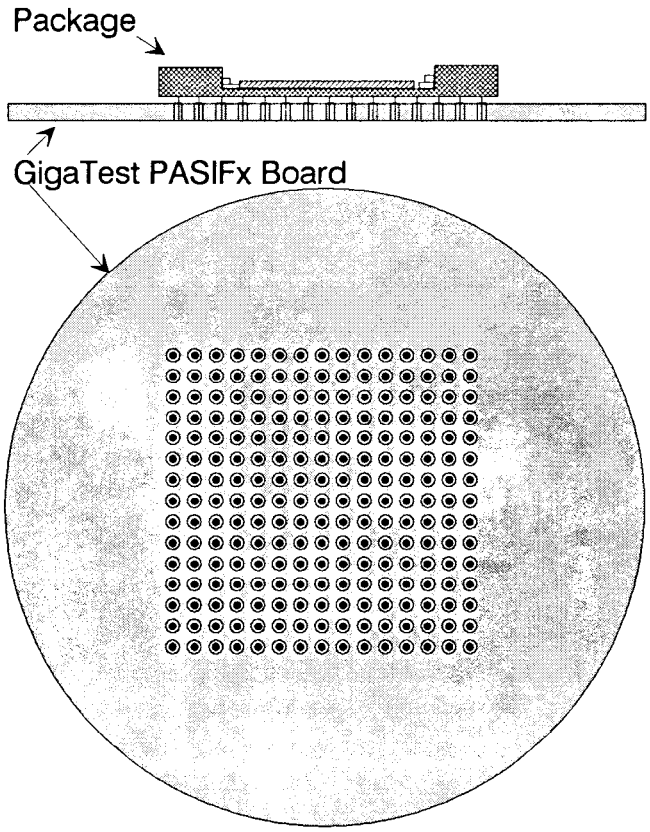


Figure 8 Details of package mounting Into the PASIFx board

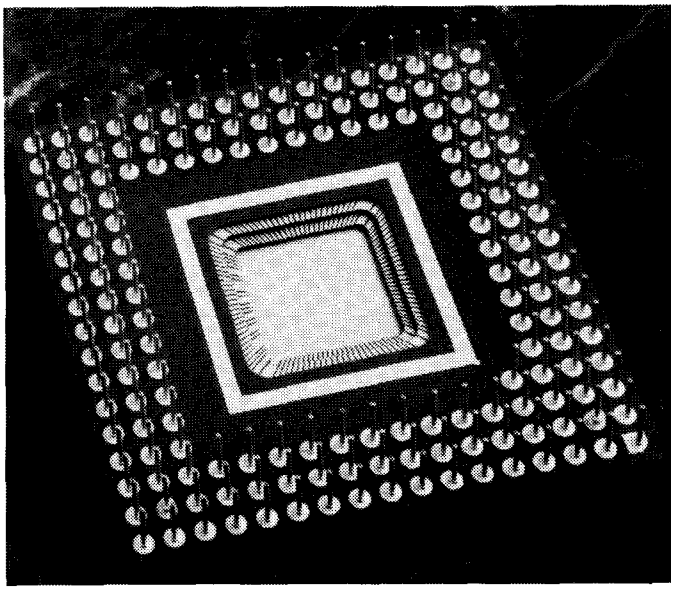


Figure 9 169-pin PGA package used for measurements.

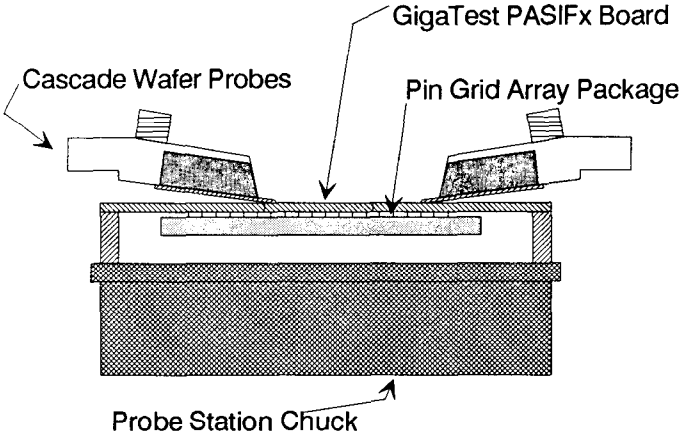


Figure 10 Details of fixture and package probing.

The probes, in this case, each have two contacts (signal and ground), with center-to-center spacing of 400μm. Contact is made to the center land and the adjacent fixture-ground plane, as shown in figure 11. With the PASIFx board, and by making the proper connections on the board and within the cavity, all measurements necessary to completely characterize the package can be easily made.

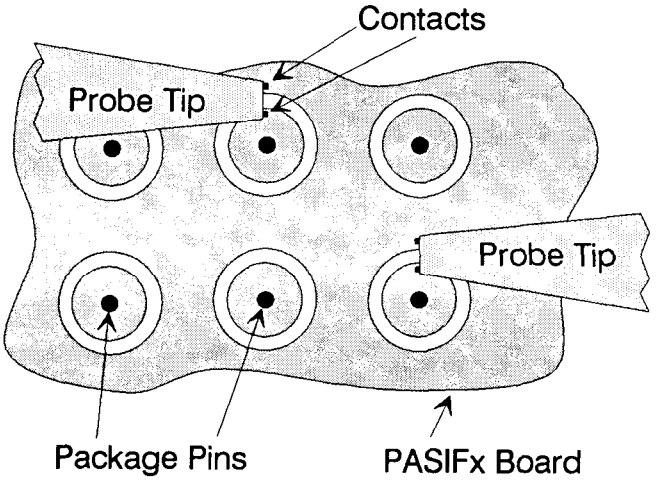


Figure 11 Details of probes contacting the lands on the PASIFx board.

Experimental results

The experimental results include data from two measurement activities. The test measurement system was first verified by using known physical and electrical structures. After verification, the previously described example was measured.

Verification measurements Measurements were first made on a fixture verification board (fig. 12) to verify the basic concept of high-frequency measurements on circuit board material. The verification board contains shorted and open 50-ohm microstrip transmission lines of various lengths, which were measured using the previously described equipment, shown in figure 13. The equipment used is listed in the previous section.

Care was taken to minimize external reflections by placing RF absorber material (Eccosorb™) on the chuck face and by using the same material to space the verification board about 3/8 inch above the chuck. Two calibrations were performed, a calibration from 0.05-10 GHz for the analog measurements and a 0.0520 GHz calibration for the TDR measurements. The wider bandwidth calibration was used with the TDR to obtain higher spatial resolution.

The calibrations were performed by first loading the calibration constants into the HP 8510, using a predefined calibration tape, and then sequentially contacting the calibration patterns on the impedance standard substrate, as shown in figure 14. This calibration typically takes five minutes, and with a warmed-up and stabilized system, will typically be valid for a week .

The S-parameters of the longest transmission line are shown in figure 15. The S_{21} loss through the transmission line is a function of frequency, and this represents good performance. For this measurement the adjacent lines were terminated to ground with 50-ohm resistors. If this was not done, little dips (1-2 dB) in the response would be present due to adjacent-line resonance. Note that both power dB and voltage ratio scales are provided. Energy reflected to the port 1 probe, S_{11}, is a function of line deviation from 50 ohms, discontinuities on the line (such as through holes at each end), and coupling to adjacent lines. The performance, again, is good. This data indicates that good performance (through 10 GHz) 50-ohm microstrip transmission lines have been fabricated on FR4 circuit board material.

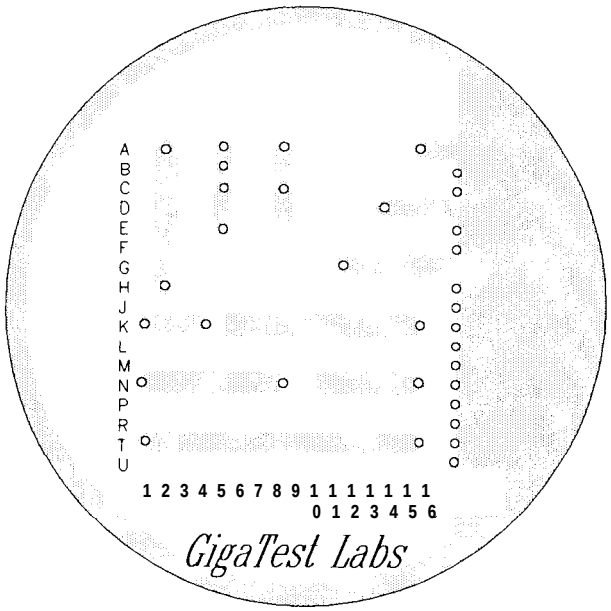


Figure 12 Top view of fixture verification board, showing open and shorted transmission lines.

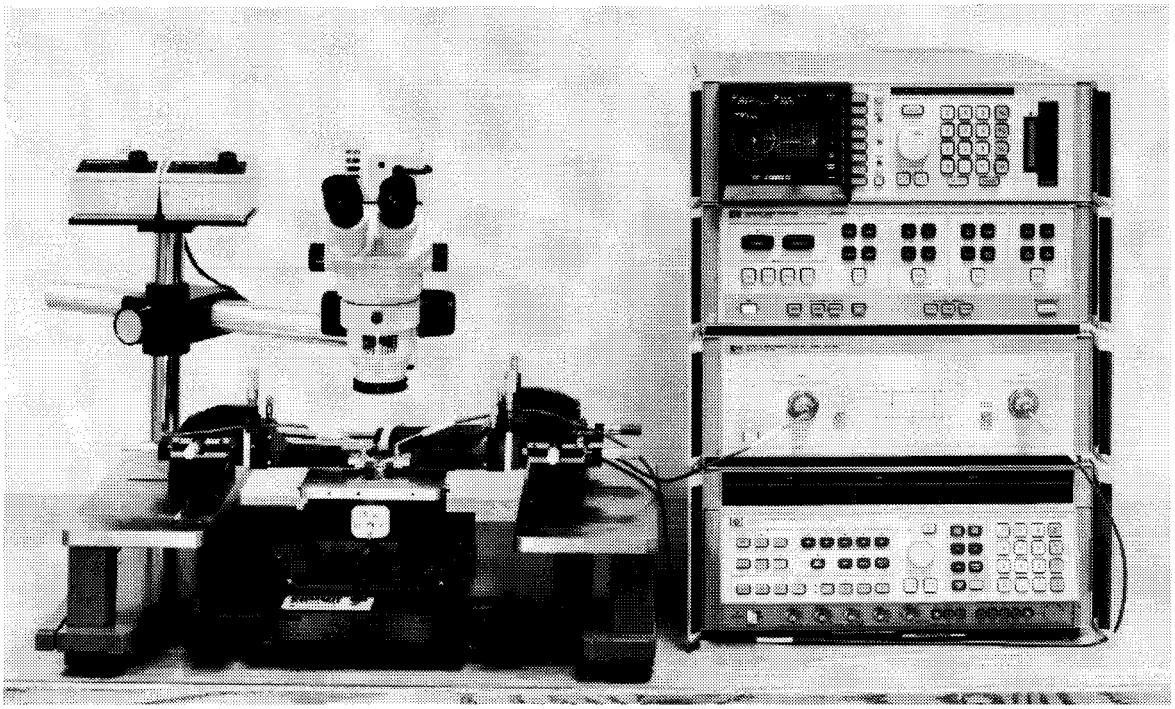


Figure 13 Typical equipment setup, with an HP 8510 network analyzer and Cascade Microtech Summit 9000™ analytical probe station.

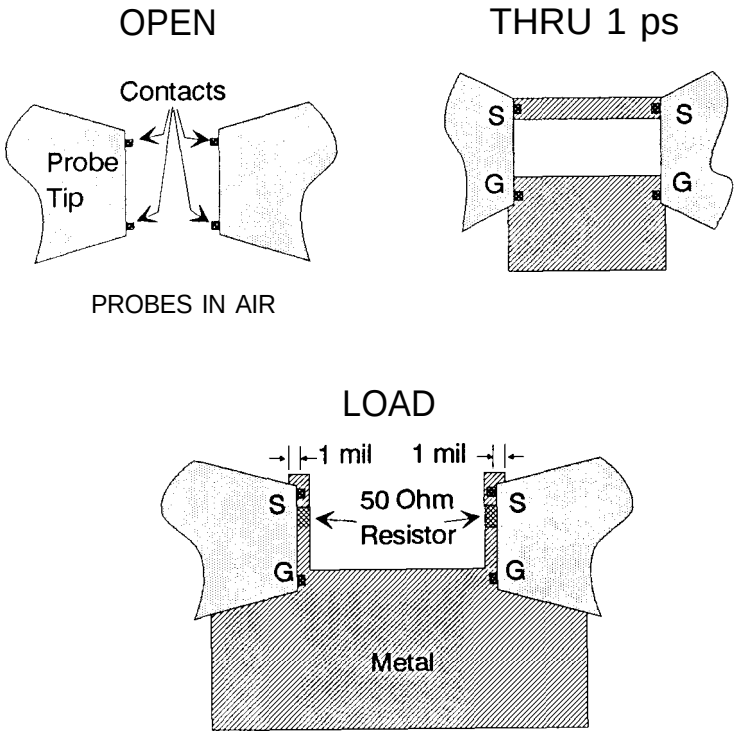


Figure 14 Calibration sequence showing which standards were contacted. Calibration typically takes 5 minutes.

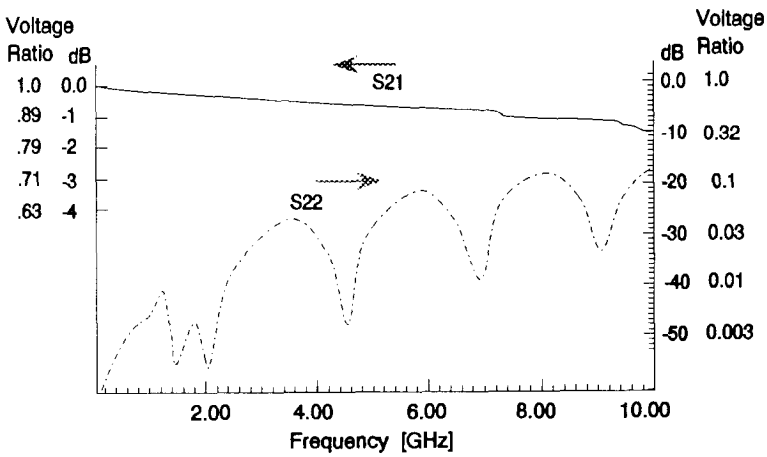


Figure 15 Response of 1.5 Inch transmission line on verification board. S_{21} is the transmission loss, and S_{22} is the reflected energy.

The TDR response of several open lines, figure 16, were measured with an HP 8510 in the TDR mode over a 20 GHz bandwidth. When the round-trip delay is plotted as a function of physical length (fig. 17) the points all lie on a straight line as expected, with the Y-intercept representing the equivalent end-effect length of the open end of the transmission line.

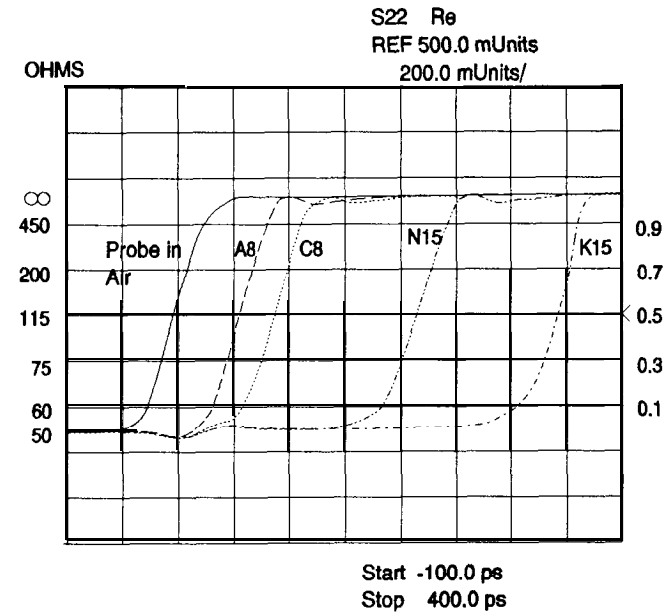


Figure 16 TDR response of several open transmission lines on the verification board.

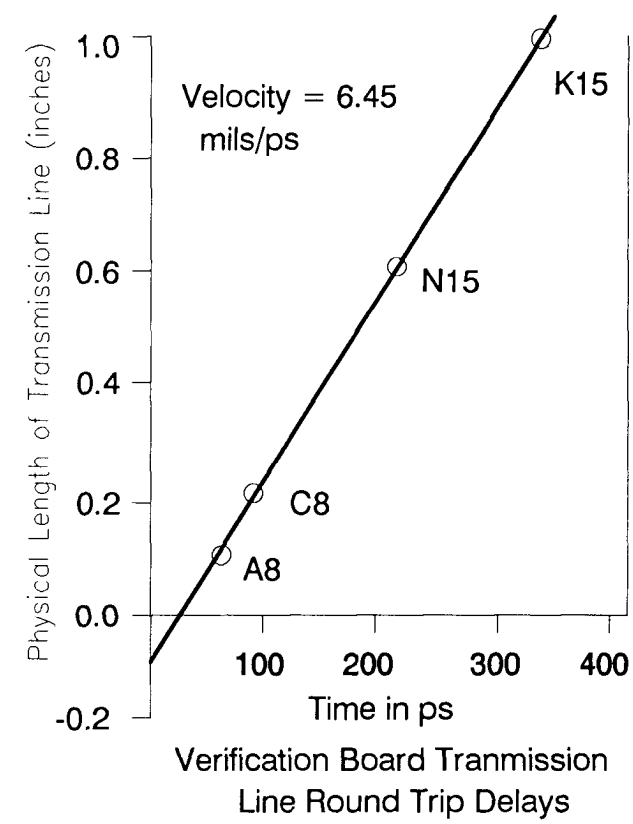


Figure 17 Plot of physical length vs. round trip delay of the lines TDR'd in figure 16. The propagation velocity Is the slope of the line, corrected to a one-path delay.

Another measurement of interest is the cross coupling between two adjacent lands on the PASIFx board (fig. 7). The data, shown in figure 18, demonstrates that cross coupling is a monotonic function of frequency and is sufficiently low through 4 GHz so that it will not mask actual package crosstalk measurements. (The PASIFx board lands can be redesigned to additionally minimize cross coupling.) A general guideline: adjacent-line crosstalk of most digital IC packages, at the maximum-rated frequency, is usually greater than -30 dB (3%) and is often greater than -10 dB (30%).

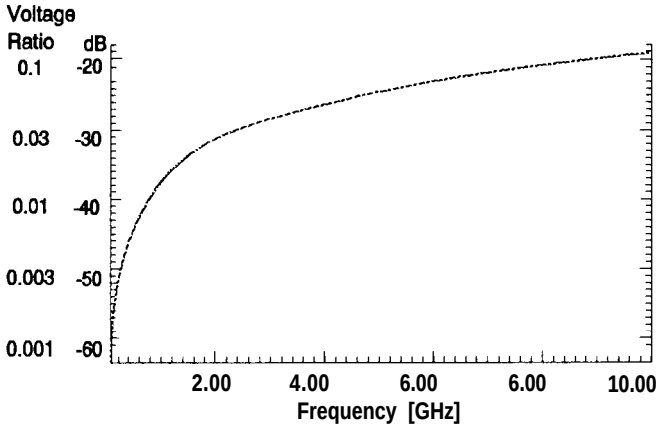


Figure 18 Cross coupling between adjacent lands on PASIFx board with no package installed.

The conclusion of these measurements is that this fixture, as designed and fabricated, will function for accurate package measurements through at least 4 GHz. If additional bandwidth is desired, then fixture lands could be modified to reduce cross coupling to adjacent lands, and a 10 GHz bandwidth is likely.

Package measurements

Package description The package measurements were all made on a 169-pin PGA (fig. 9) designed at National Semiconductor for ECL use. This package is relatively sophisticated in design and has five planes; 3 VCC, 1 VTT, and 1 VEE planes. The two signal-trace planes are located between the three VCC planes, resulting in what is known in the microwave world as stripline. With this many planes it is expected the ground inductance will be small and most of the inductance will be contributed by the package leads. An additional benefit of using the three VCC planes is expected to be constant impedance signal traces. Constant-impedance traces have relatively low cross coupling between adjacent traces because the signal-trace electric fields will be terminated mostly to the VCC planes, rather than intersecting adjacent signal traces. The pin labeling scheme is as shown in figure 7.

Equipment The equipment used is the same as for the verification measurements. The calibration ranges are also the same.

Common-ground inductance measurement The ground inductance is common to all measurements and is one of the most difficult parameters to measure accurately. It is recommended that the ground inductance be measured first, as it may be a significant part of all other measurements and inadvertent errors may result if the common-ground inductance is not considered.

The approach used to measure ground inductance was to (a) wire bond all VCC, VEE, VTT cavity traces to the cavity plane (the cavity plane is the VEE plane in this case); (b) connect all the package ground pins to the fixture plane except one (A8), resulting in the first-order equivalent circuit shown in figure 19. Thus, the inductance measured is primarily that of just one pin, and the effect of the other pins inductance is the same as pin A8. The measurements are shown on a Smith chart (fig. 20). Recall that on a Smith chart, all purely resistive values lie on the horizontal axis, with (in this case) 50 ohms in the center, 0 ohms on the far left, and infinite ohms on the far right. Inductive responses are on the top semicircle, and capacitive on the bottom. The frequency response of a pure inductor would start at the far left at dc (a short circuit), and as the frequency increased, would travel clockwise around the top of the Smith chart until finally, at infinite frequency, it would be at the far right point.

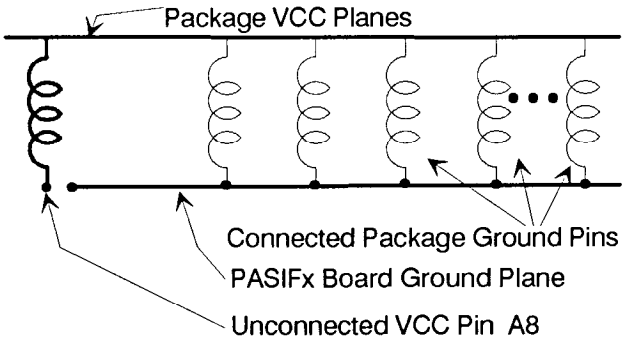


Figure 19 Equivalent circuit of the VCC plane (ground) inductance measurement. All VCC pins are connected to fixture ground except A8, which is measured.

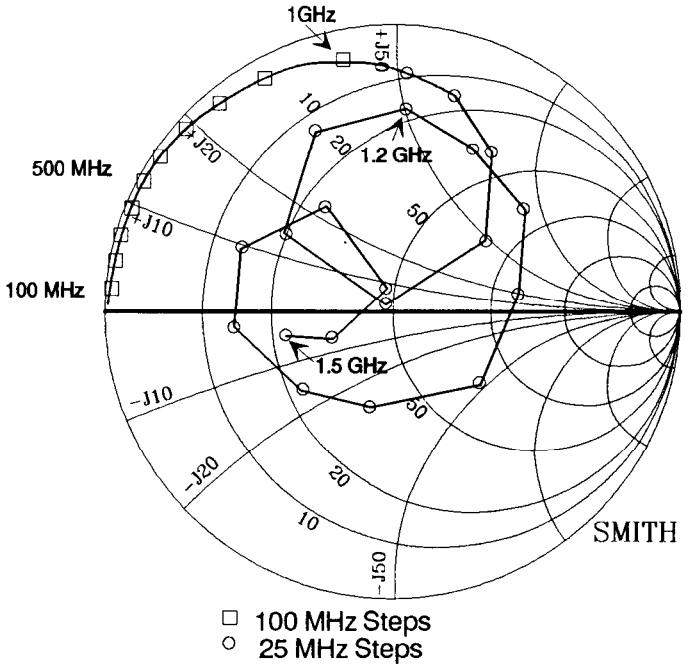


Figure 20 Smith chart response of ground-inductance measurement. Note initial inductive response, followed by three closely spaced (in frequency) resonances (looping).

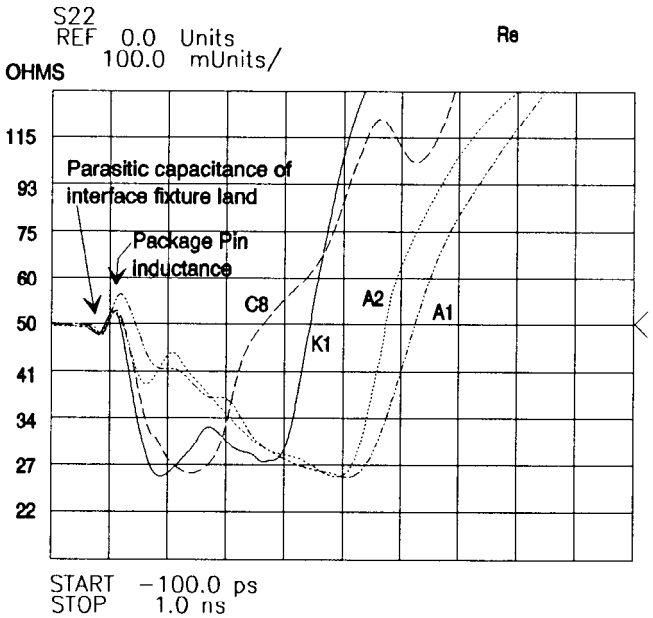


Figure 21 TDR of the longest, shortest, and two additional signal traces in the 169-pin PGA. The traces are not terminated in the cavity.

The S-parameter data (fig. 20) shows an inductive response up to 1.1 GHz, with a small resistive component (indicated by the response moving inside the Smith chart) then various resonances are encountered, indicated by the looping on the Smith chart. The inductance value is 4.5 nH, and since there are 15 VCC pins, the average VCC plane common inductance is 0.28 nH. One can also measure other VCC pins to see if there is a spatial dependence on the inductance value (if there is, then a more complex model may be required).

Open trace TDR The HP 8510 was used in the TDR mode (20 GHz bandwidth) to look at the longest and shortest signal traces and two signal traces in between (fig. 21). The signal traces were not terminated in the cavity. When the physical length is plotted versus the round-trip delay (fig. 22), all the points lie on a straight line, as expected. The Y-intercept is the trace end effect, and the length of the package pin connected to the PASIFx board. The TDR data indicates that the package signal traces are not 50 ohms, but rather about 30 ohms, and some signal traces are relatively constant impedance, whereas others are not. Note the response due to the capacitive load on the land and via of the PASIFx board, and the inductive response due to each package pin.

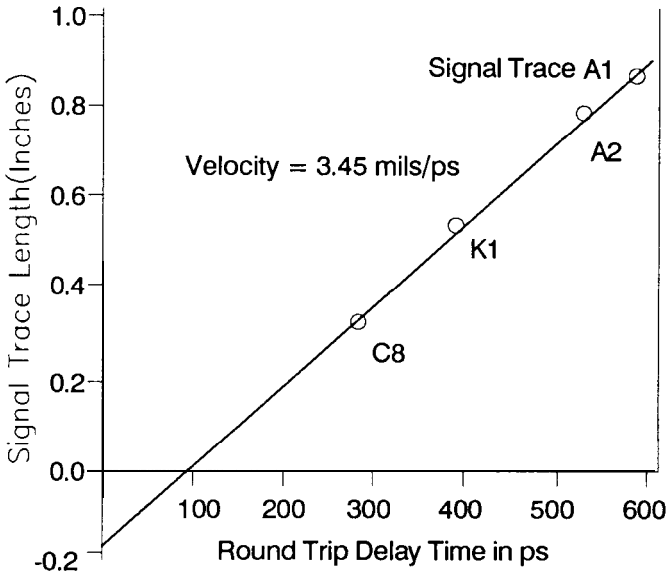


Figure 22 Plot of physical length versus round trip delay for the signal traces TDR'd in figure 21. The propagation velocity is the slope of the line, corrected to a one-path delay.

Transmission A 50-ohm transmission line (part of a calibration standard) was scribed, epoxied in the cavity (fig. 23) and wire bonded to traces K1 and K17. Probes were landed on pins K1 and K17 on the PASIFx board, measurements made, shown in figure 24. In figure 24, the TDR response looking into pin K1 and pin K17 are both plotted. The TDR response first shows an approximately 30-ohm trace, followed by the 50-ohm transmission line in the cavity, and then the other trace. The second trace does not show a 30-ohm response, but it must be remembered that much of the initial voltage step was reflected back to the source generator at the first 50-ohm to 30-ohm transition, and that this needs to be corrected for at subsequent reflections. The fact that the K1 and K17 response are similar verifies this.

The S-parameters are shown in figure 25. The frequency response S_{21} is the loss, and below about 0.8 GHz the loss is minimal, becoming higher at the 1-2 GHz range. This is because most of the energy is being reflected from the 50- to 30-ohm discontinuity, as seen in S_{11}. At frequencies above 3.2 GHz the transmission loss becomes severe, probably because the metalization is resistive and rough, resulting in high skin effect losses. This indicates that this metalization system is probably not usable above 3 GHz. Simpler transmission line test structures would need to be laid out and fabricated to more accurately evaluate high-frequency metalization performance, if that is desired.

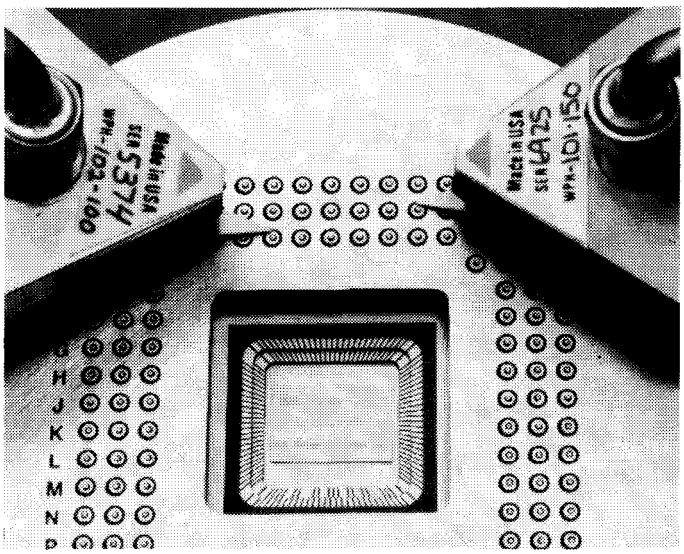


Figure 23 Photo showing 50-ohm transmission line in the 169-pin PGA cavity, set up to measure the series combination of: signal trace K1, the transmission line, and signal trace K17.

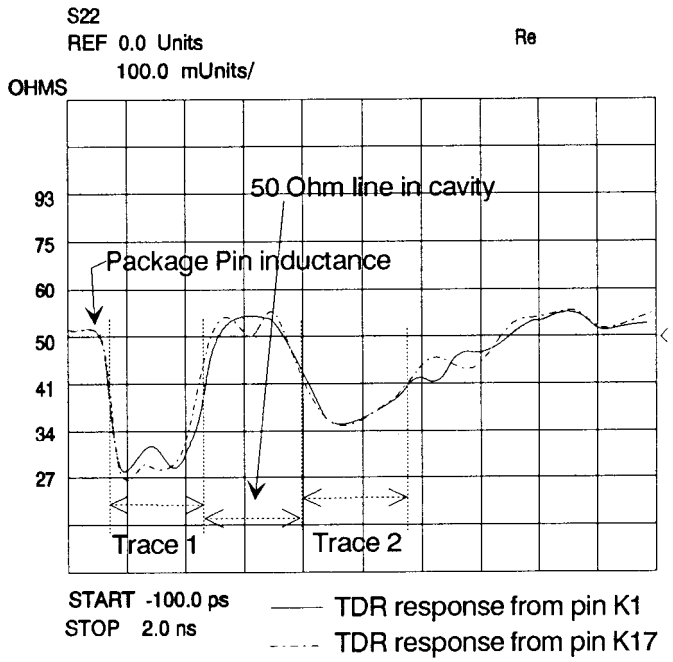


Figure 24 TDR of the series combination described in figure 23. The signal trace impedance is about 30 ohms.

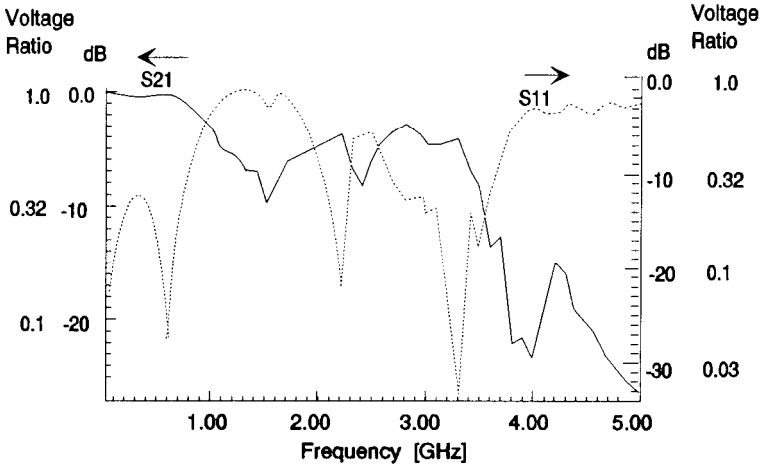


Figure 25 S-parameter response of the series combination described in figure 23.

Cross coupling Two adjacent lines, A1 and A2, were terminated in 30 ohms in the cavity with the Cascade Microtech Surrogate Chip™ test substrate. Traces Al and A2 were selected because they are among the longest traces in this package, and would be expected to exhibit worst-case cross coupling. Figure 27 shows the terminated case frequency response. S-parameter S_{12} is the coupling between traces A1 and A2 as measured at the PASIFx board, and is -20 dB (10%) or less up through 800 MHz. At 1 GHz cross coupling is - 10 dB (30%) and remains at that level or greater through 5 GHz.

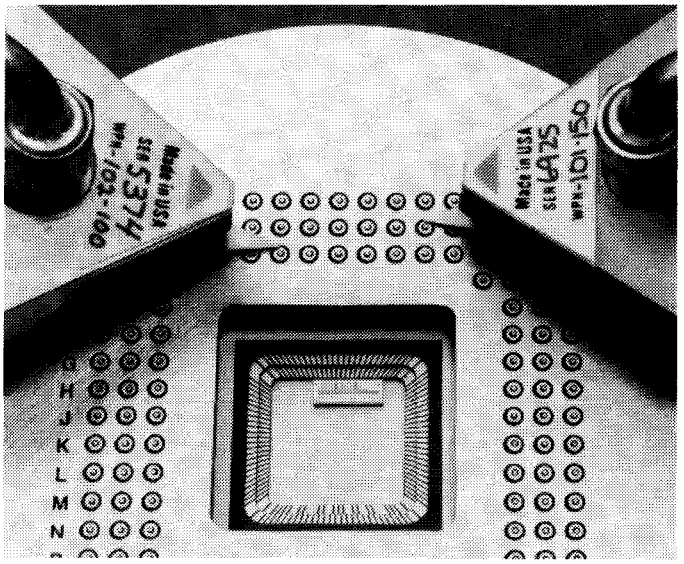


Figure **26 Photo showing Cascade Microtech Surrogate Chip terminating signal traces A1 and A2 for cross-coupling measurements.**

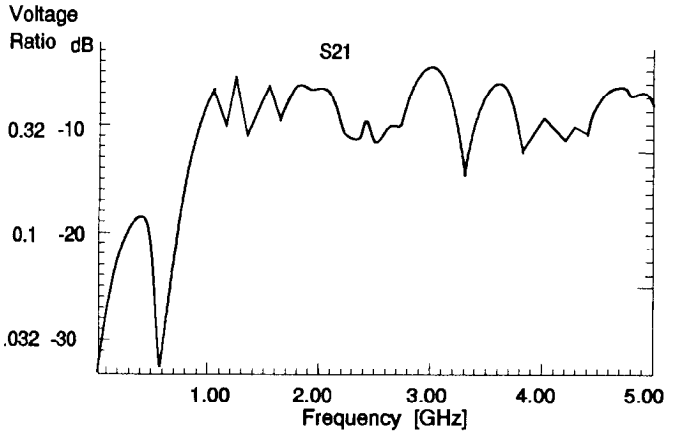


Figure 27 Cross-coupling measurements between signal traces A1 and A2, terminated in cavity with 30 ohms.

Discussion of package measurements and preliminary modeling

The Smith chart response of the ground inductance demonstrates a fundamental problem in package design. As shown in figure 20, the response below 1 GHz is inductive, with a slight resistive component, then at about 1.1 GHz a resonance occurs, followed immediately by two more resonances. The first resonance is probably caused by the VCC plane resonating. The first resonance point of a metal plane occurs at a half wavelength. From figure 22, the signal propagation velocity is 3.45 mils/ps, and the VCC planes are roughly 1.7 x 1.7 inches in size. Recall that

$$\lambda = 1/f,$$

where

1 is the wavelength in units of time and
f is the frequency.

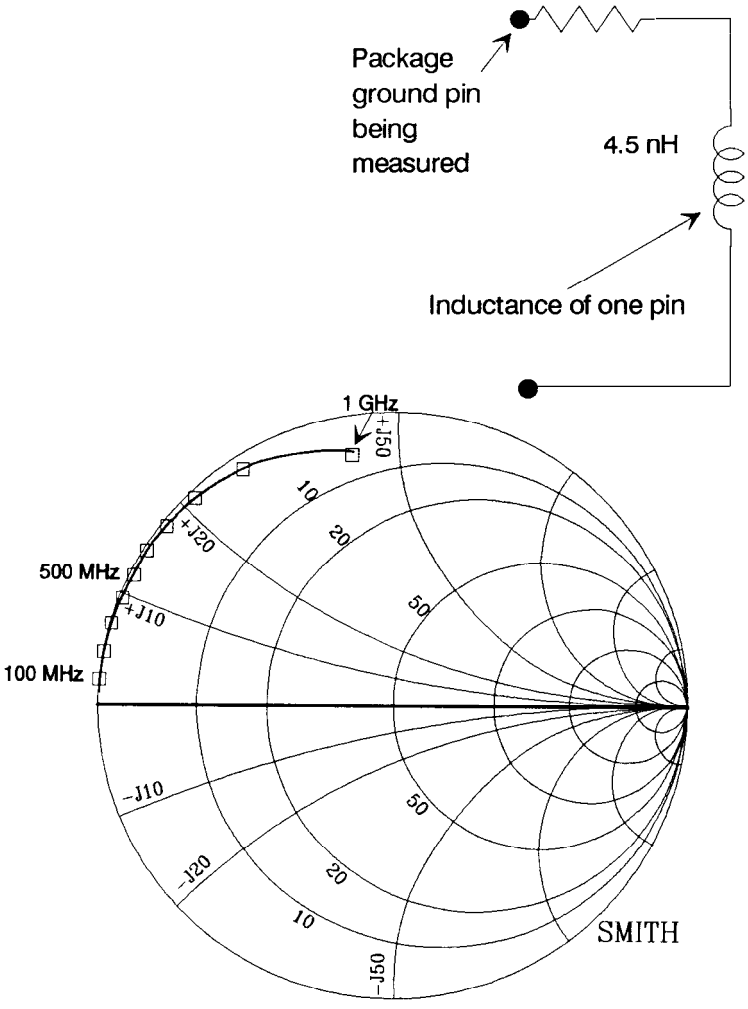
In this case

$\lambda/2$: = (1.75 inches)/3.45 ps/mil) = 0.5 ns

or f = 1 GHz

which corresponds very closely to the measured value of 1.1 GHz. The other two resonances may be the other two VCC planes, coupled by the inductive pins, which may tune the resonances slightly, or it may be the VTT and VEE planes resonated in sequence.

Recall that what is being measured in figure 20 and modeled in figure 28 is the inductance of basically one VCC pin, and the VCC plane resonance. Given that there are 15 VCC pins in this package, the resultant equivalent VCC plane inductance circuit is shown figure 29. This model is expected to be accurate through 1.1 GHz, the frequency at which the first resonance occurs. It will be a subject of a future paper to model this resonance. Note that when an actual die is placed in the cavity, bond wires will connect the VCC pads to the VCC traces, and the composite inductance of these bond wires should be added in series 0.5 Ohms



• 100 MHz Steps

Figure 28 Proposed initial model for VCC plane (ground) inductance measurement (a), up to the first resonance frequency, and the calculated response of this model (b). Compare with measurement in figure 20. Note this is the model of one VCC pin and the VCC plane.

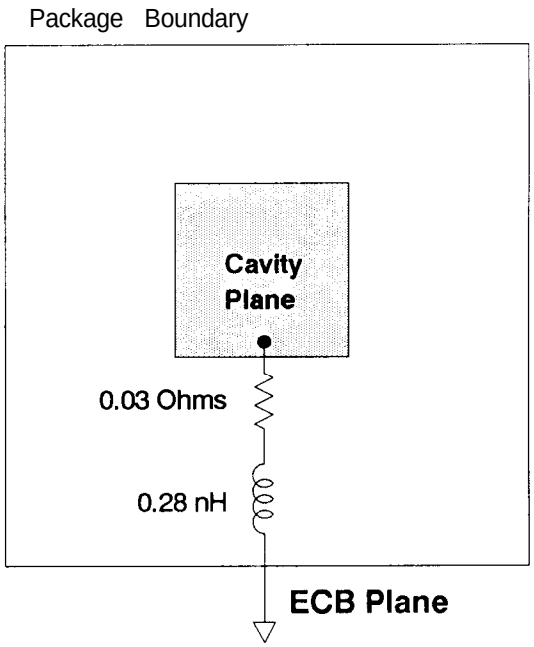


Figure 29 Proposed VCC plane (ground) inductance equivalent circuit, modeling up to the first resonance frequency. This model does not include the inductance, due to bond wires from die to VCC traces.

Ground plane resonance is a fundamental performance limit of a package. What occurs at resonance is that the plane is no longer equipotential, but rather is acting like an antenna, radiating to the dielectric, and to all signal traces on the package. Given that this resonance occurs at approximately 1 GHz, and using the analog to digital bandwidth rule of thumb of 10:1 this would imply a maximum clock rate for this package of 100 MHz, for *ground plane resonance limitations only.*

The transmission measurements of figures 23, 24, and 25 illustrate the problem of impedance mismatch. Looking at figure 25, the transmission response (S_{21}), the transmission is fairly flat through 0.8 GHz, then drops to -10 dB (32%) at 1.5 GHz. At this same frequency S_{11}

peaks, indicating the energy is being reflected, so the transmission loss at 1.5 GHz is not caused by series losses in the signal traces, but rather by reflections at the discontinuities where the impedances change value. This is verified by modeling this effect by using a linear modeling program, with results shown in figure 30. As shown, this effect is generally modeled using lossy transmission lines, particularly in S_{11}. S-parameter S_{21}, however, is not modeled as well, because the VCC plane resonance is not included. The transmission data indicates reasonable performance up to 0.8-1.0 GHz.

The cross-coupling measurements also demonstrate the effect of the VCC plane resonance. The cross coupling is 10% or less below 0.8 GHz, raising to 30% at 1.1 GHz, where the VCC plane resonates.

Fixturing for other packages

High-frequency characterization of digital IC packages is very new, so techniques are still in a state of development. Each package type that departs significantly from that discussed in this paper will require special consideration, Fortunately, products will soon be available to ease this problem. Cascade Microtech already supplies microwave probes, probe holders, probe stations, calibration substrates, microwave cables, and fittings and will soon be supplying Surrogate Chip" substrates (patent pending, fig. 31). GigaTest Labs will be supplying universal and custom PASlFx boards in standard materials and thickness. Hewlett-Packard, of course, supplies a whole range of network analyzers, as well as TDR instruments, which are designed to work with the Cascade Microtech calibration substrate constants.

Package characterization recommendations

Sequence of events

1. Fixture each package type for easy probing, using microwave probes.

2. Measure common-ground inductance first, because it is common to all other measurements.

3. Use TDR measurements for several signal traces, using a wide bandwidth for good spatial resolution, and select the basic model topology.

4. Measure S-parameters.

5. Optimize basic model with S-parameters. The model should include the first resonance, which will be the upper frequency limit of the model.

6. Verify model by comparing the calculated time domain response with measured time domain response, using a pulse generator.

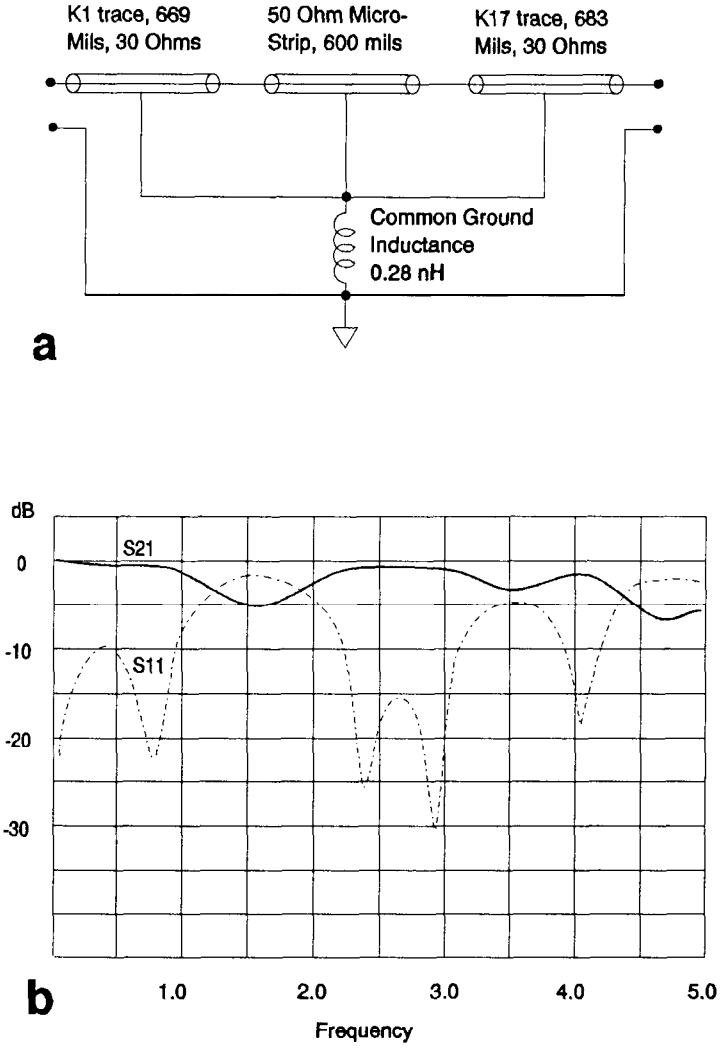


Figure 30 Linear model (a) of figure 25 data (series combination of signal trace K1, the transmission line, and signal trace K17) and the calculated response (b) of the model.

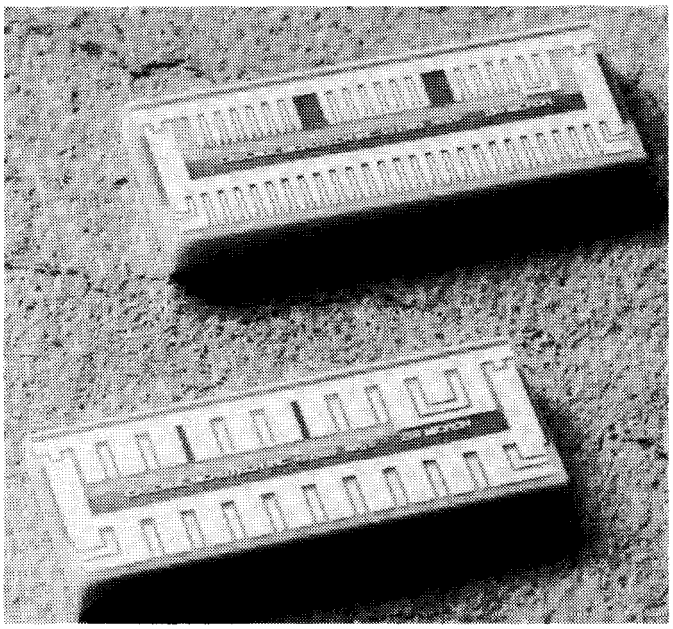


Figure 31 Surrogate Chip'" test substrates (patent pending) with calibration standards (top half) and short transmission lines where the probes land (bottom half). The short transmission lines are wire bonded to the traces to be measured, and to ground.

Conclusions

Accurate characterization of current digital IC packages requires instrumentation with analog bandwidths of 5 GHz for frequency domain measurements, and 20 GHz for high spatial-resolution TDR measurements. Complete package characterization involves measuring and modeling:

- common ground impedance
- cross coupling of the signal lines
- power supply impedance
- transmission loss of the signal lines

This paper has demonstrated:

1. Highly accurate measurements of a complex digital IC package can be easily and quickly performed using Cascade Microtech microwave wafer probes, the PASlFx board to adapt packages to microwave probes, and a Hewlett- Packard 8510B network analyzer.

2. Data obtained from these measurements can be used to optimize selected models, using various linear and nonlinear optimizing programs,

3. Ground plane resonances were measured at 1.1 GHz and above. These resonances define a package upper frequency limit, which would not be detected by low-frequency measurement and modeling techniques.

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Acknowledgements

The authors wish to thank Sandeep Mirchandani of National Semiconductor for the packages used in this paper and for promoting the package characterization activity along with Dave Bellandi of Hewlett-Packard. The authors also with to thank Jerry Schappacher, Reed Gleason, and Keith Jones for their many suggestions.

Appendix A

Bandwidth requirements

A common question when measuring packaging is “how high in frequency should I measure my package to assure a required digital performance?” The most direct approach is to compute the Fourier expansion coefficients for a train of square waves and look at how each additional harmonic affects the risetime (fig. Al). This data can be linearly scaled for any arbitrary clock frequency as shown in figure A2. Note the assumptions here are (a) there is a symmetrical square-wave clock and (b) no phase shift as a function of frequency. In general, the expected risetime for a 100 MHz clock is about 0.5 ns, meaning that harmonic content to at least 900 MHz is required, and harmonic content to 1500 MHz would be desirable for a well-defined edge.

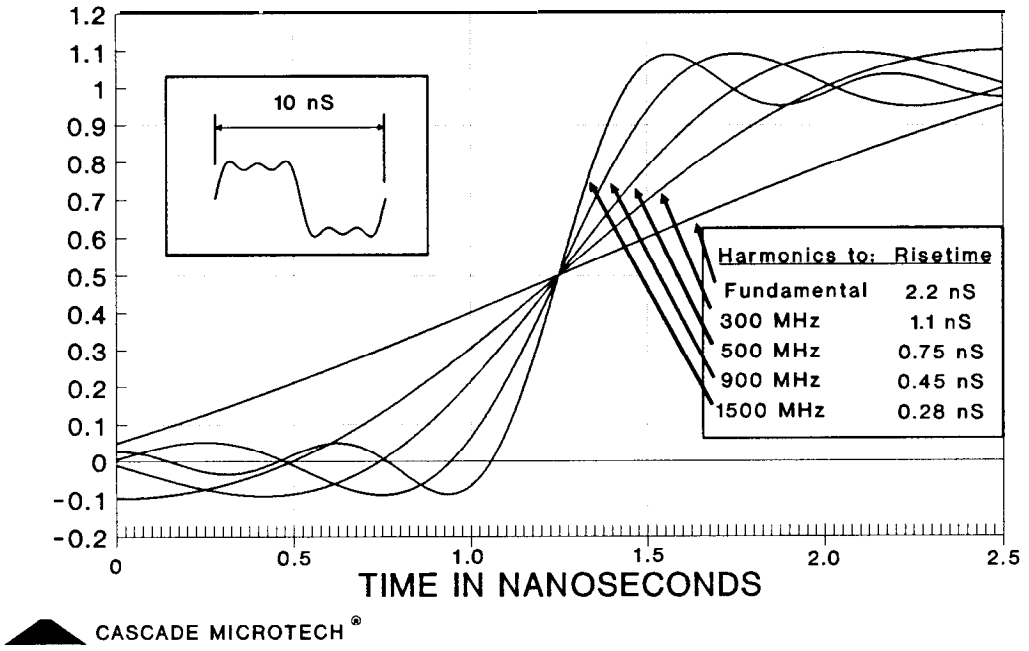

Figure A1 Risetime vs. harmonic content for a 100 MHz square wave.

Appendix A (continued) ➔

The guideline for general-use conditions is that a square-wave clock requires harmonics to 10 times the fundamental clock frequency. For package characterization purposes, use an analog bandwidth of 30 times the maximum expected digital clock frequency. This recommendation corresponds well with the recommendations in MIL-STD-883.[9] This extended bandwidth will allow exploration of various resonances and an assessment of how much margin the package has, and will result in more accurate package models. Use these guidelines when selecting equipment, including network analyzers, cables, probes, and other fixtures. Figure A1 is also useful for estimating maximum signal risetimes, given that you know the maximum analog bandwidth of a package. When using figure A1, keep in mind the above assumptions; if they are violated, the estimated risetimes for a given bandwidth will go down.

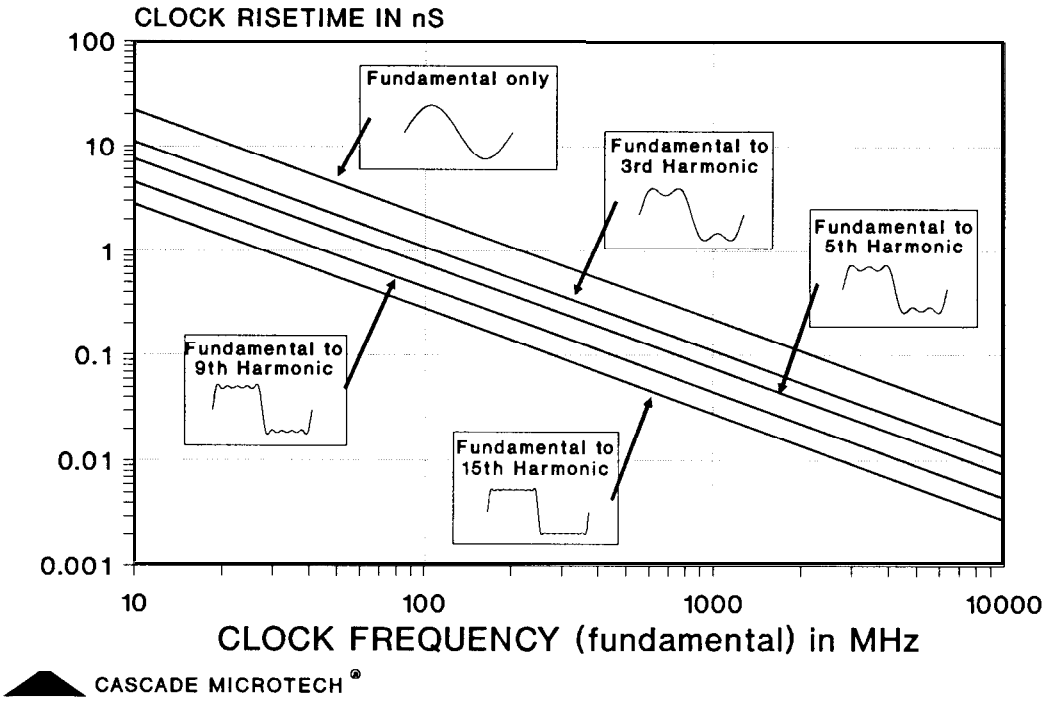

Figure A2 Bandwidth requirements for risetime performance, assuming square waves.