ECE 451
Packaging Technologies

Jose E. Schutt-Aine
Electrical & Computer Engineering
University of Illinois
jesa@illinois.edu

System-Level Integration (Microelectronic Packaging)

Semiconductor

* Unprecedented Innovations in CMOS, Si-Ge,Copper Wiring
* Fundamental technical Limits

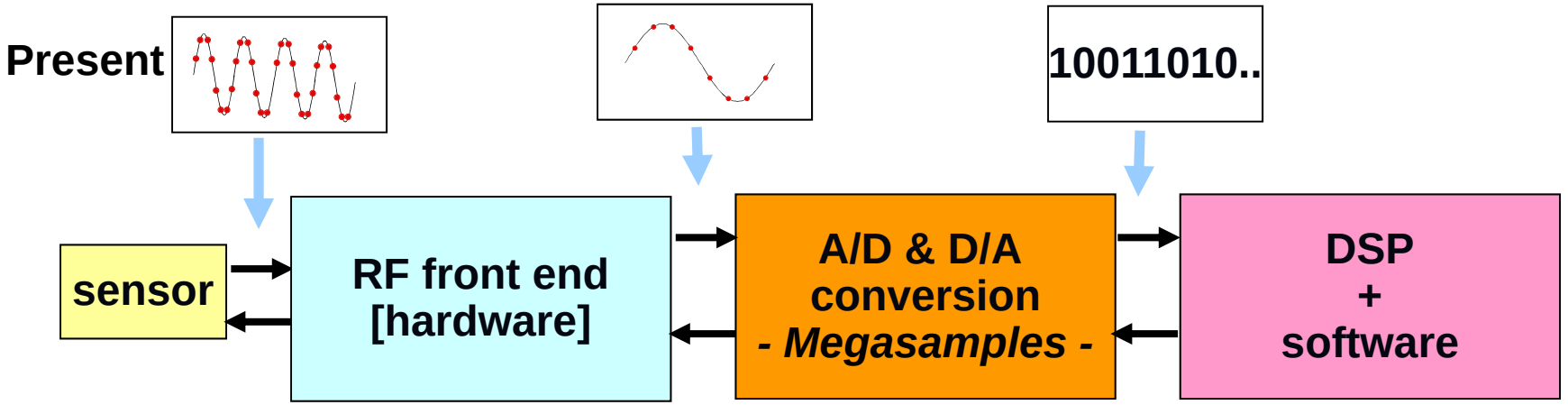
Electronic Systems

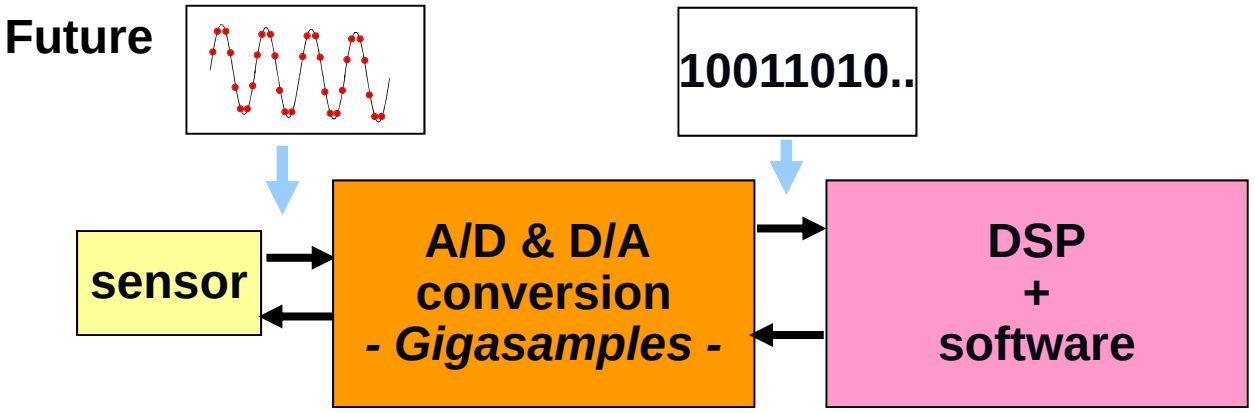
* Computers, telecom & Consumer Products Merge
* Portable, Wireless, & Internet Accessible
* Very Low Cost & Very High Performance

Microelectronic Packaging

* High Cost, Low Performance, Low Reliability
* Lack of Skilled Human Resources

Early Conversion to Digital Domain

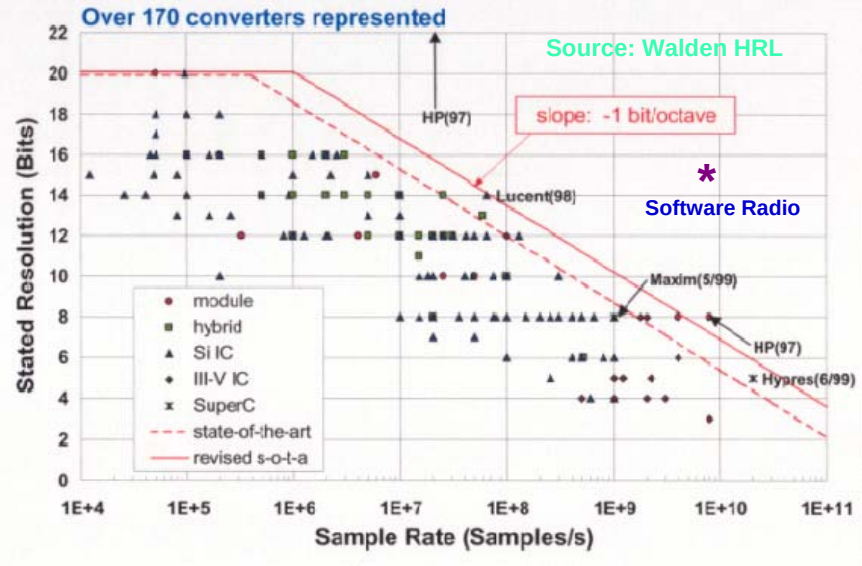




Advantages

- Reconfigurability
- Moore's law
- Lower power
- Better SI
- Smaller size
- Higher bandwidth

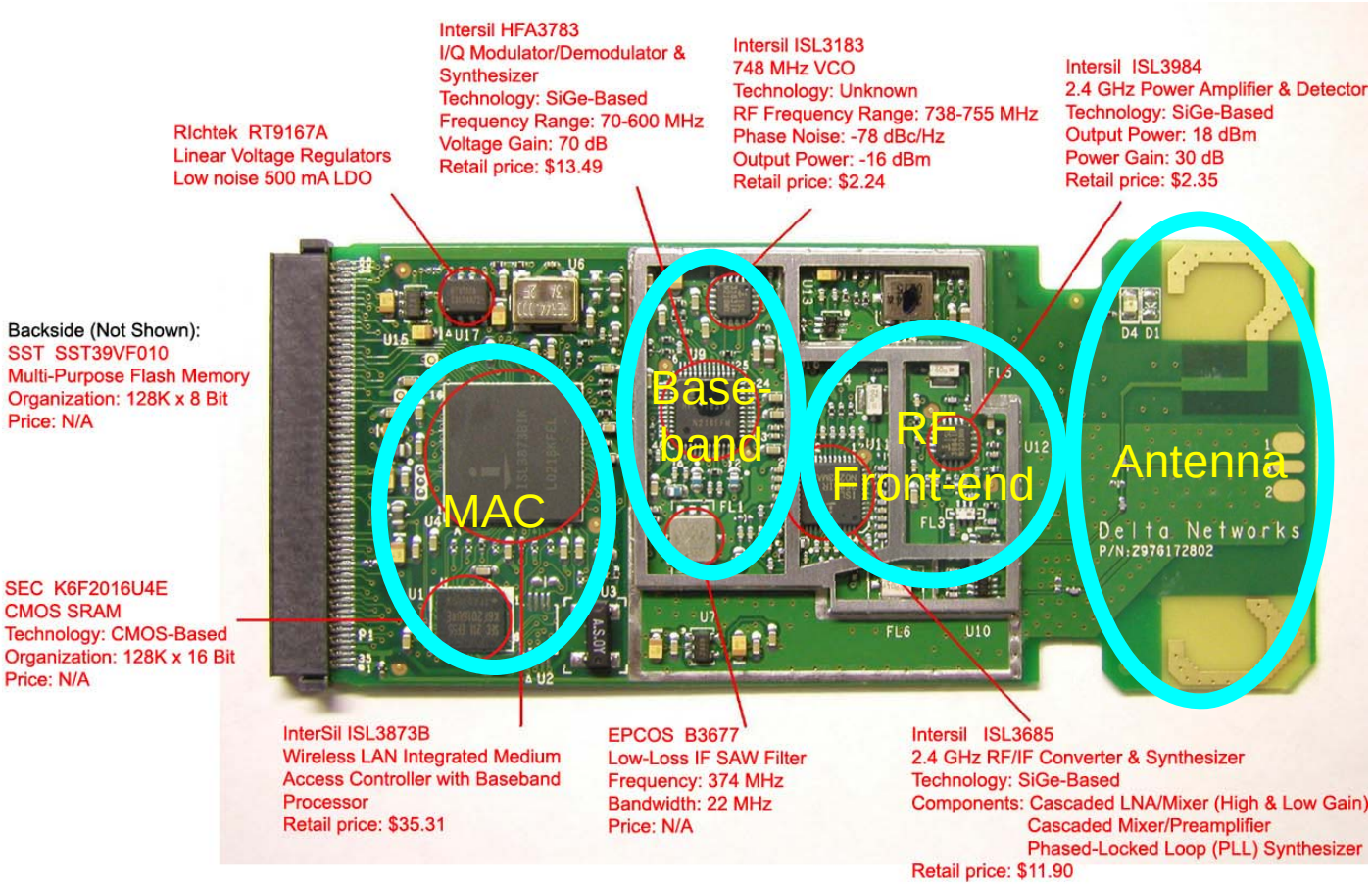
ADC Requirements



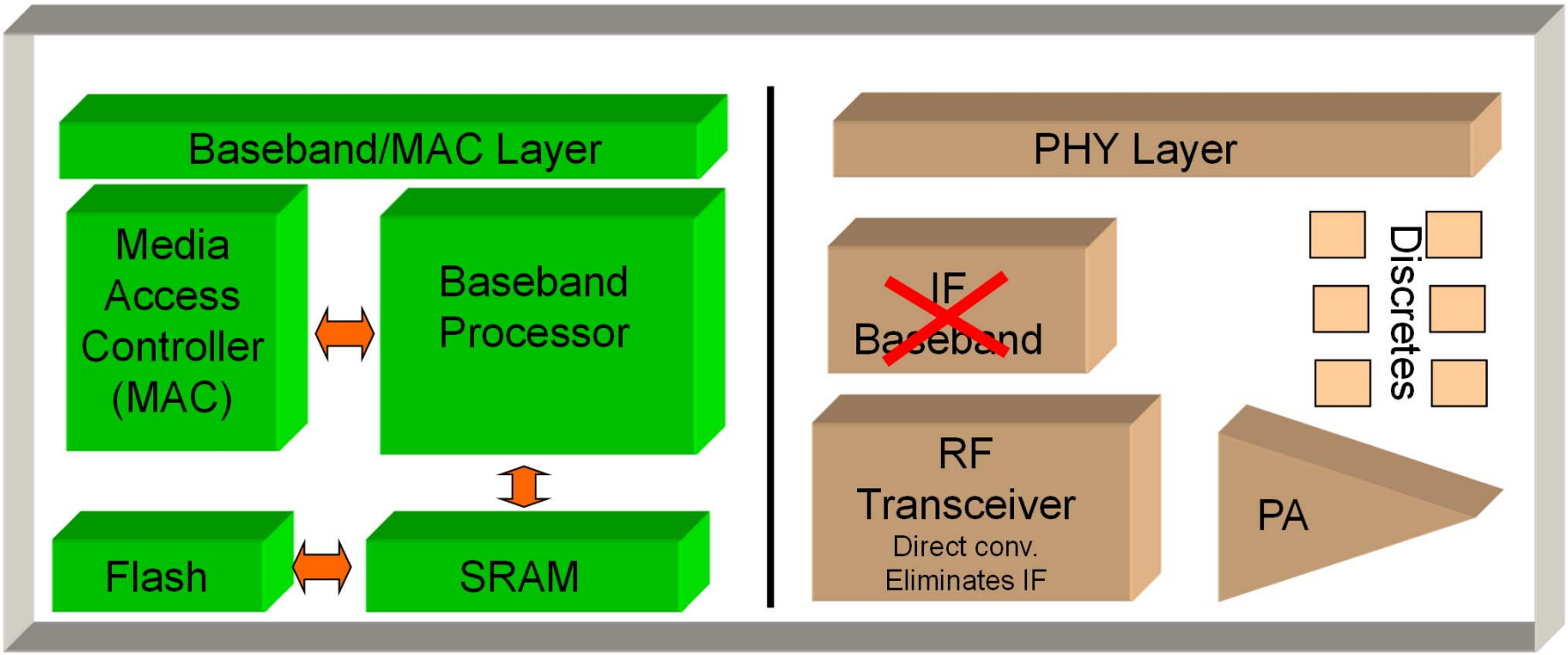
State-of-the art A/D Converters

- Sampling speed > 5GSamples/s
- Resolution: N > 14 bits
- Dynamic range > 60 dB
- Power dissipated < 5W
- SNR(dB) = 6.02N+1.76
- SFDR(dB) = 6.02N

802.11b WLAN Card Components



WLAN – Building Blocks



RF Front End Technologies

Product	PA	LNA	Mixer	VCO	Filter	Switch
Technology (Standard)	GaAs Si SiGe	Si	Si	Si GaAs	Si	Si GaAs
Technology (Alternate)	InP GaAs SiGe	InP GaAs	InP GaAs	InP GaAs	MEMS	InP GaAs MEMS
Criterion	PAE, linearity	Low power	Linearity, 1/f noise	1/f noise	High Q	Isolation, Insertion loss

Transistor Technologies

	Si Bipolar	GaAs MESFET	GaAs HBT	InP HBT
base resistance	high	-	low	low
transit time	high	-	low	low
Beta*Early voltage	low	-	high	high
col-subst capacitance	high	-	low	low
turn on voltage	0.8	-	1.4	0.3
thermal conductivity	high	-	low	medium
transconductance	50X	1	50X	50X
device matching	< 1 mV	> 10 mV	1 mV	1 mV
hysteresis or backgating	negligible	> 10 mV	negligible	negligible
breakdown voltage	< 10 V	> 8 V	> 10 V	low
fT (GHz)	30	100	100	160

Trends & Enabling Technologies

Materials/Processing

- RF CMOS, SiGe
- AlGaAs/GaAs, InGaP/GaAs
- Metamorphic GaAs
- InP SHBT, DHBT

Radio Architectures

- Polar vs Cartesian loop
- Direct Conversion
- Software Radio

CAD Tools

- Device behavioral models
- RF Time-domain tools
- Fast Solvers

Packaging

- Differential designs
- RF MEMS
- LTCC

Packaging Challenges

- Package is bottleneck to system performance
- Package cost is increasing percentage of system cost
- Package limits IC technology
- On-chip system can outperform package capability

Advantages of SOC

* Fewer Levels of Interconnections
* Reduced Size and Weight
* Merging of Voice, Video, Data,...

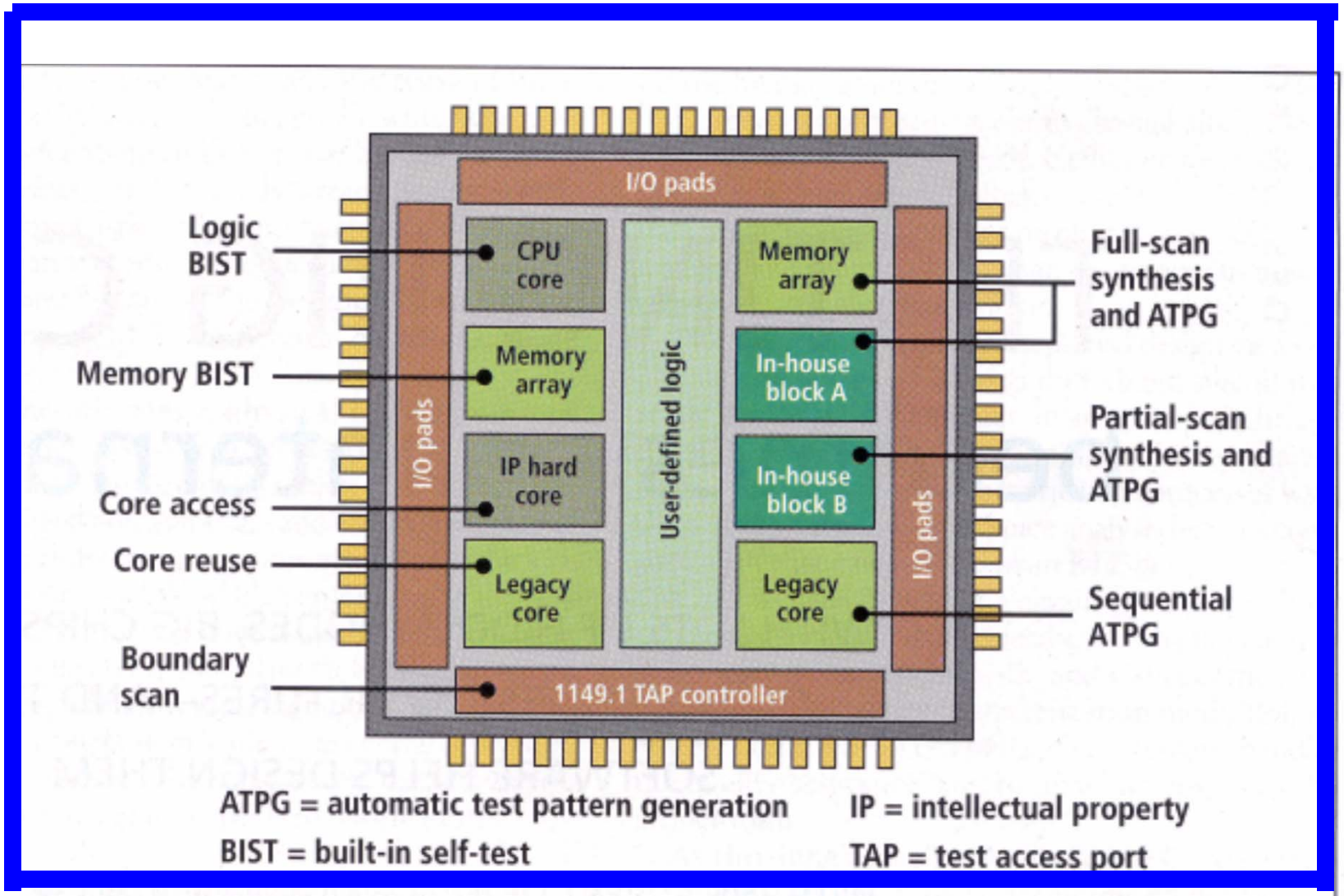
Arguments against SOC

* Challenges too Big
* Legal issues

Challenges for SOC

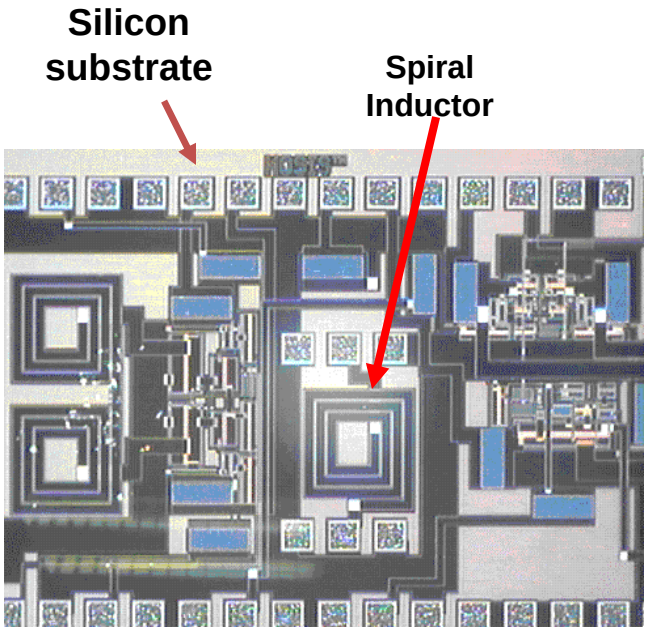
* Different Types of Devices
* Single CMOS Process for RF and Digital
* Design Methodology not available
* EDA Tools cannot handle level of complexity
* Intellectual Property
* Signal Integrity
* High-Power Requirements of PA

System on a Chip (SOC)



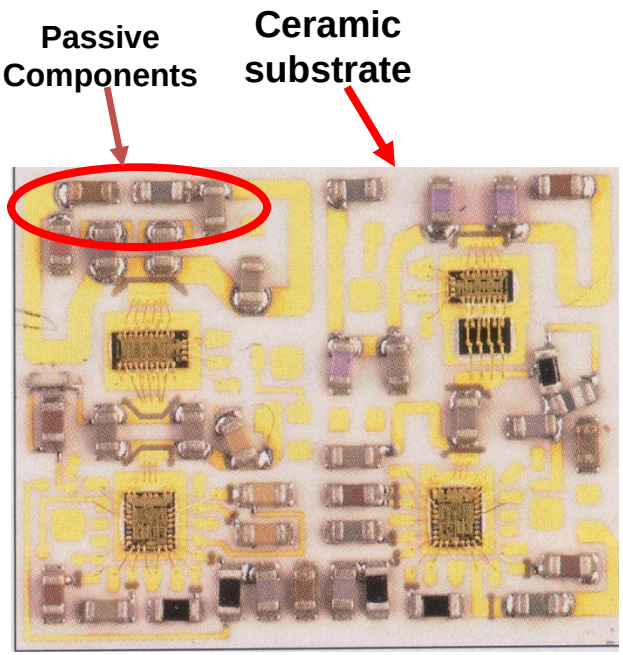
SOC vs SOP

System on Chip



Voltage Controlled Oscillator
(UIUC-CAD group – 1999)

System on Package

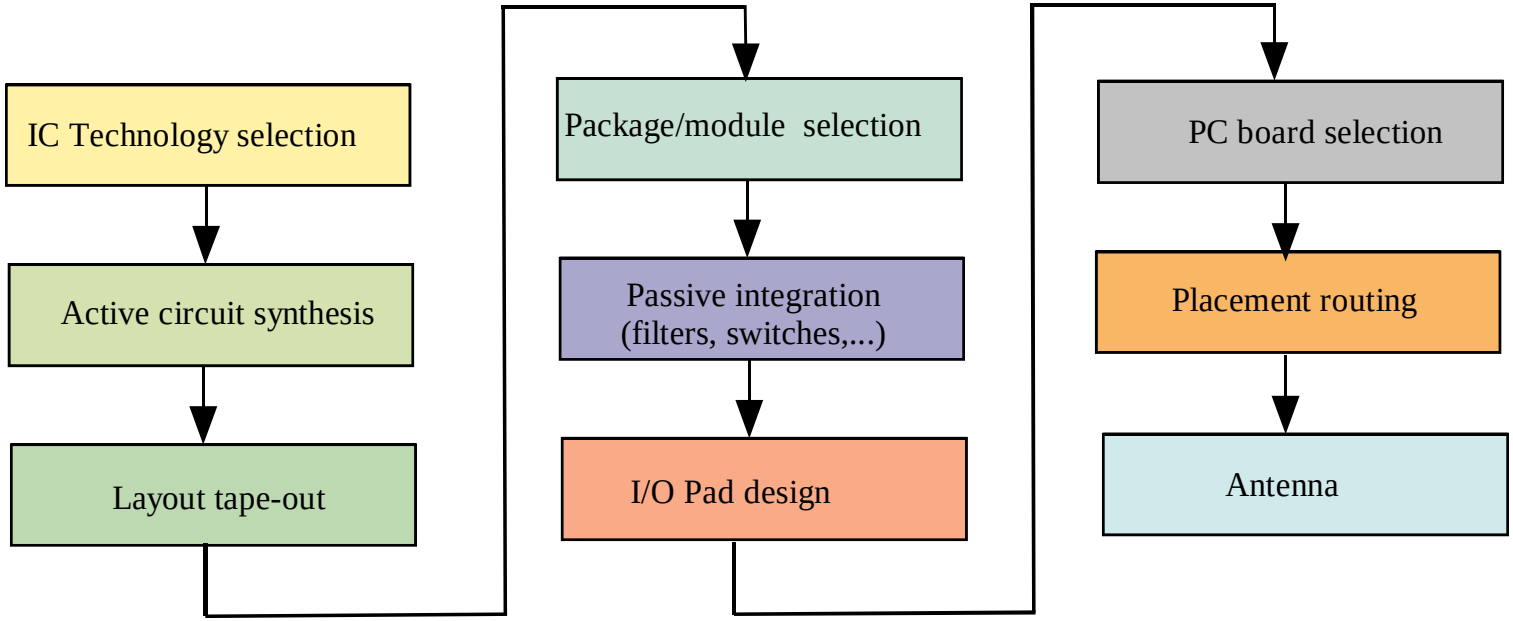


Triple-band GSM/EDGE Power Amp Module
(RF Design Magazine – 4/02)

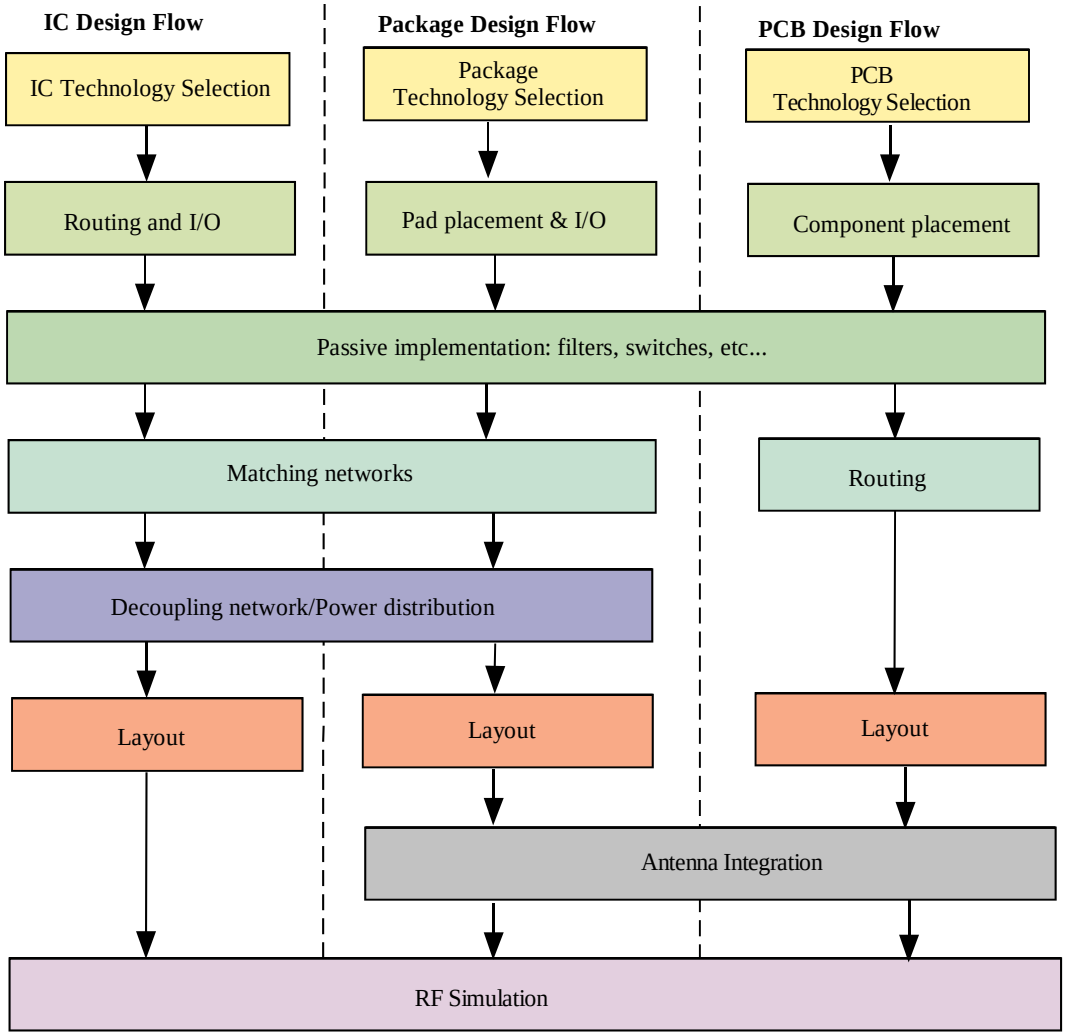
SOP vs SOC

	SOP	SOC
Low cost consumer products (<$200)	YES	YES
Portable products ($200-$2000)	YES	NO
Single processor products ($1-$5K)	YES	NO
High Performance Products (>5K)	YES	NO
Automotive and Space Applications	YES	NO

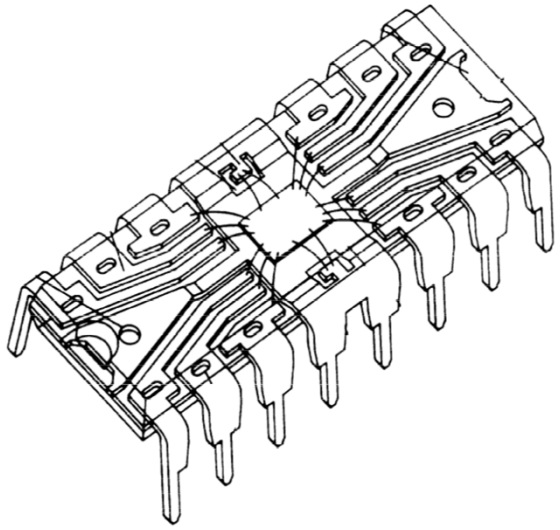
Traditional Design Flow



Co-Design Flow

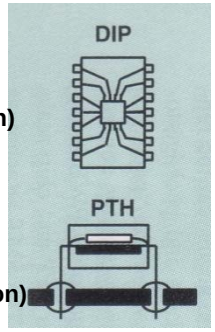
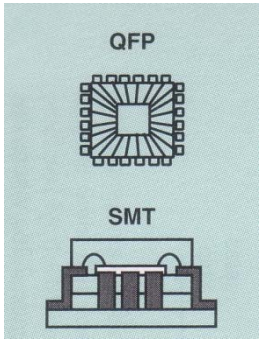
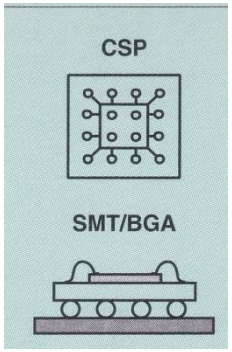
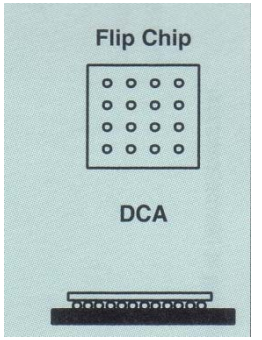


Dual-in-Line (DIP) Package



- Mounted on PWB in pin-through-hole (PTH) configuration
- Chip occupies less than 20% of total space
- Lead frame with large inductance

Package Types

	DIP	QFP	CSP	Flip Chip
Top View (showing chip topackage connection) / **Plane View** (showing package to board connection)				
Chip Size (mm × mm)	5 ×5	16 × 16	25 ×25	36 × 36
Chip Perimeter (mm)	20	64	100	144
Number of I/Os	64	500	1600	3600
Chip Pad Pitch (μm)	312	128	625	600
Package Size (in × in)	3.3 × 1.0	2.0 × 2.0	1.0 × 1.0	1.4 × 1.4
Lead Pitch (mils)	100	16	25	24
Chip Area (mm^2)	25	256	625	1296
Feature Size (μm)	2.0	0.5	0.25	0.125
Gates/Chip	30K	300K	2M	10M
Max Frequency (MHz)	5	80	320	1280
Power Dissipation (W)	0.5	7.5	30	120
Chip Pow Dens (W/cm^2)	2.9	4.8	9.3	2.0
Pack Pow Dens (W/cm^2)	0.024	0.3	4.8	9.8
Supply Voltage (V)	5	3.3	2.2	1.5
Supply Current (A)	0.1	2.3	13.6	80

Substrate Materials

Material	Surface roughness (μm)	$10^4 \tan\delta$ at 10 GHz	ε_r	Thermal conductivity K ($W/cm^2/^oC$)	Dielectric strength (kV/cm)
Air (dry)	N/A	~0	1	0.00024	30
Alumina: 99.5% 96% 85%	 0.05-0.25 5-20 30-50	 1-2 6 15	 10.1 9.6 15	 0.37 0.28 0.2	 4×10^3 4×10^3 4×10^3
Sapphire	0.005-0.025	0.4-0.7	9.4,11.6	0.4	4×10^3
Glass, typical	0.025	20	5	0.01	-
Polyimide	-	50	3.2	0.002	4.3

Substrate Materials

Material	Surface roughness (μm)	$10^4 \tan\delta$ at 10 GHz	ε_r	Thermal conductivity K ($W/cm^2/^oC$)	Dielectric strength (kV/cm)
Irradiated polyolefin	1		2.3	0.001	~300
Quartz (fused) i.e. SiO2	0.006-0.025	1	3.8	0.01	10×10^3
Beryllia	0.05-1.25	1	6.6	2.5	-
Rutile	0.25-2.5	4	100		-
Ferrite/garnet	0.25	2	13-16	0.03	4×10^3

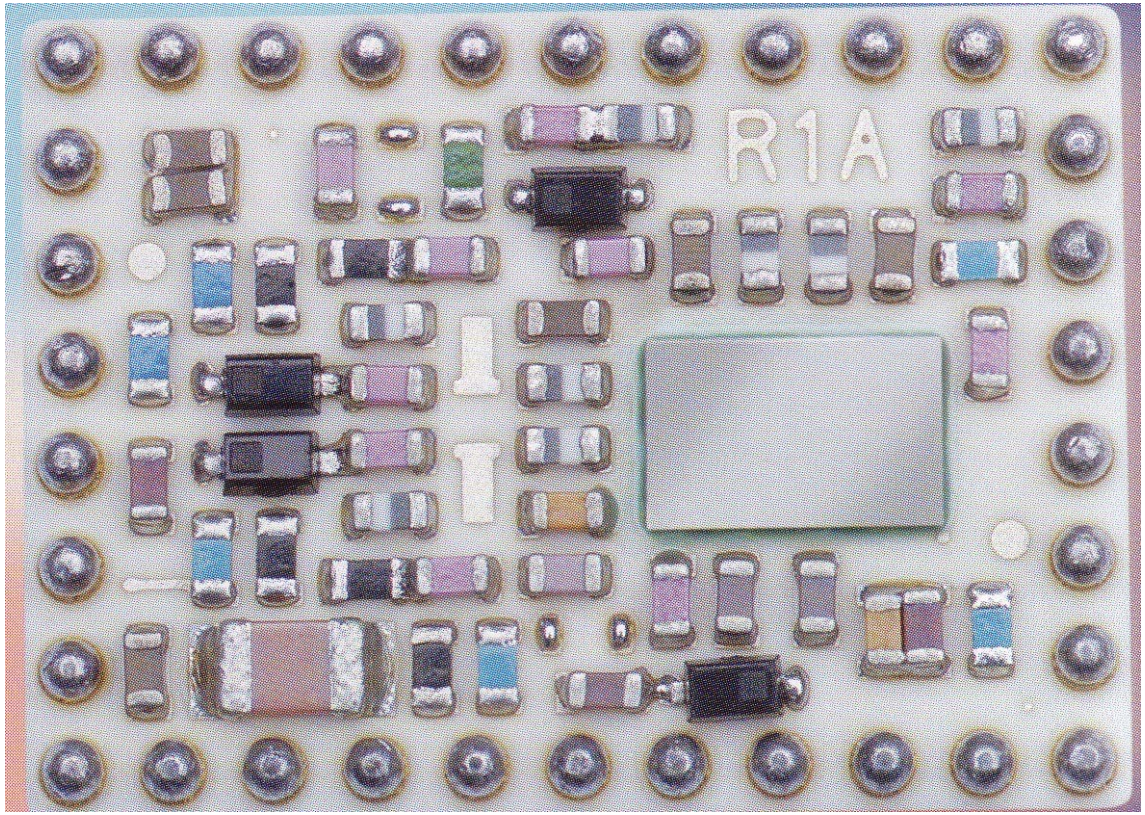
Substrate Materials

Material	Surface roughness (μm)	10^4 tanδ at 10 GHz	ε_r	Thermal conductivity K ($W/cm^2/^oC$)	Dielectric strength (kV/cm)
FR4 circuit board	~6	100	4.3-4.5	0.005	-
RT-duroid 5880	0.75-1 4.25-8.75	5-15	2.16-2.24	0.0026	-
RT-duroid 6010	0.75-1 4.25-8.75	10-60	10.2-10.7	0.0041	-
AT-1000	-	20	10.0-13.0	0.0037	-
Cu-flon	-	4.5	2.1	-	-

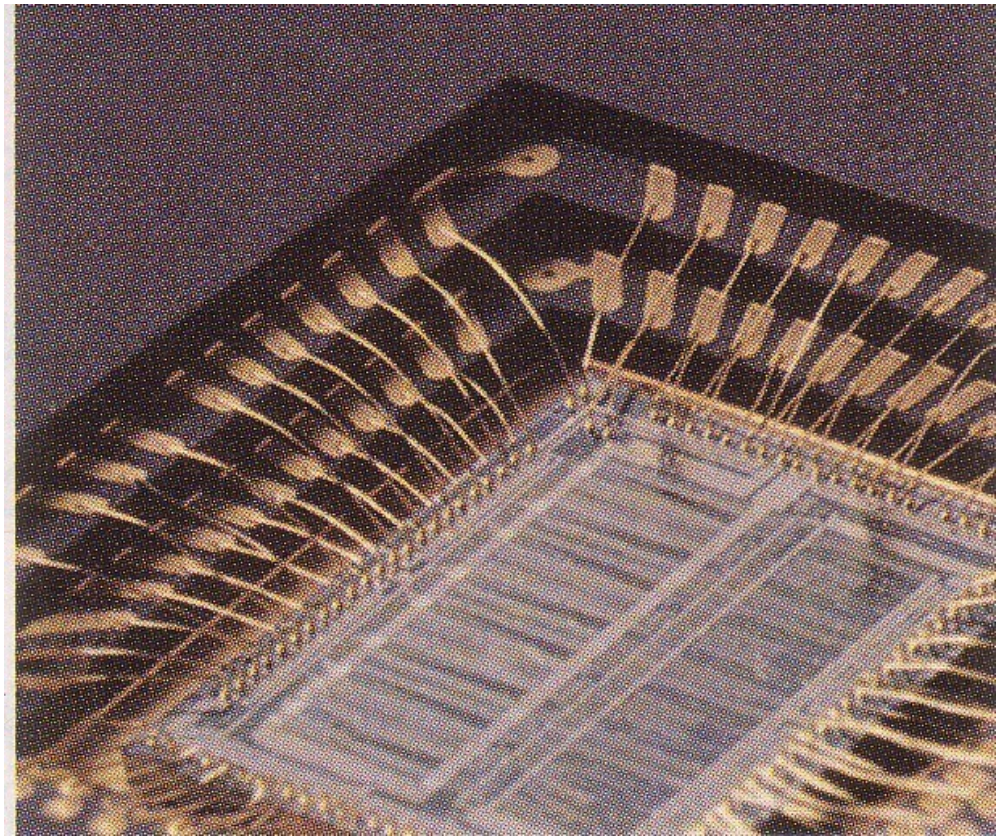
Substrate Materials

Material	Surface roughness (μm)	10^4 tanδ at 10 GHz	ε_r	Thermal conductivity K ($W/cm^2/^oC$)	Dielectric strength (kV/cm)
Si (high resistivity)	0.025	10-100	11.9	0.9	300
GaAs	0.025	6	12.85	0.3	350
InP	0.025	10	12.4	0.4	350
SiO2 (on chip)	-	-	4.0-4.2	-	-
LTCC (typical green tape 951)	0.22	15	7.8	3	400

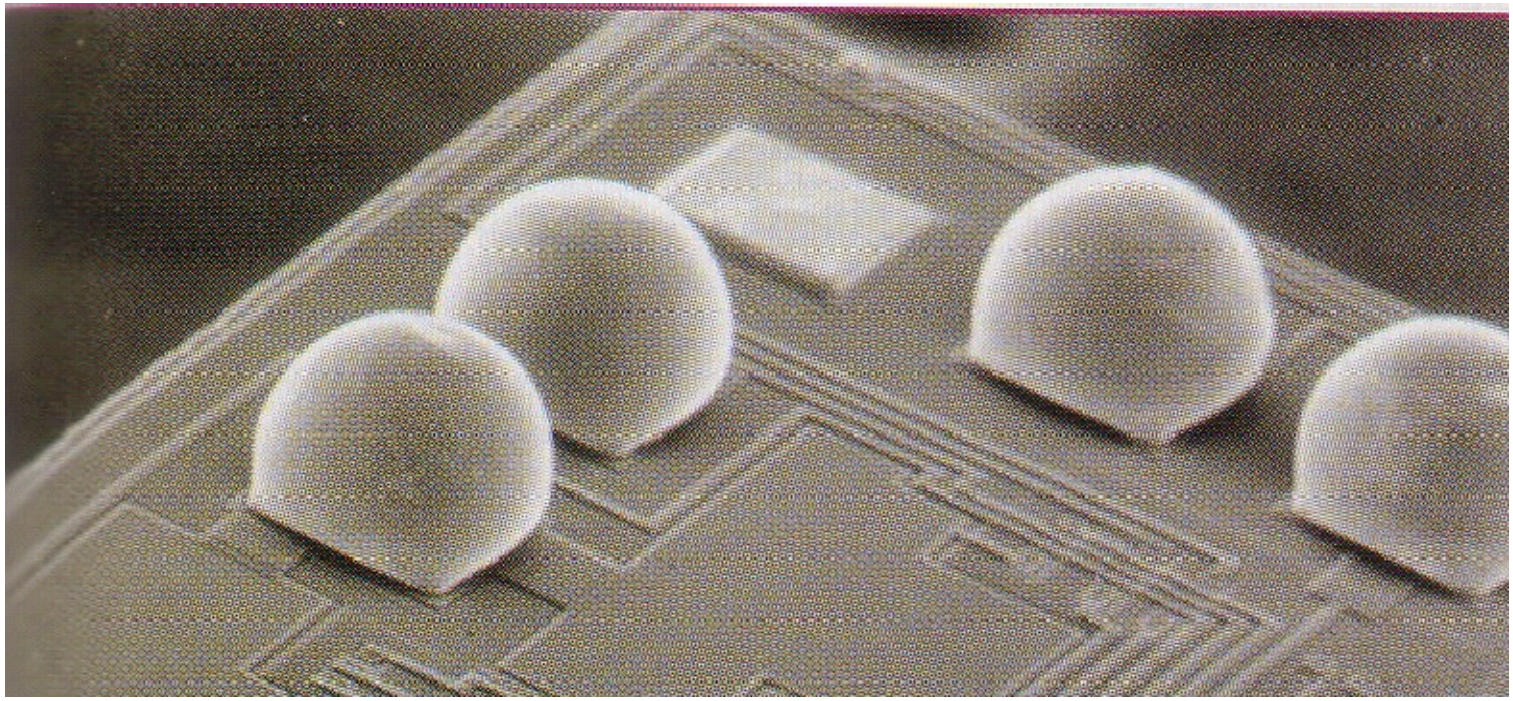
Ceramic Substrate



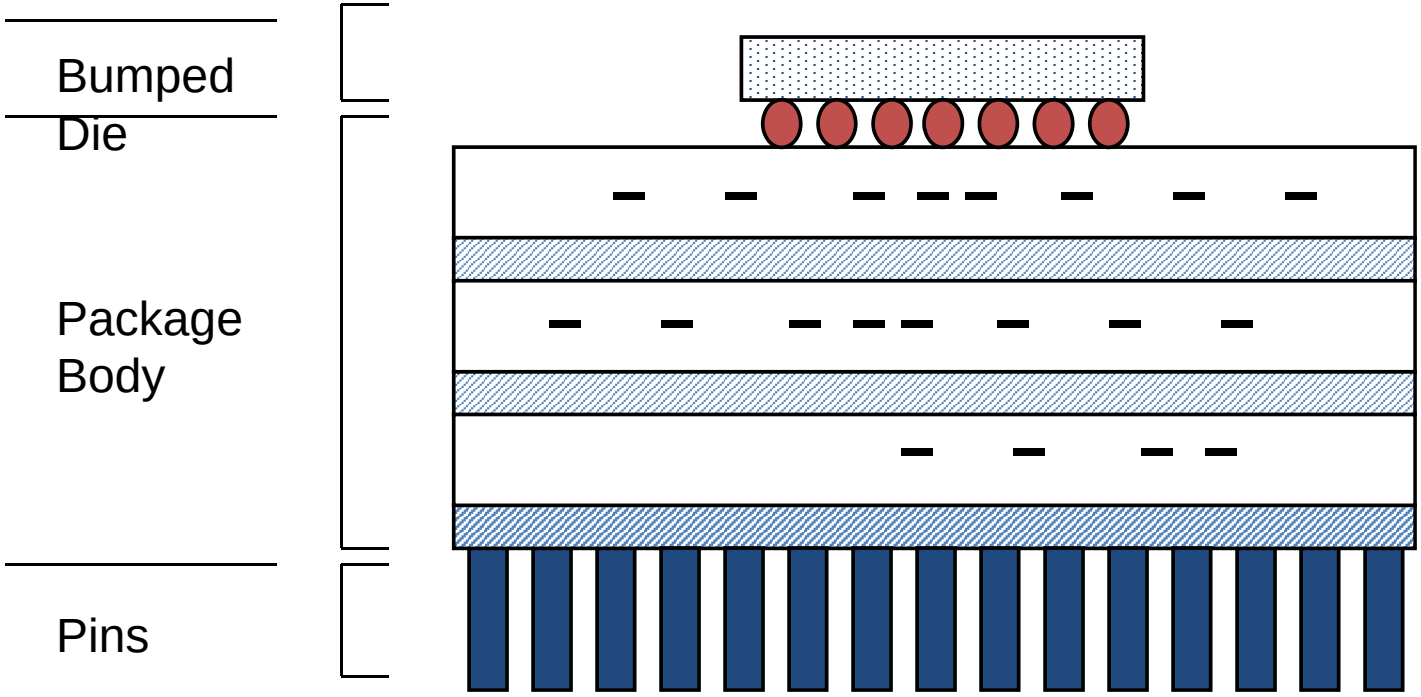
Stacked Wire Bonds



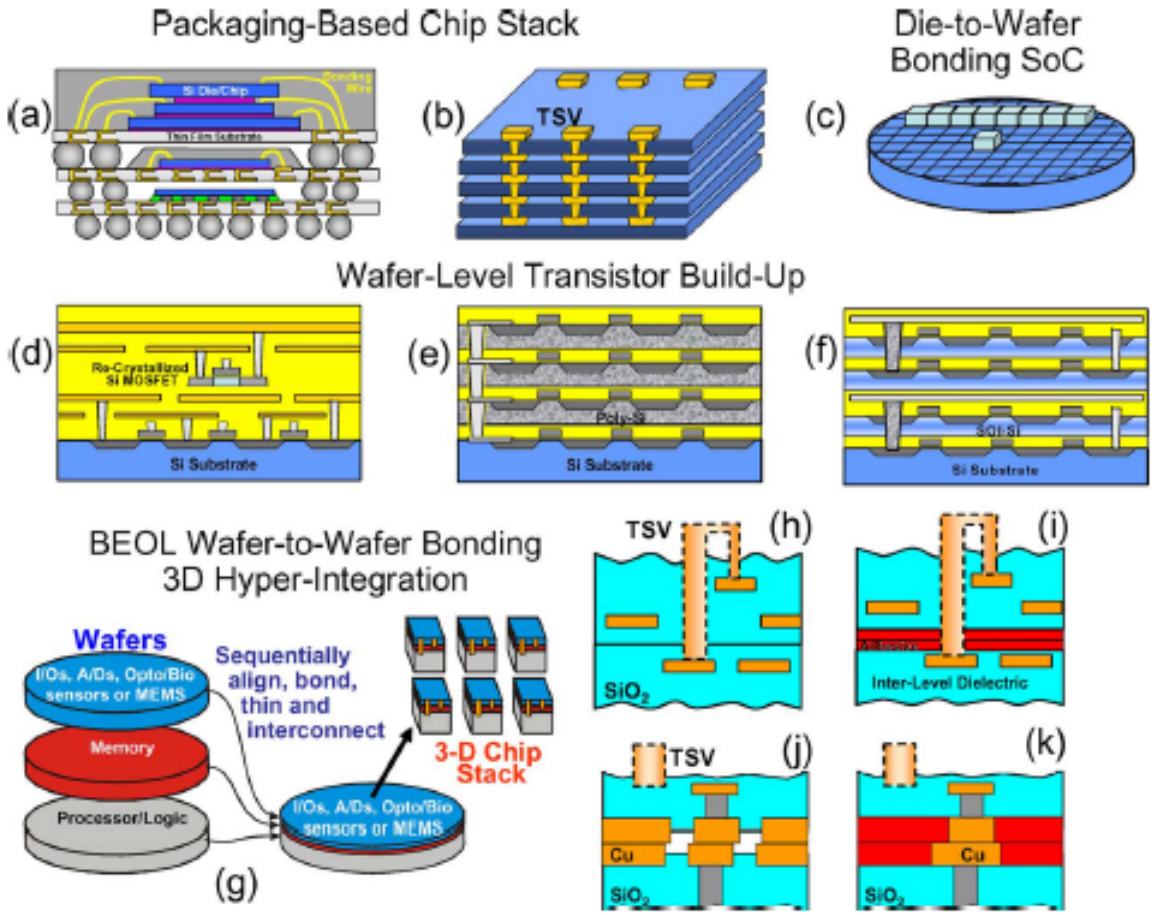
Ball Bonding for Flip Chip



Flip Chip Pin Grid Array (FC-PGA)

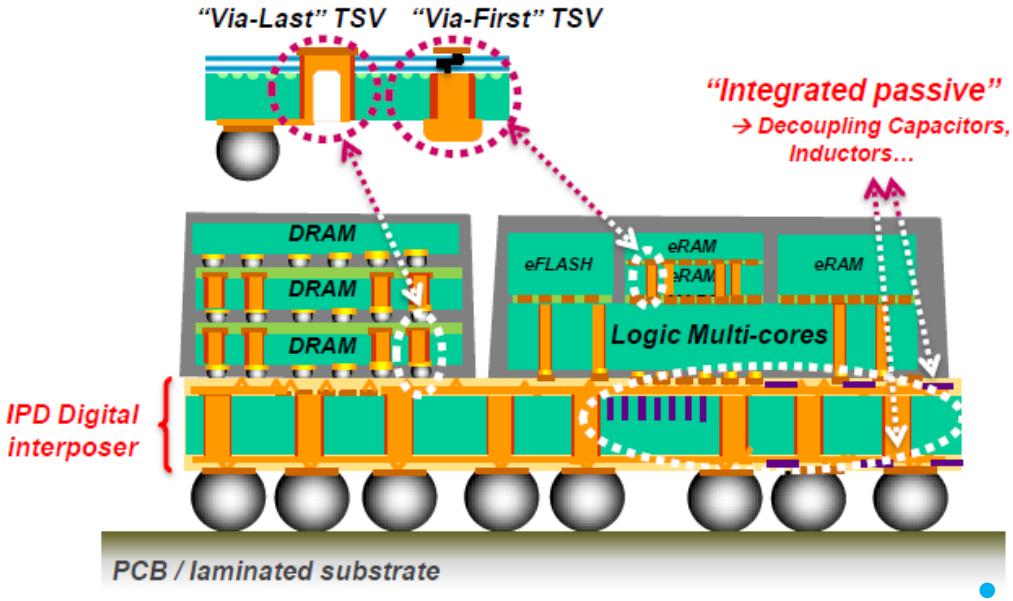


3D Packaging



Source: Jian-Qiang Lu, "3-D Hyperintegration and Packaging Technologies for Micro-Nano Systems", Proceedings of the IEEE, pp 18-30, Vol. 97, No. 1, January 2009.

3D Packaging



Source: Yole Report 2009.

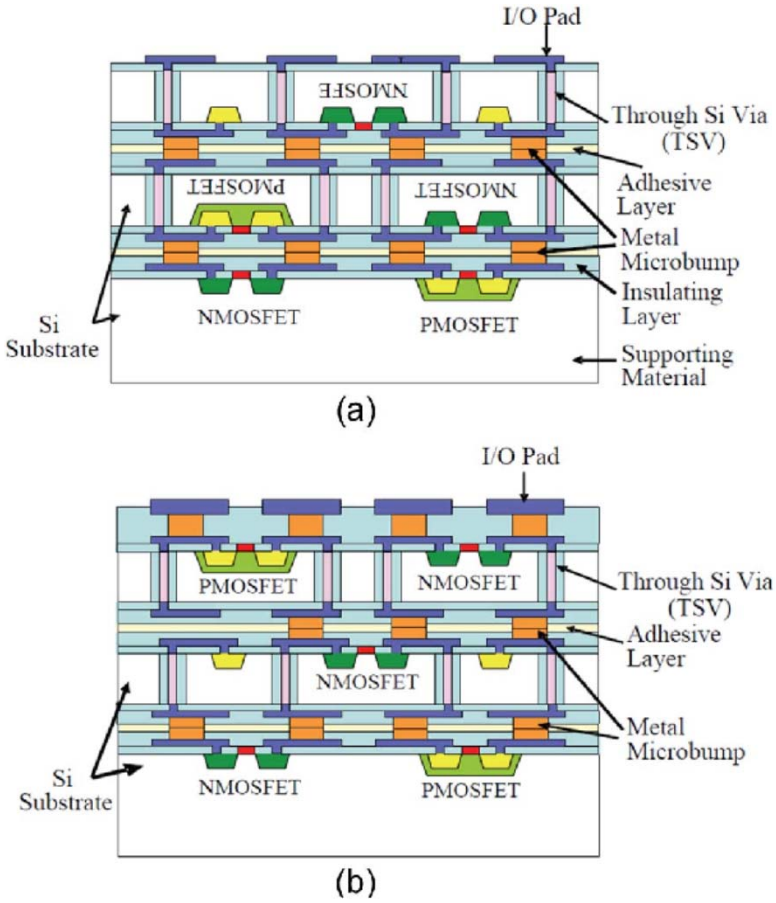
Key concepts

- Wires
  - shorter
  - lots of it
- Heterogeneous integration
  - Analog and digital
  - Technologies (GaAs and Si?)

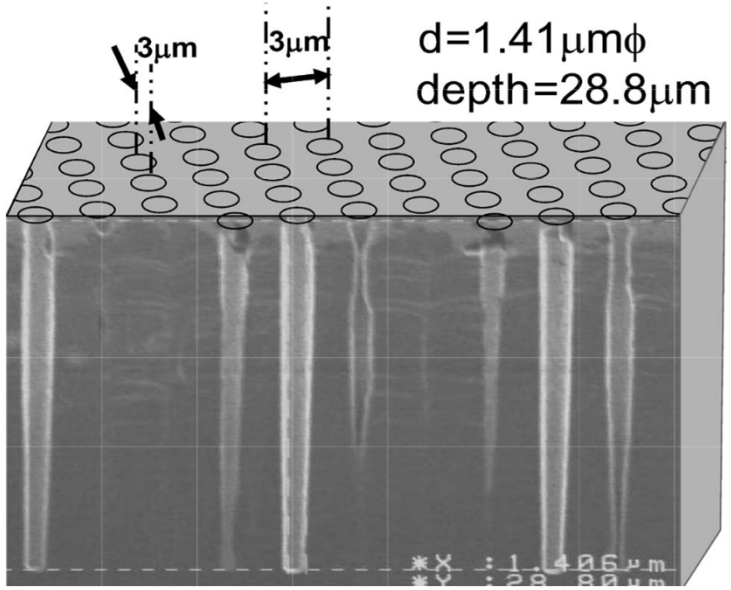
3D Industry

- Samsung
  - 16Gb NAND flash (2Gx8 chips) Wide Bus DRAM
- Micron
  - Wide Bus DRAM
- Intel
  - CPU + Memory
- OKI
  - CMOS Sensor
- Xilinx
  - 4 die 65 nm interposer
- Raytheon/Ziptronix
  - PIN Detector Device
- IBM
  - RF Silicon Circuit Board/ TSV Logic & Analog
- Toshiba
  - 3D NAND

Through-Silicon Vias



Mitsumasa Koyanagi," High-Density Through Silicon Vias for 3-D LSIs"
Proceedings of the IEEE, Vol. 97, No. 1, January 2009



From: M. Motoshi, "Through-Silicon Via, Proc. of IEEE Vol. 97, No. 1, January 2009.

TSV Density: $10/cm^2$ - $10^8/cm^2$

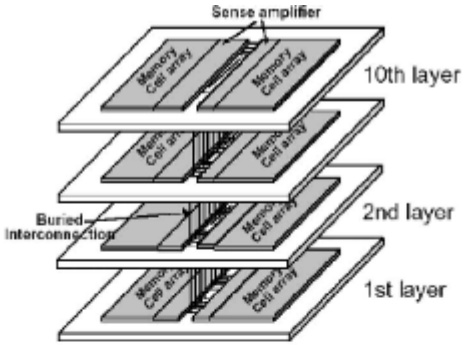
Through-Silicon Vias (TSV)

Advantages

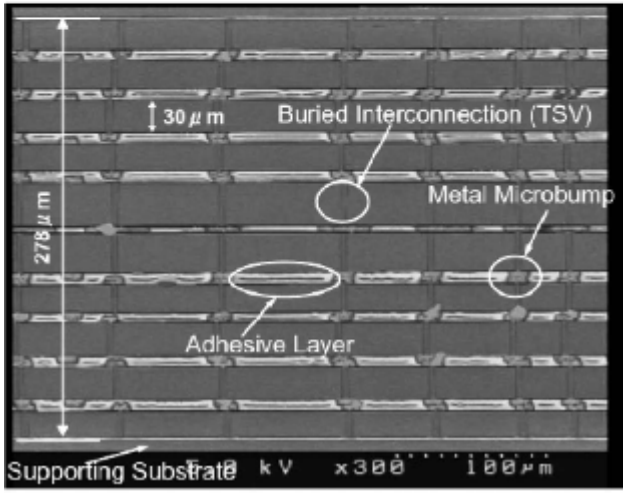
- Make use of third dimension
- several orders of magnitude (10/cm^2 to 10^8/cm^2)
- Minimize interconnection length
- More design flexibility

Issues

- **3D Infrastructure & supply chain**
- **I/O Standardization**
- **EMI**
- **Thermal management and reliability**



(a)



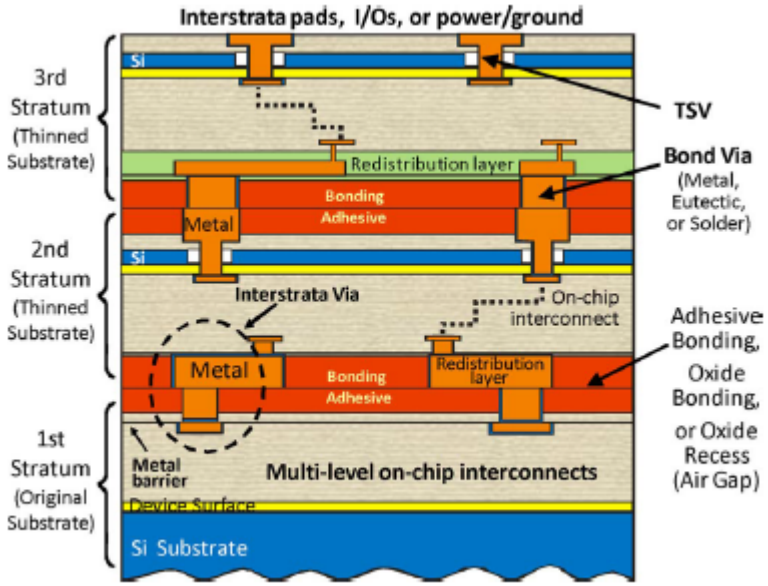
(b)

From Koyanagi et al., IEEE Proceedings, Feb 2009

TSV Pitch

TSV Pitch ≠ Area / Number of TSVs

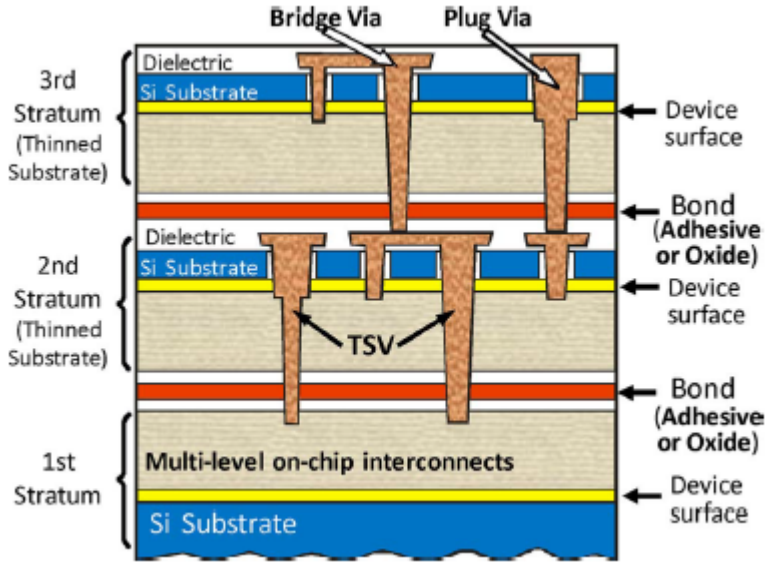
- TSV pitch example
  - 1024 bit busses require a lot of space with larger TSVs
  - They connect to the heart and most dense area of processing elements
  - The 45nm bus pitch is ~100 nm; TSV pitch is > 100x greater



Source: Jian-Qiang Lu, "3-D Hyperintegration and Packaging Technologies for Micro-Nano Systems", Proceedings of the IEEE, pp 18-30, Vol. 97, No. 1, January 2009.

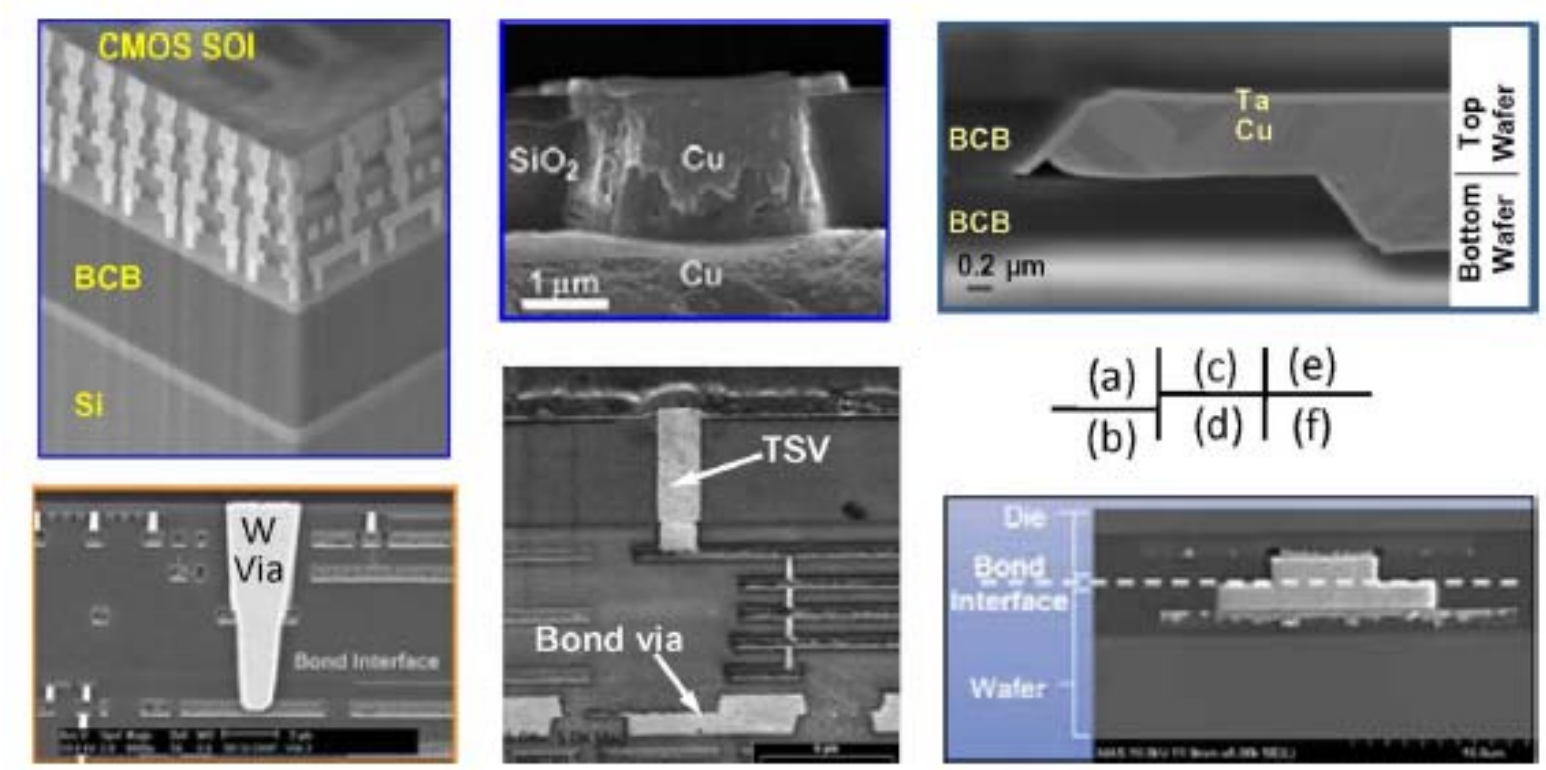
Through-Silicon Vias (TSV)

- Via First
- Via Last
- Via at Front End (FEOL)
- Via at Mid line
- Via at Back end (BEOL)



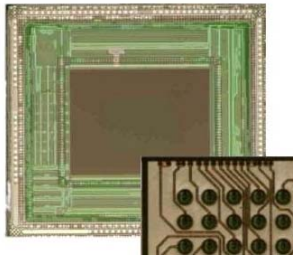
Source: Jian-Qiang Lu, "3-D Hyperintegration and Packaging Technologies for Micro-Nano Systems", Proceedings of the IEEE, pp 18-30, Vol. 97, No. 1, January 2009.

Through-Silicon Vias (TSV)



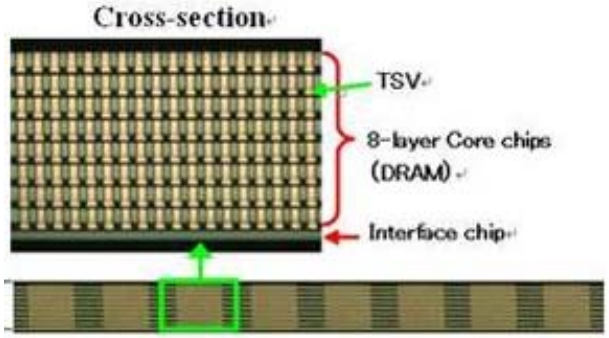
Source: Jian-Qiang Lu, "3-D Hyperintegration and Packaging Technologies for Micro-Nano Systems", Proceedings of the IEEE, pp 18-30, Vol. 97, No. 1, January 2009.

TSV-Based Products



STMicro CMOS image sensor in WLP/TSV package

Sony Video / DSC camera with BSI CMOS image sensors



Elpida's 3D TSV stacked DRAM memory

There are currently about 15 different 3D-IC pilot lines worldwide

3D-IC and TSV

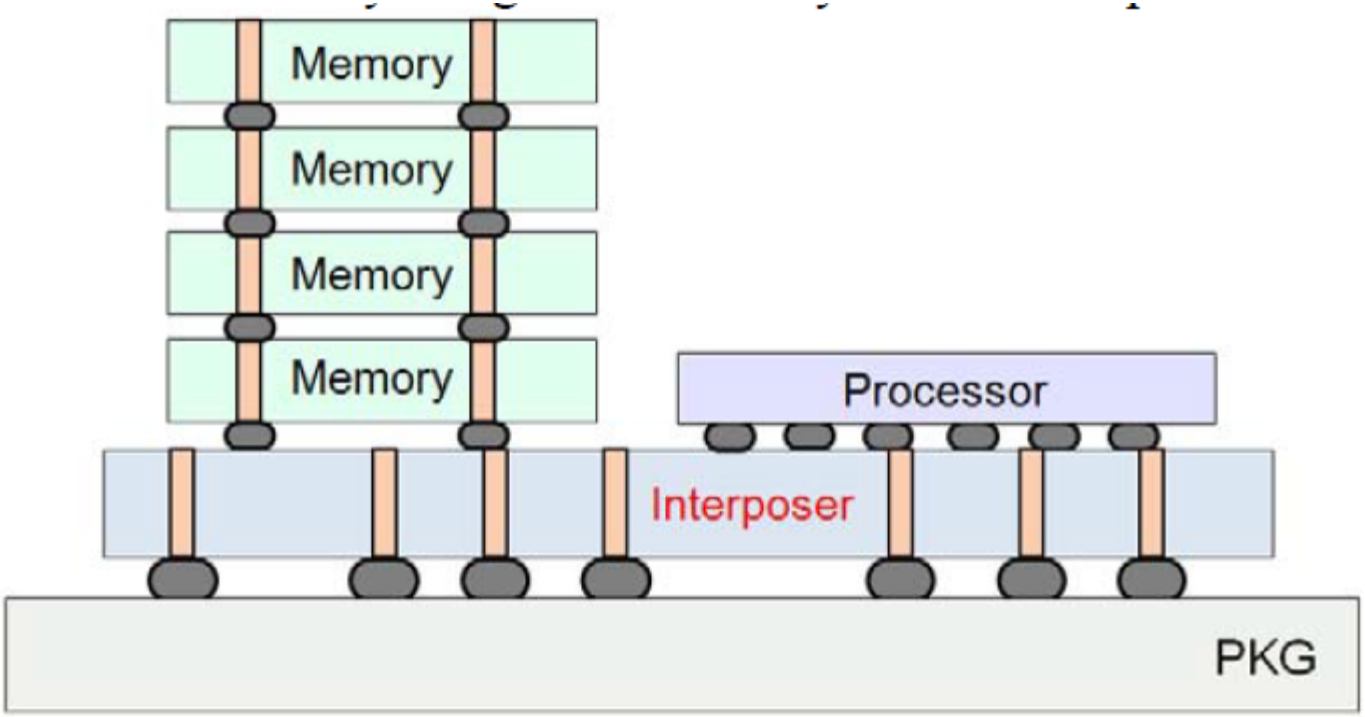
- Stacking of chips makes heat transfer through the z-direction difficult.
- Lossy silicon substrate makes coupling between adjacent TSVs strong.
- TSV noise can be easily coupled to the adjacent TSV through conductive silicon substrate
- 3D IC yields are much lower than 2D-IC
- Difficult to detect TSV and MOS failures

Solution: Use 2.5D integration

2.5D Integration

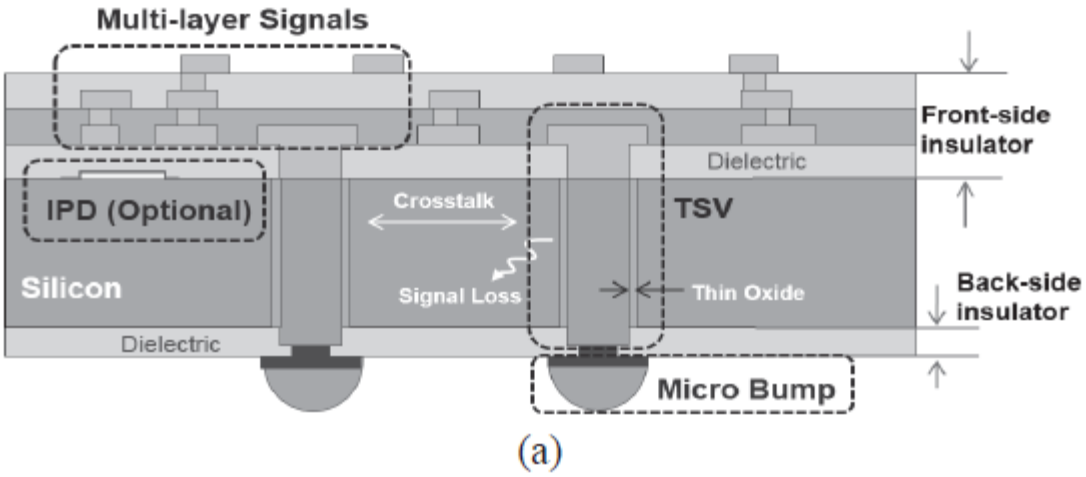
- 2.5D-IC emerges as a temporary solution
- In 2.5D-IC, several chips are stacked on interposer only homogeneous chip stacking is used.
- fine-pitch metal routing is necessary because it increase I/O counts
- For this purpose, an interposer is used where small width and small space metal routing is possible.
- Silicon substrate is usually used for an interposer because on-silicon metallization process is mature and fine-pitch metal routing is possible

Silicon Interposers



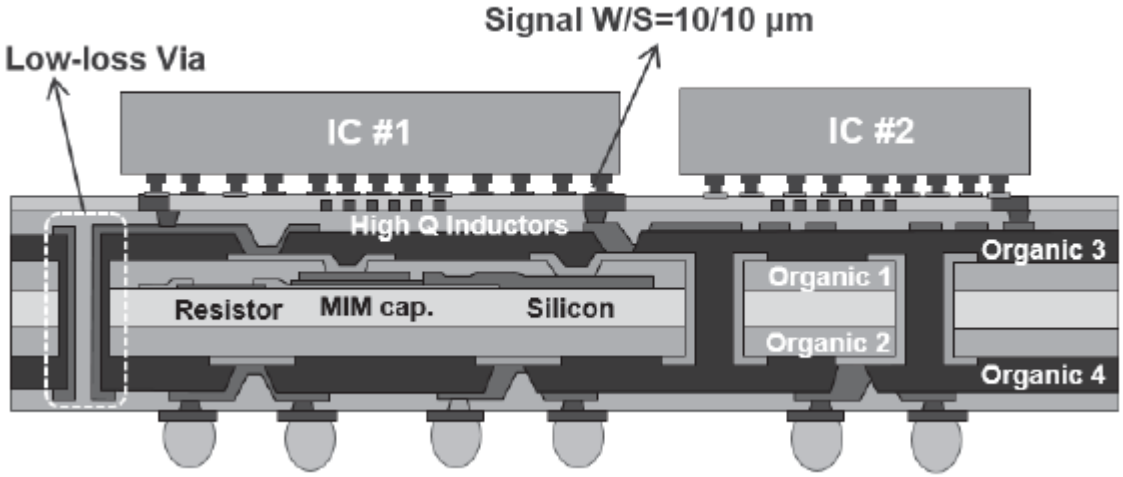
Source: J. Kim et al – DesignCon 2013.

Silicon Interposers



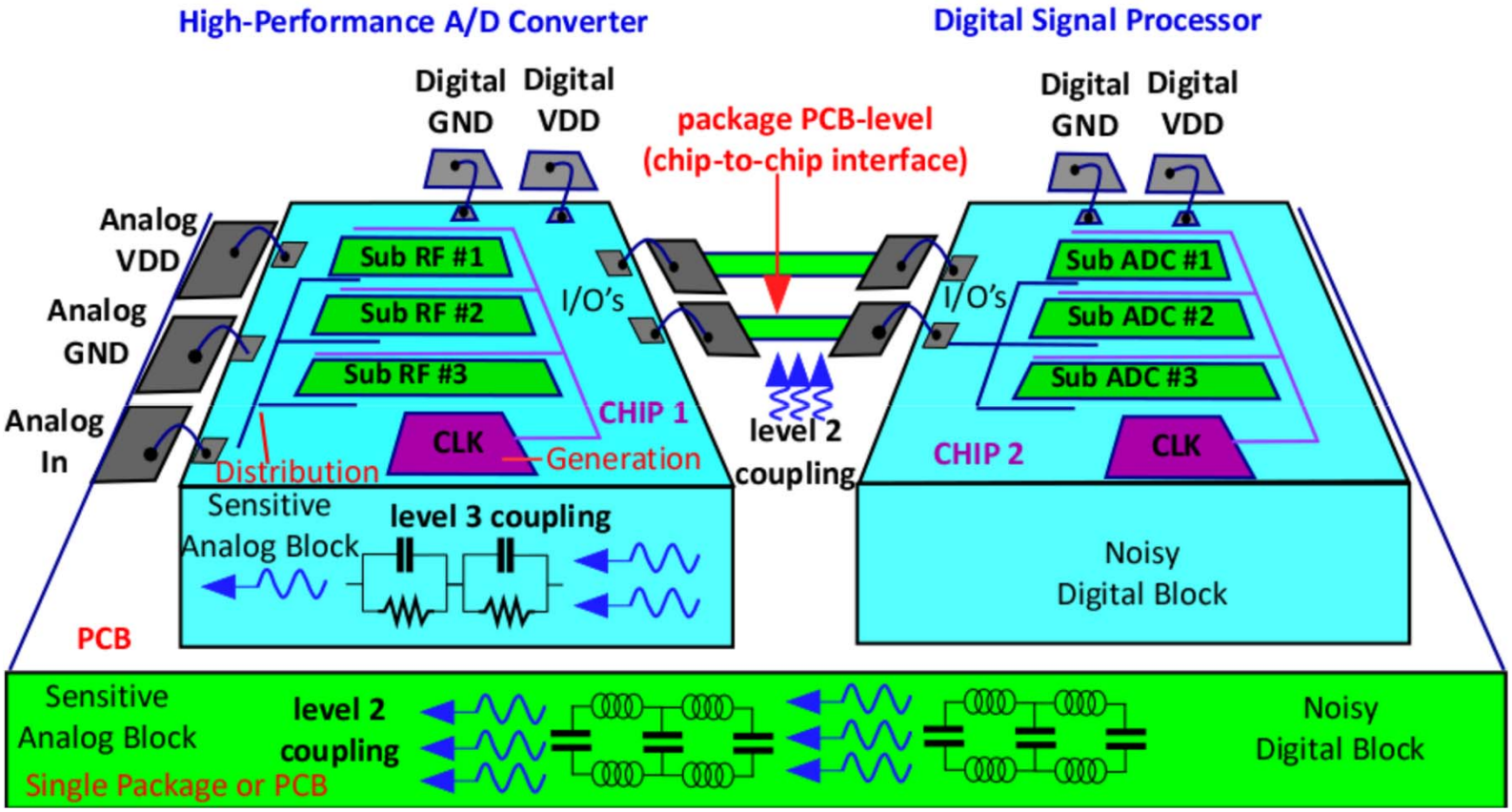
Source: Jong-Min Yook, Dong-Su Kim, and Jun-Chul Kim, "Double-sided Si-Interposer with Embedded Thin Film Devices", 2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013), pp 757-760.

Silicon Interposers



Source: Jong-Min Yook, Dong-Su Kim, and Jun-Chul Kim, "Double-sided Si-Interposer with Embedded Thin Film Devices", 2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013), pp 757-760.

Coupling Noise in Mixed Signal Systems

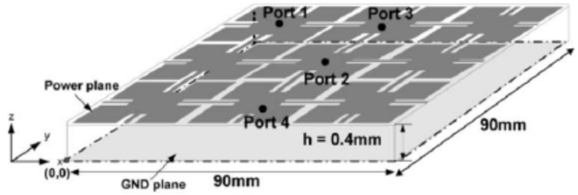


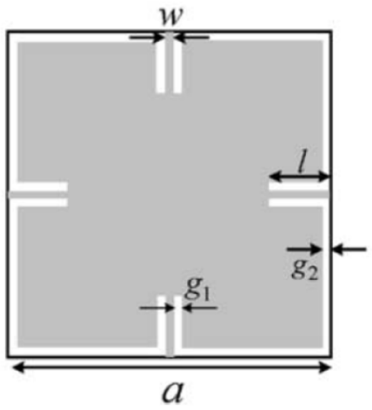
Proposed Solution

- Electromagnetic Bandgap (EBG) Structures
  - Definition: One-, Two- or Three-Dimensional Periodic Metallic/Dielectric System which Exhibits Band Rejection Behavior
  - Bandstop filter characteristics due to shunt capacitances and series inductance
  - Design can be optimized for PDN applications

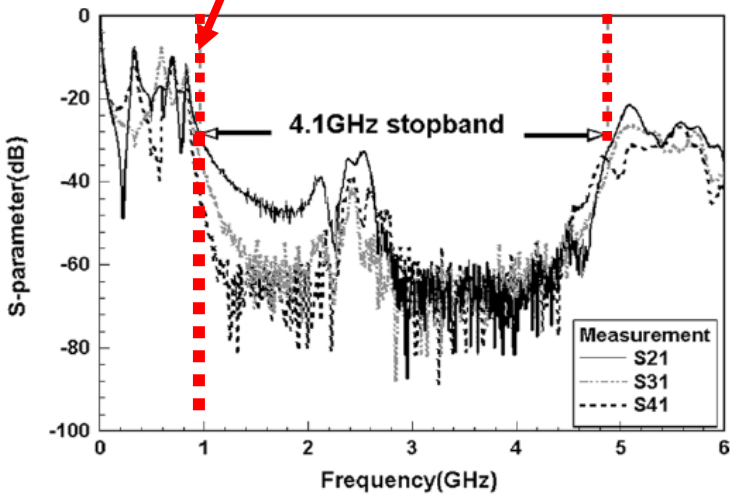
Electromagnetic Bandgap Structures (EBG)

IEEE MWCL July 2004

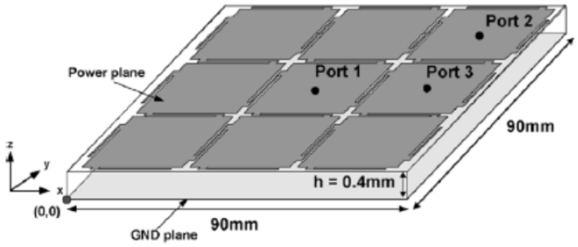


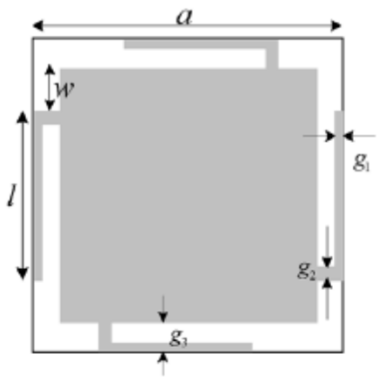


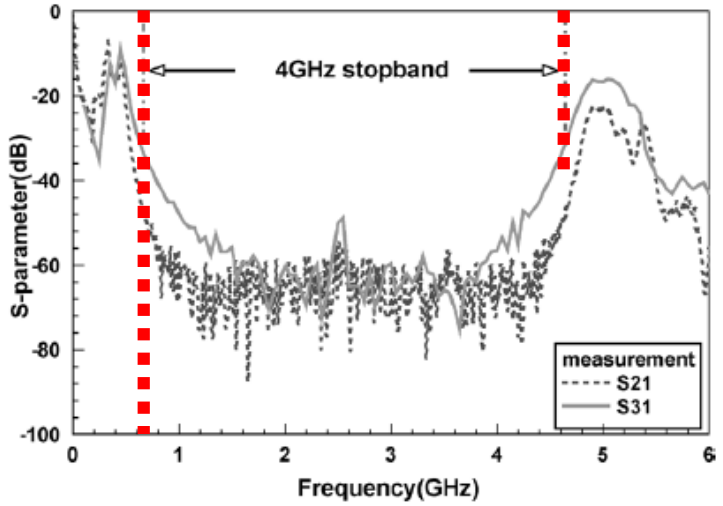
LPF: C_P and L_{bridge}



IEEE MWCL Mar. 2005

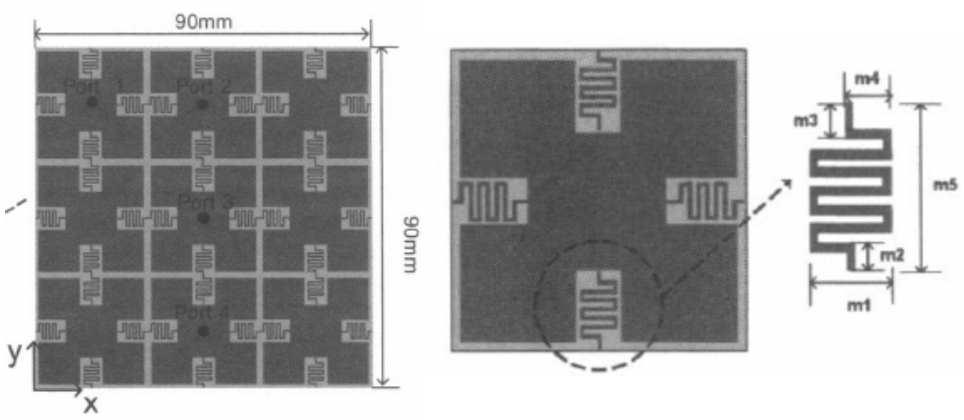


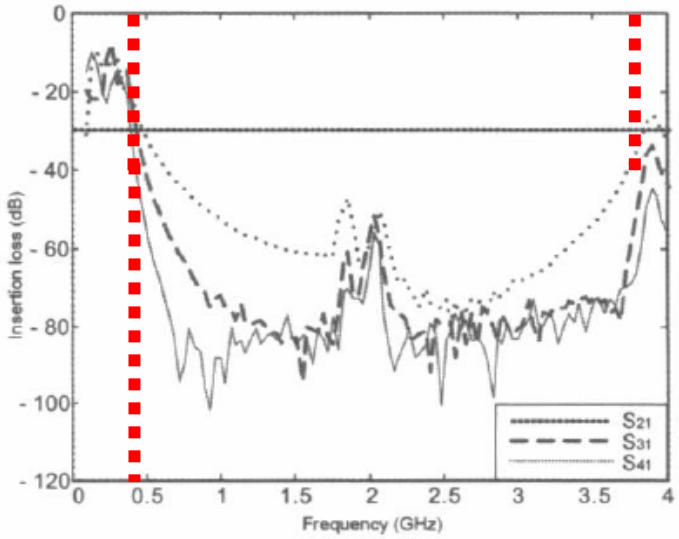




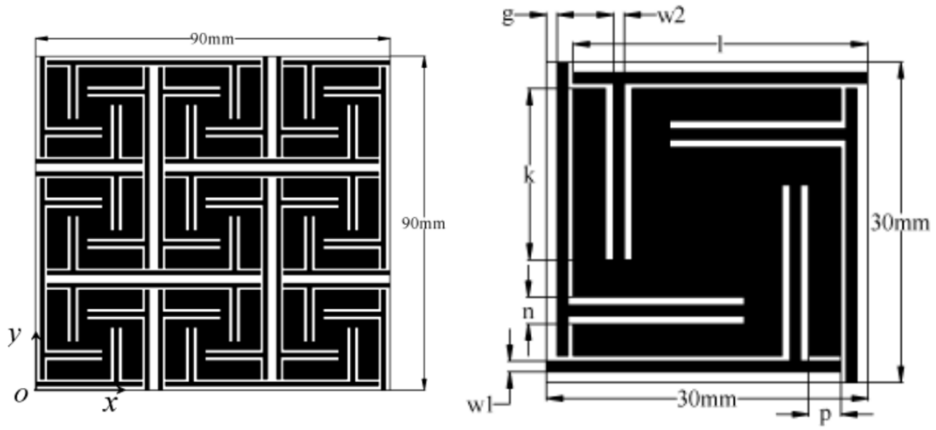
Planar-type EBG Structures

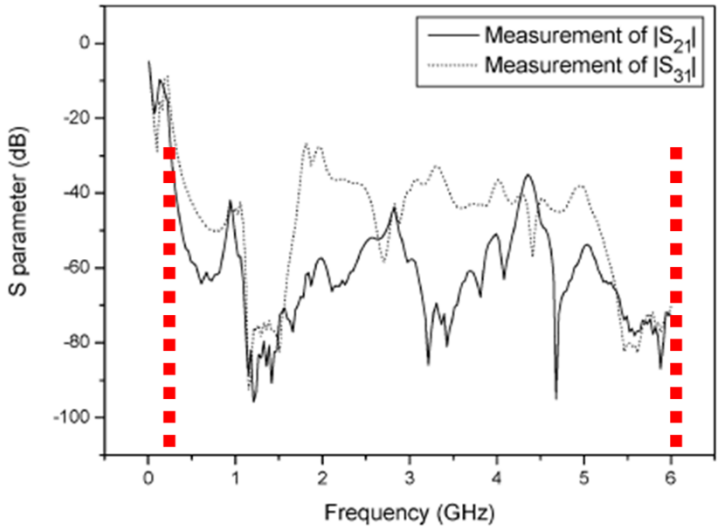
IEEE APS July 2005





IEEE MWCL Mar. 2006

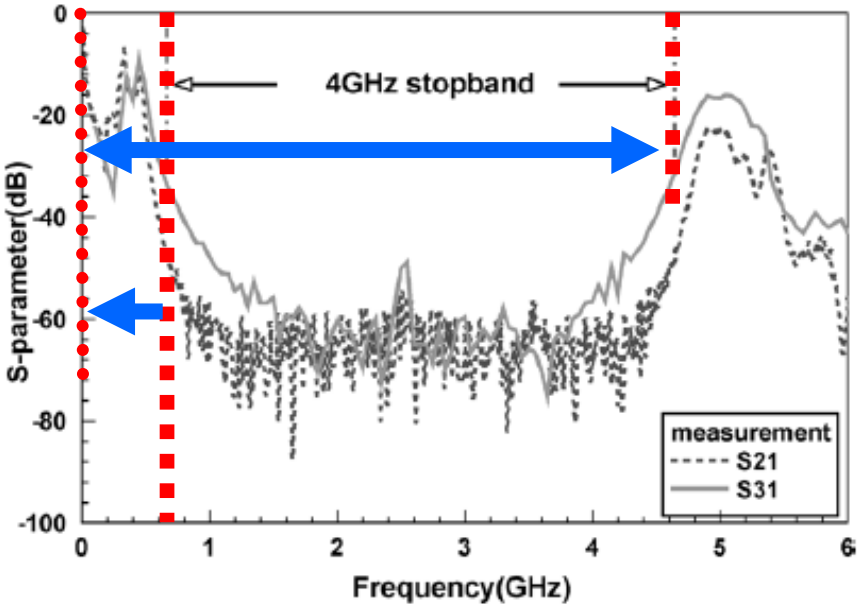


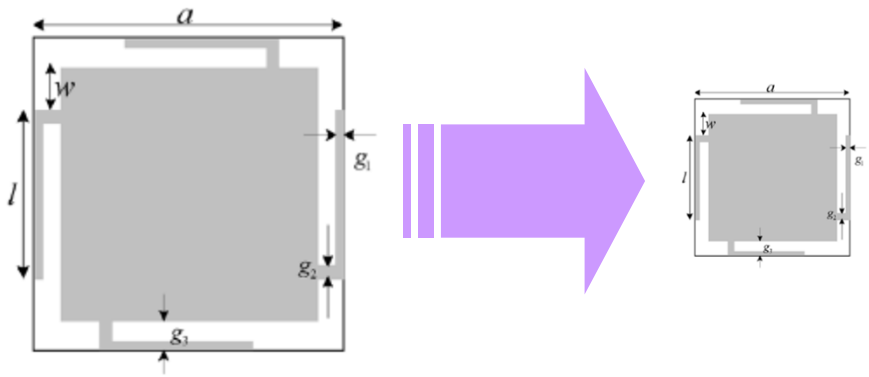


EBG Structure

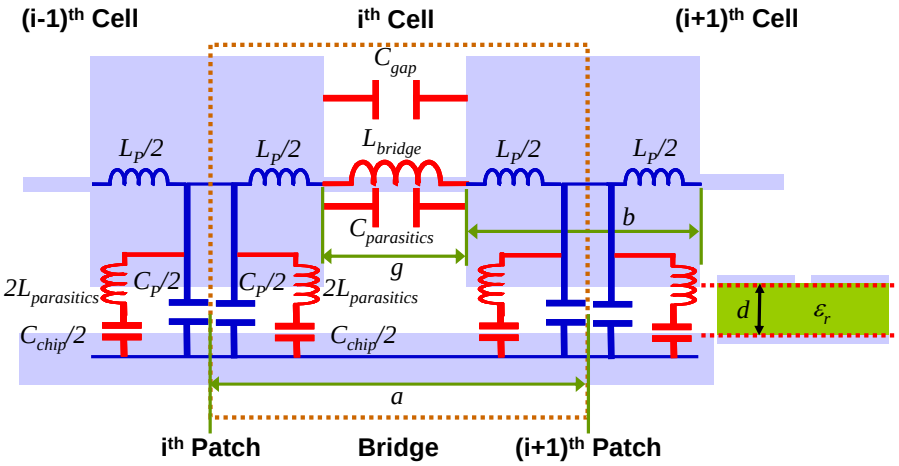
1. Reducing Cut-off Frequency of Planar-type EBG Structure
   - (In Consequence) Enhancing Noise Suppression Bandwidth

2. Miniaturizing Unit Cell of Planar-type EBG Structure
   - Without Degradation in Stopband Bandwidth



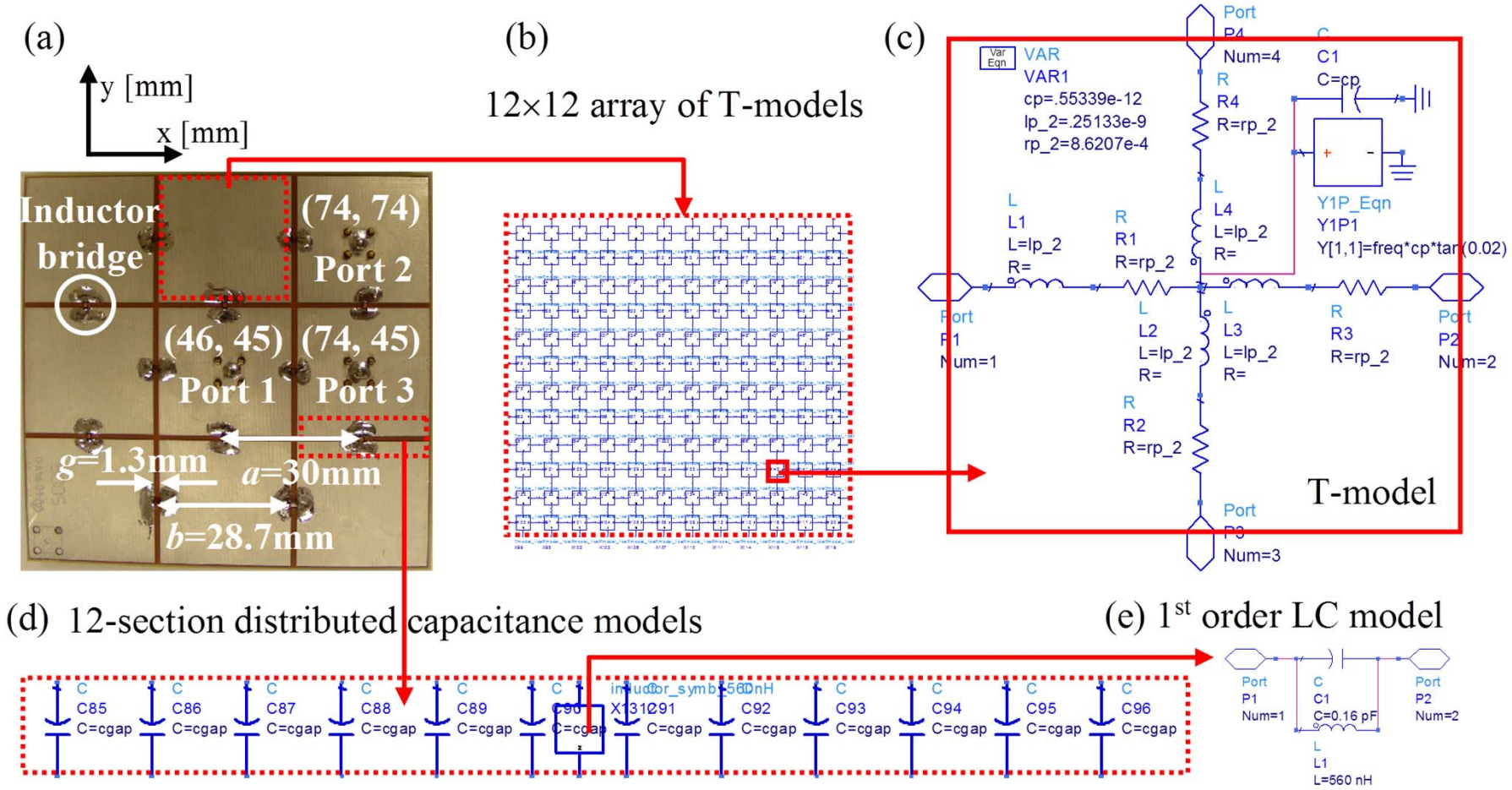


EBG Structure



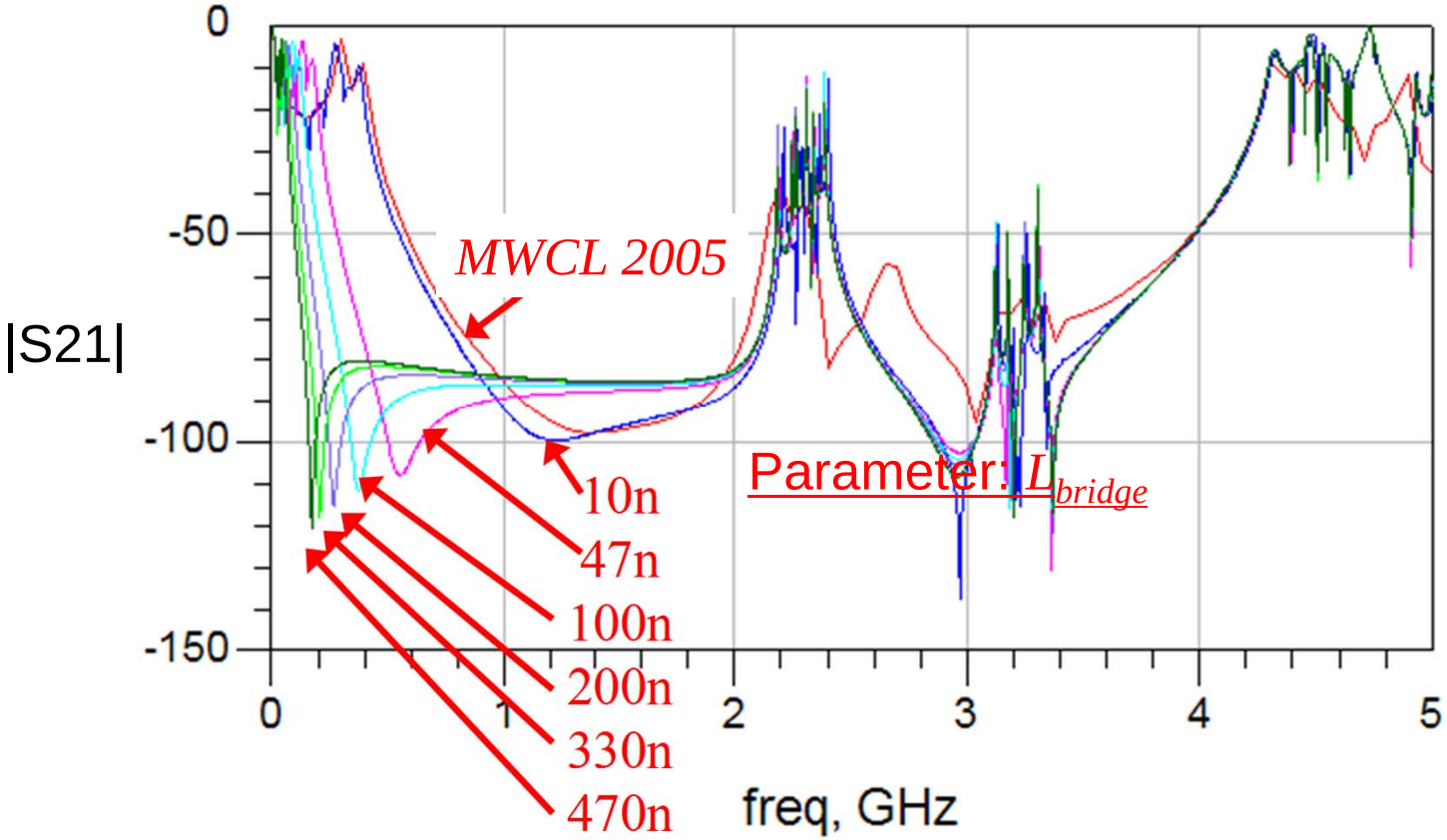
Methods of Cut-off Frequency Enhancements	Dominant Circuit Level Components in Fig.	Cut-off Frequency ($f_{lowpass\_cutoff}$) [MHz]	High Frequency Limitation of EBG Structure
Method 1: Conventional Planar-type EBG Structure	L_P, L_{bridge} (=L_{MSL}), and C_P	$\left[\pi\sqrt{C_P\left(L_P + L_{MSL}\right)}\right]^{-1}$	1st Resonant Frequency of Patch at $c/\left(2b\sqrt{\varepsilon_r}\right)$
Method 2: Increasing Bridge Inductance using Series Lumped Chip Inductors	L_P, L_{bridge} (=L_{chip}), and C_P	$\left[\pi\sqrt{C_P\left(L_P + L_{chip}\right)}\right]^{-1}$	1st Resonant Frequency of Patch at $c/\left(2b\sqrt{\varepsilon_r}\right)$
Method 3: Increasing Patch Capacitance using Shunt Lumped Chip Capacitors	L_P, L_{bridge}, $L_{parasitics}$, C_P, and C_{chip}	$\left[\pi\sqrt{C_P^{'}\left(L_P + L_{bridge}\right)}\right]^{-1}$	Parallel Resonant Frequency of C_P and $L_{parasitics}$ at $1/\left(2\pi\sqrt{C_P L_{parasitics}}\right)$

Verification: ADS Simulation



Simulation Results

– EBG Structure with 90x90 mm² Ground Plane Area



On-Chip Issues

- Goal – to perform low-cost, simple and accurate time domain measurement of SI parameters on interconnects in .13µm technology, such as:
  - Dispersion
  - Effect of vias
  - Propagation delay
  - Crosstalk
  - Crosstalk-induced delay
  - Differential mode signaling
  - Clock distribution trees
  - …
- **Reference work:** **A. Deutsch et al, *"On-Chip Wiring Design Challenges for Gigahertz Operation"*, pp 529-555, Proc. IEEE, vol. 89, No. 4, April 2001.**

On-Chip Fundamental Challenges

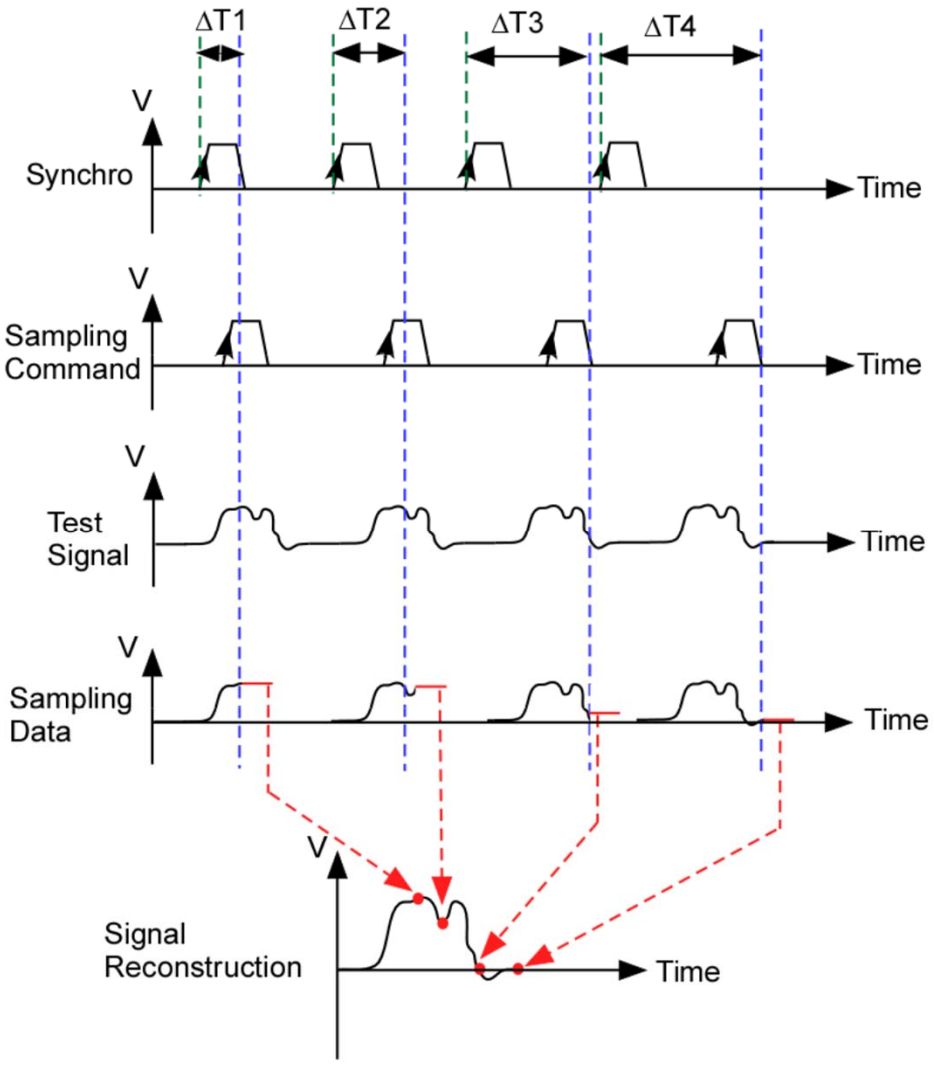
– Circuits performing measurements are in the same technology as the circuits being measured

– Cannot be made intrinsically "faster", sampling at Nyquist rate is not possible

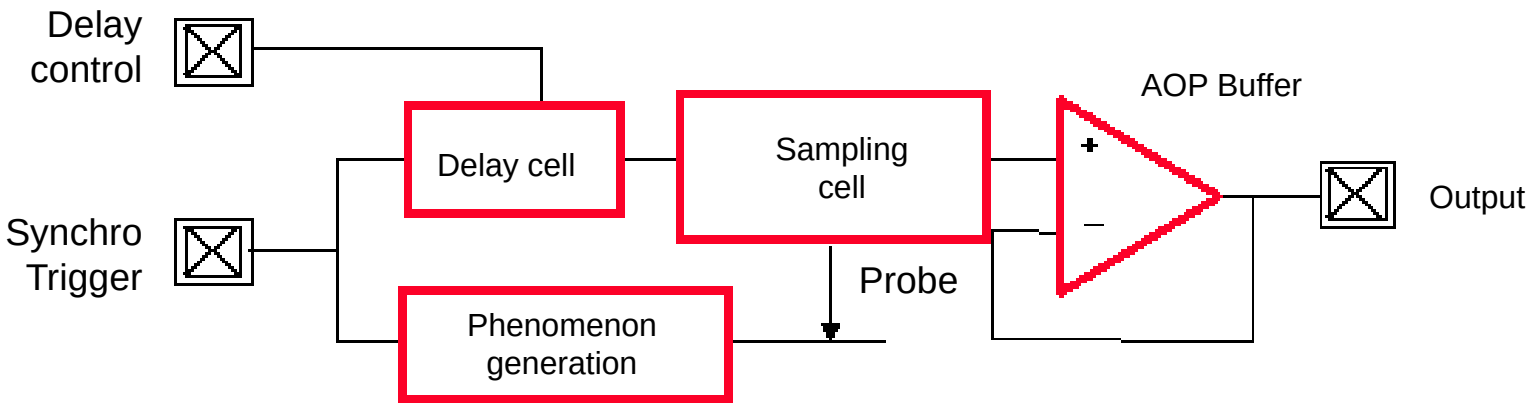
– Solution: take repeated samples at a lower rate

- **Reference work in .18µm**: **F. Caignet et al, *"The Challenge of Signal Integrity in Deep-Subμm CMOS Technology"*, Proc. IEEE, vol. 89, No. 4, pp. 556-573, April 2001.**

Subsampling



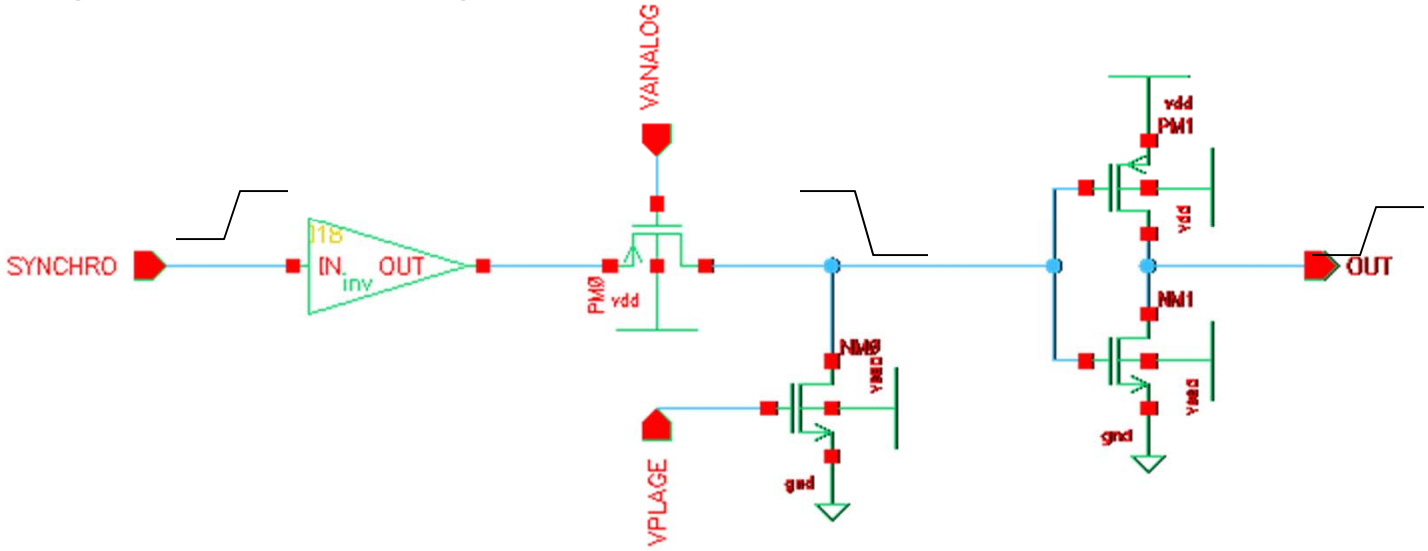
Basic Circuit Principle



- External synchronization triggers a phenomenon
- Sampled by a transmission gate switch after an externally controlled delay
- Sampled analog voltage stored in AOP input capacitance, buffered, exported out of the chip to the ADC

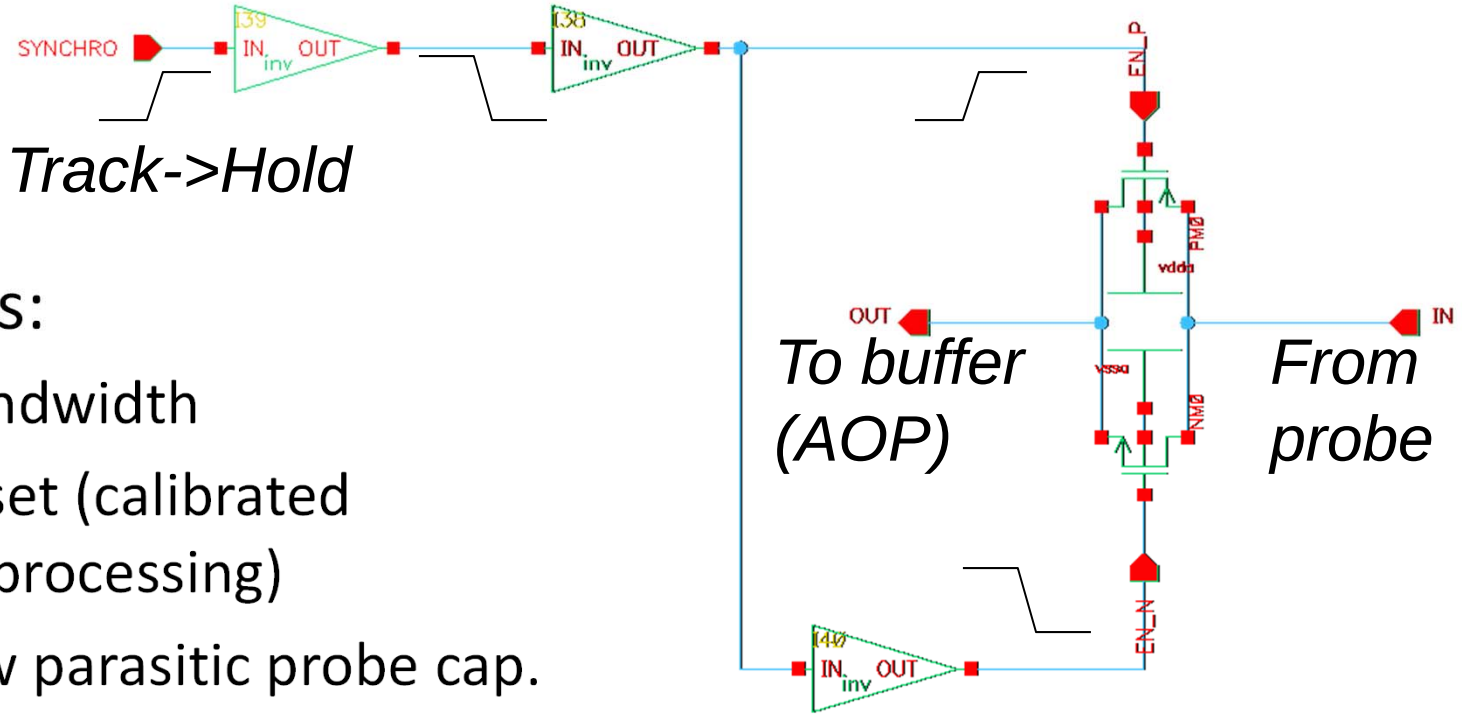
Delay Cell

- Requirements:
  - Delay law linear with Vanalog for any Vplage (can also be calibrated in post-processing)
  - Vplage allows changing the observability window (zoom in/out)



Sampling Cell

- Simple transmission gate switch used



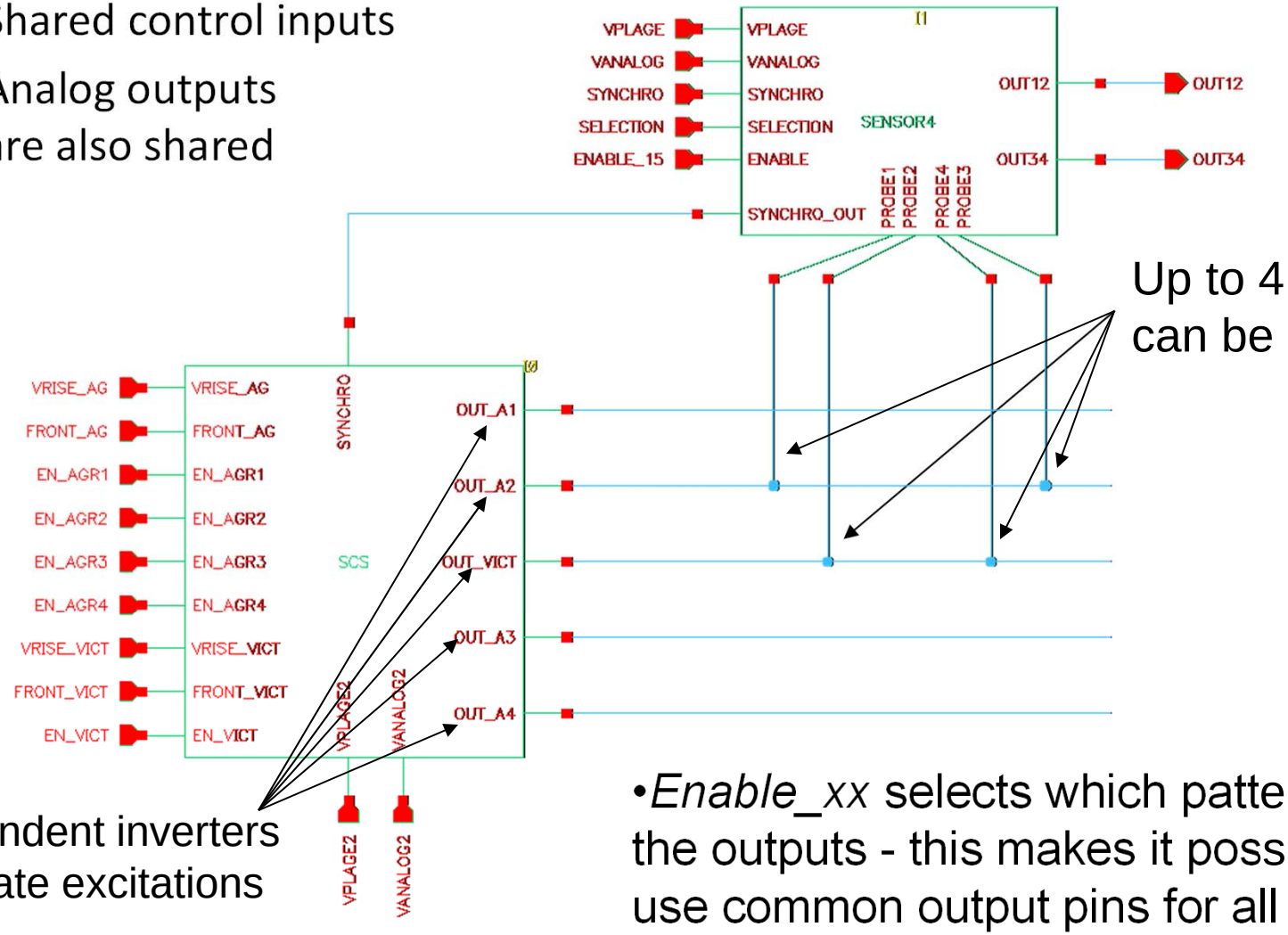
- Objectives:
  - Max bandwidth
  - Min offset (calibrated in post-processing)
  - Very low parasitic probe cap.
  - Overdriven to VDD_AOP,VSS_AOP to reduce I_off leakage, increase BW

Additional Calibration Circuit

1. Complete circuit offset calibration
   - Probe input directly excited externally
   - Ramp from 0 to Vdd
2. Delay law calibration
   - Ring oscillator, with a frequency divider (to relax requirements on the oscilloscope used for measuring delay law)

Single Pattern Schematic

- Shared control inputs
- Analog outputs are also shared

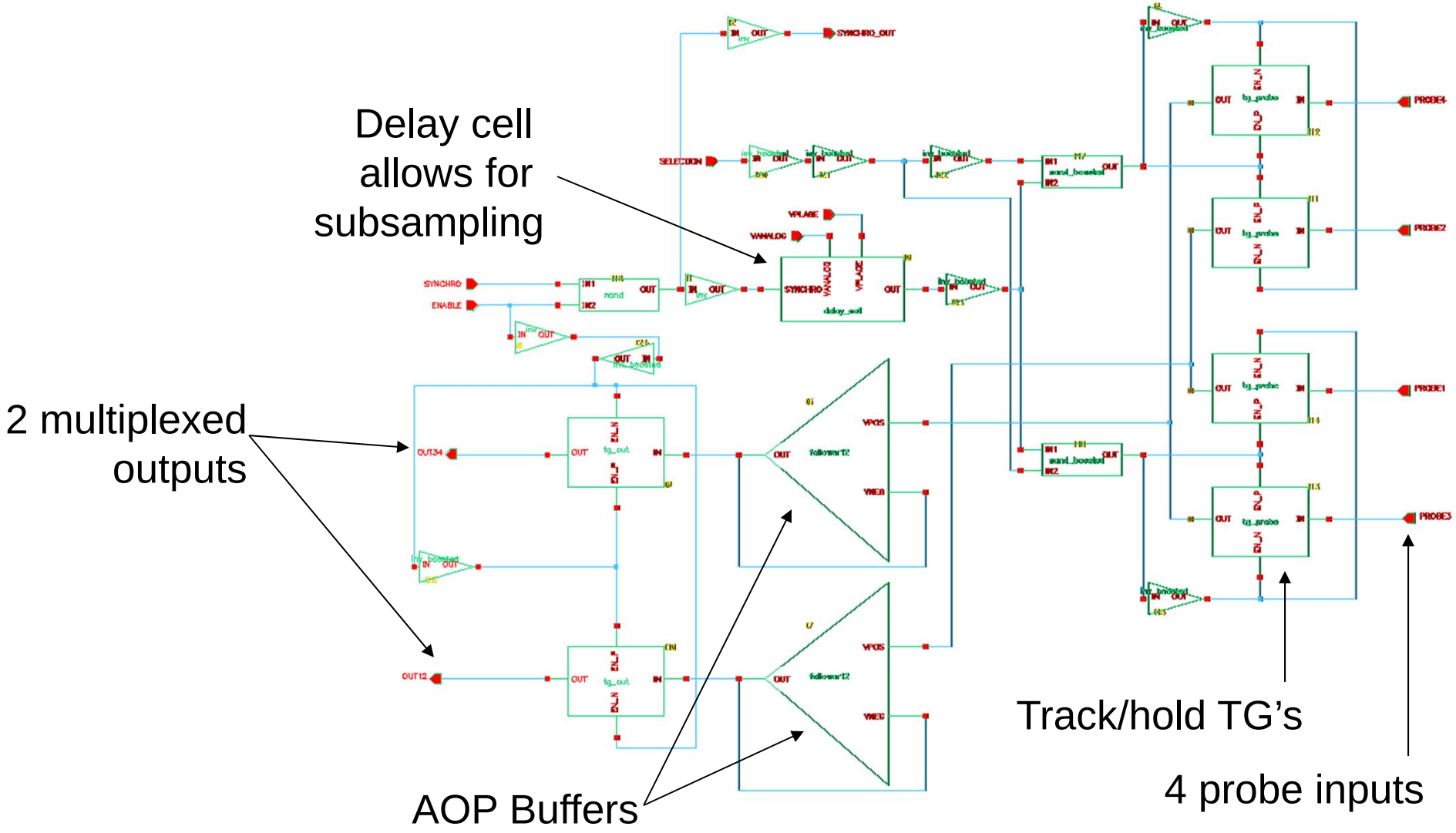


Up to 4 points can be probed

5 independent inverters to generate excitations

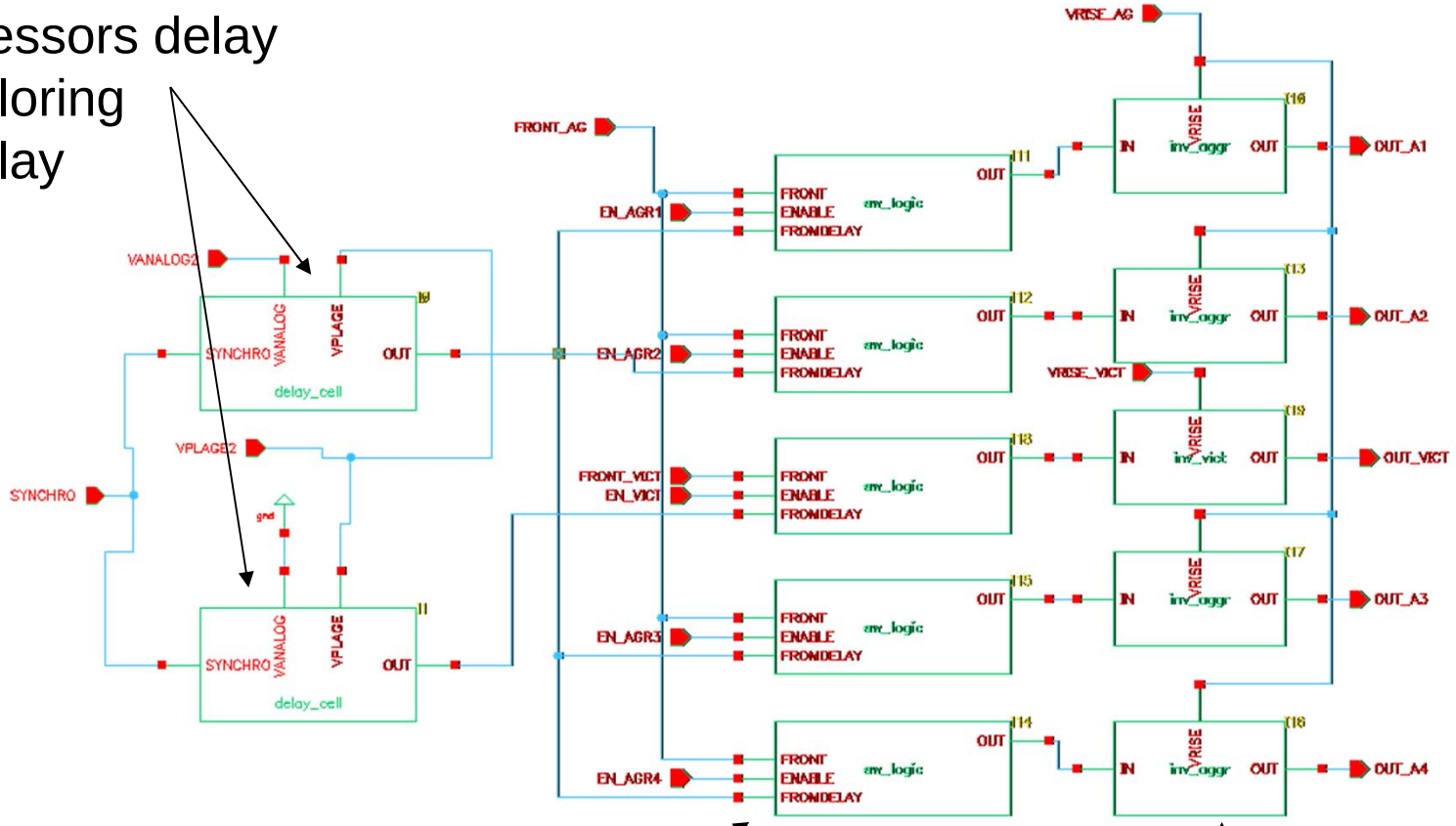
•*Enable_xx* selects which pattern drives the outputs - this makes it possible to use common output pins for all patterns

Four-Probe Sensor



Switching Control System

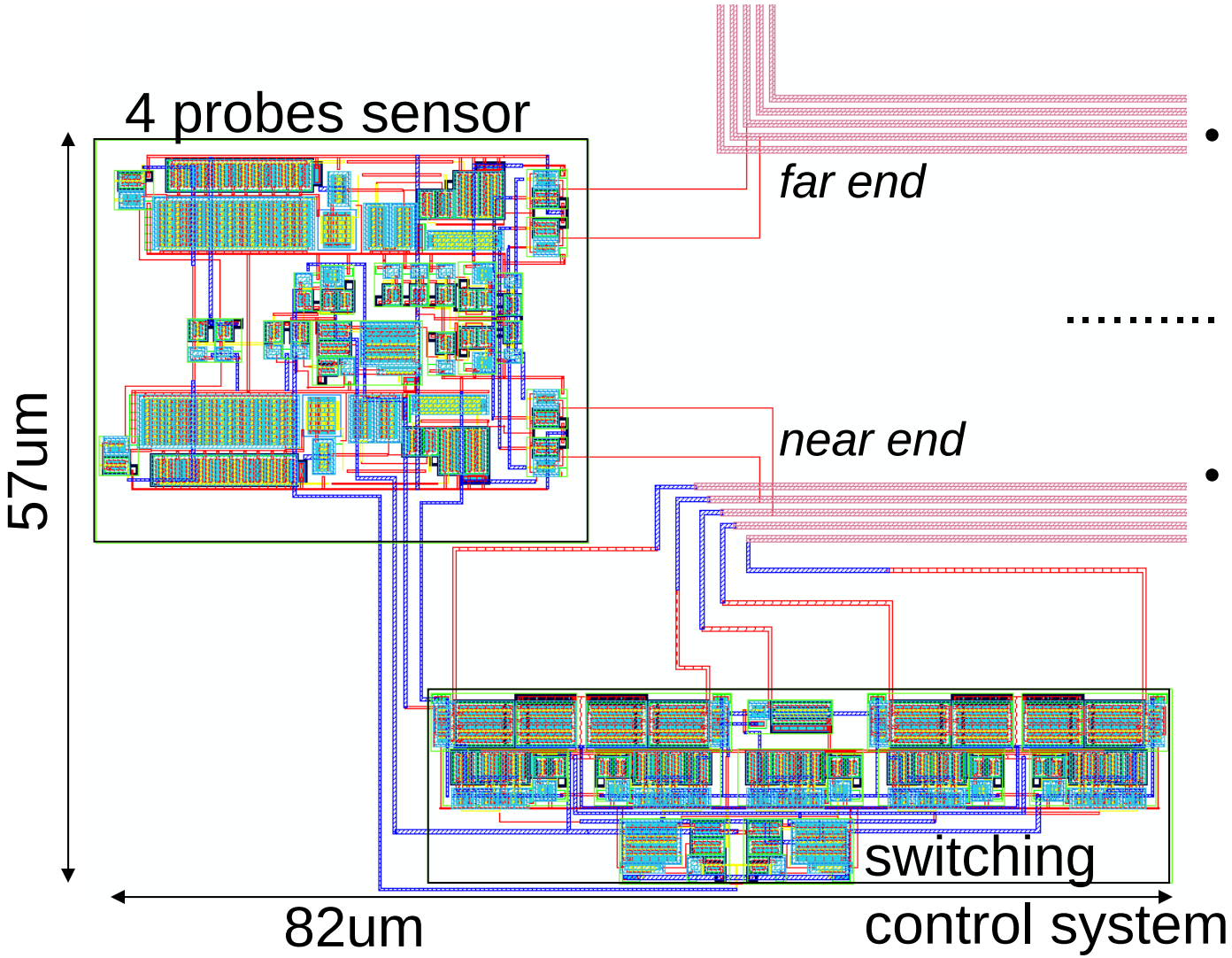
Victim/Aggressors delay cells for exploring crosstalk delay



5 independent control logic blocks

Strong inverters driving the interconnects

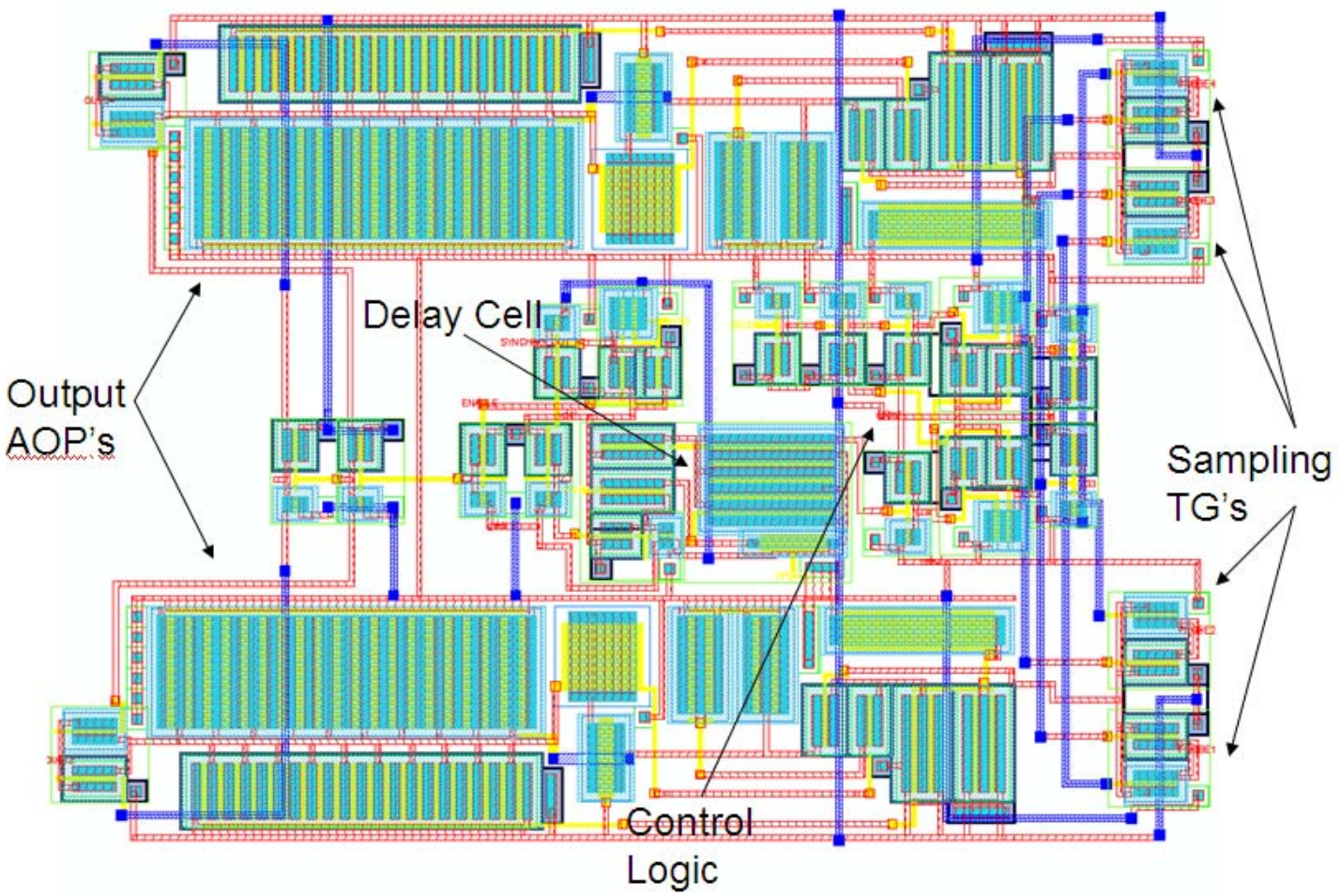
Oscilloscope Block Layout



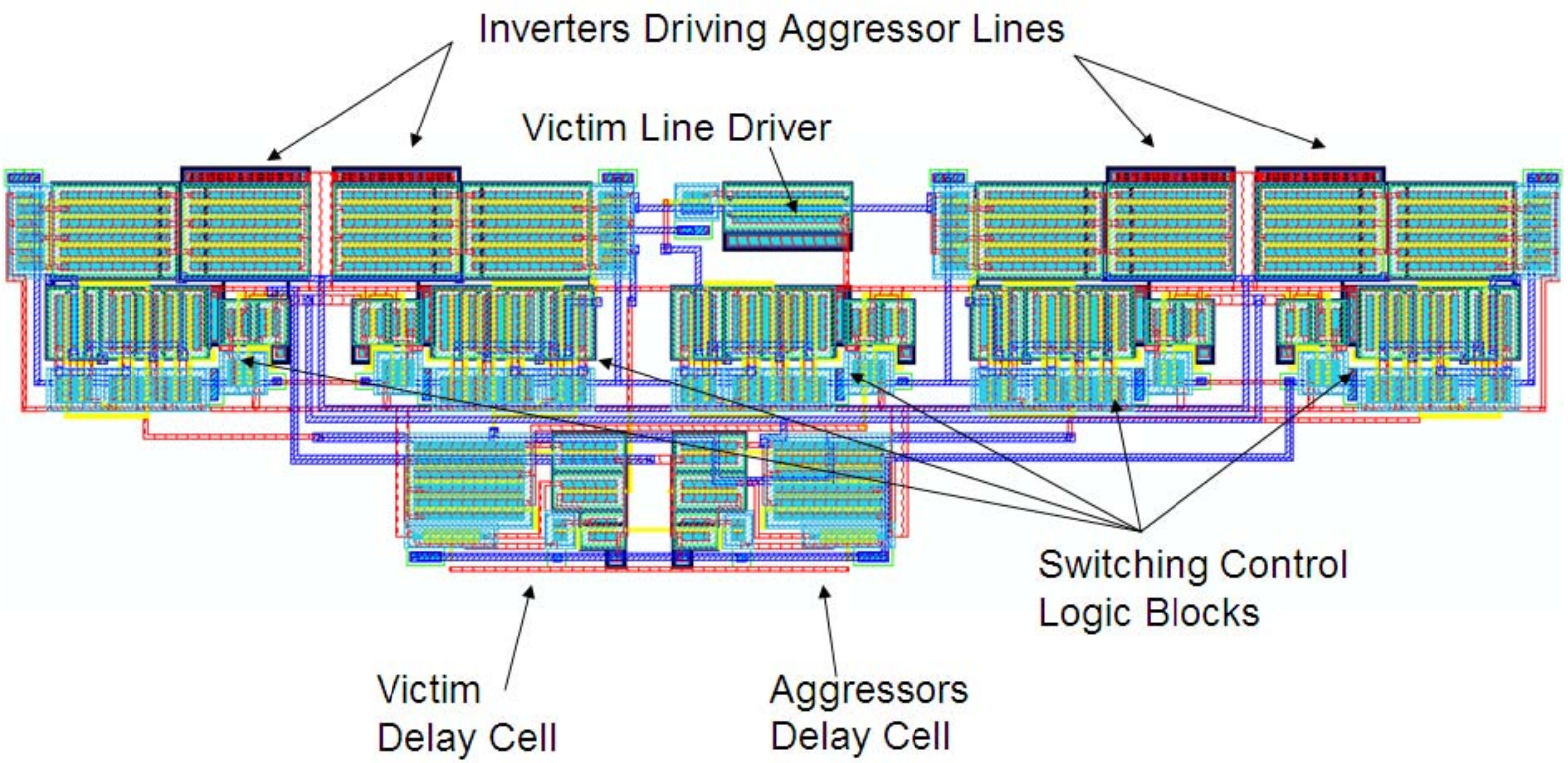
- The bulk of the area occupied by the interconnects under test

- Long lines can be folded several times to fit into chip width limits

Four-Probe Sensor Layout

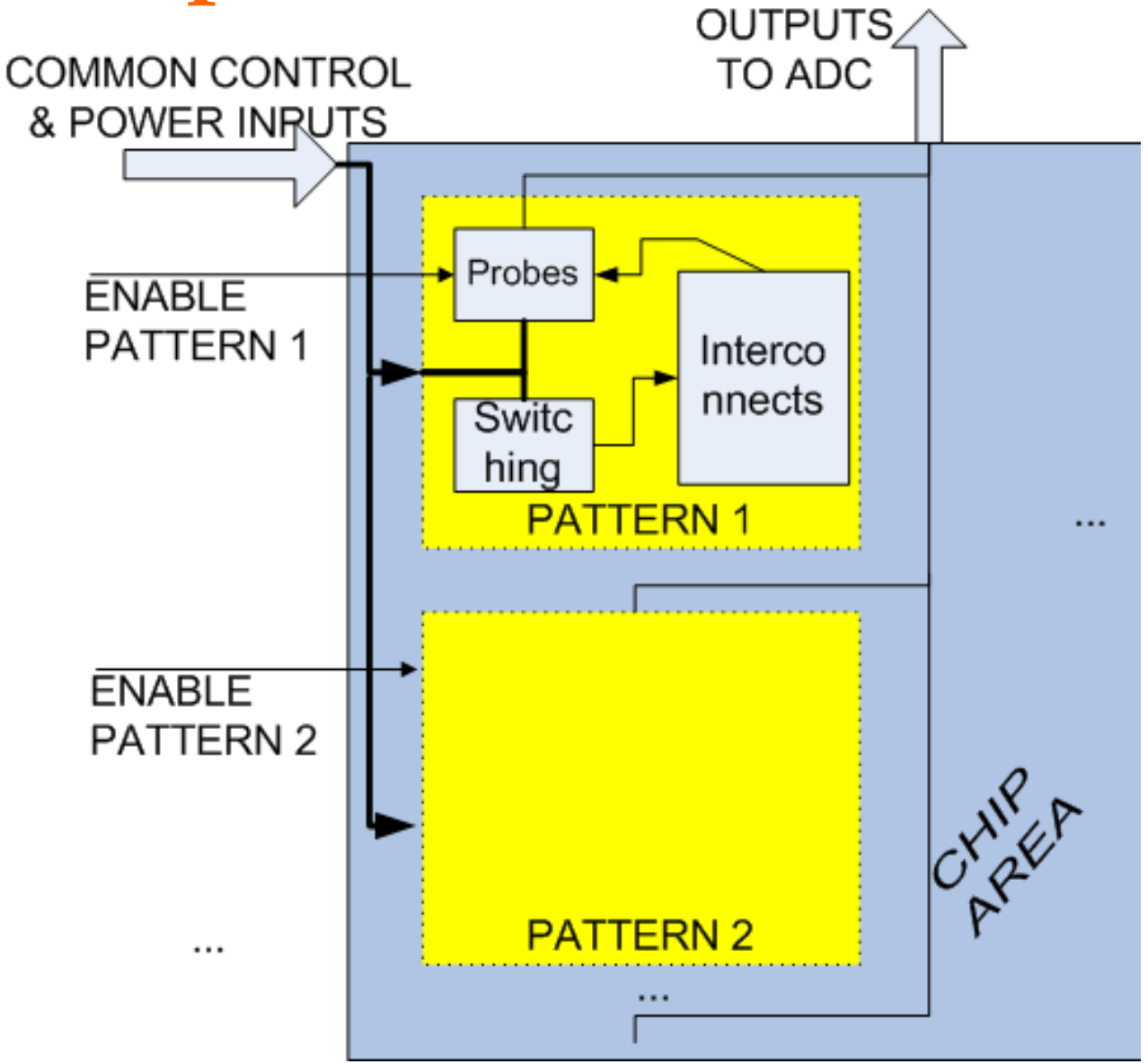


Switching Control System Layout



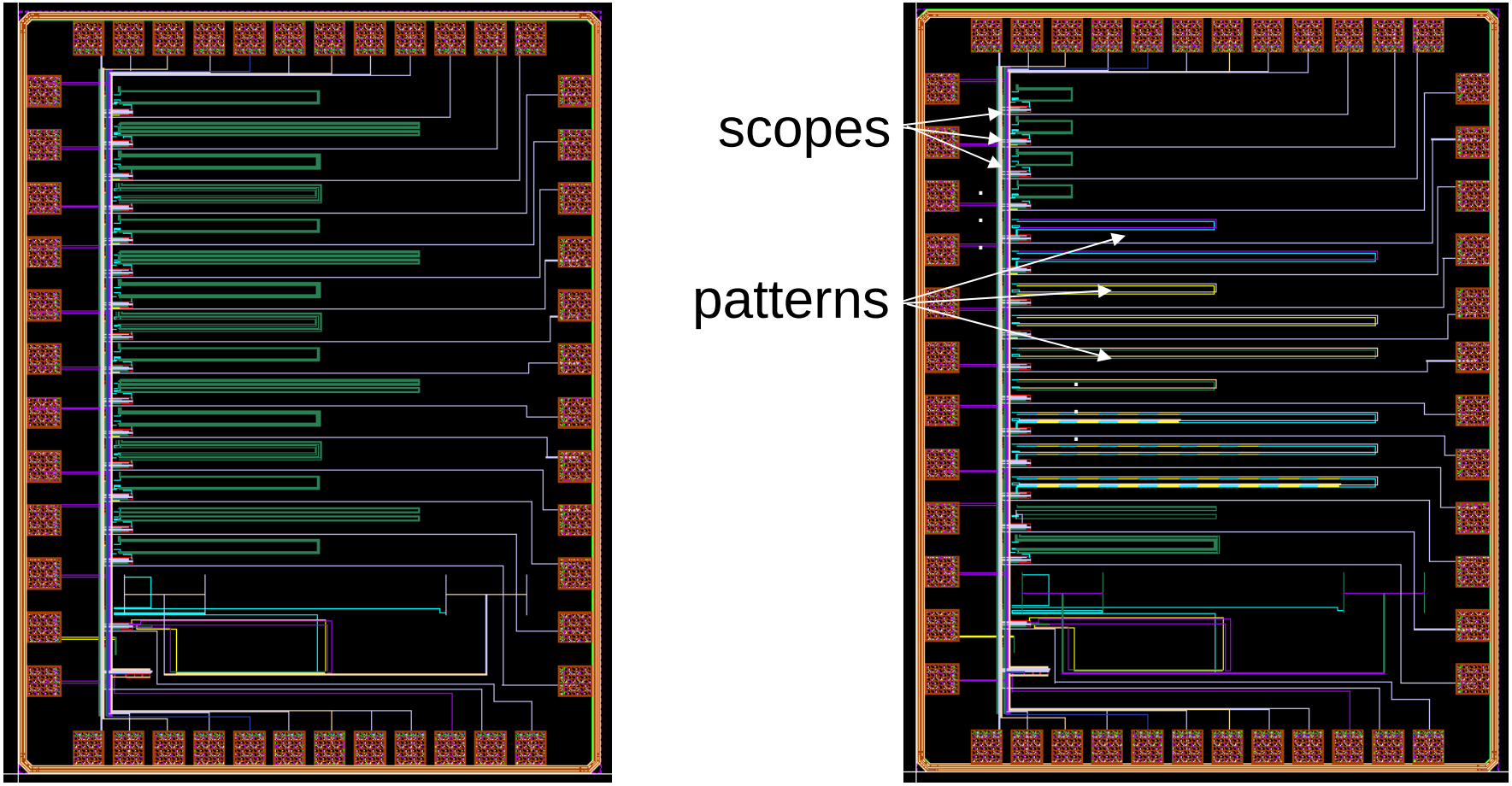
Multiple Patterns

- All inputs and outputs are slow-changing
  - Analog inputs are control voltages or enable bits
  - output sampled at ~1Msample/s
- Exact pin assignment and routing to each pattern should not be critical



Chip Layout

16 interconnect patterns on each, +2 calibration structures



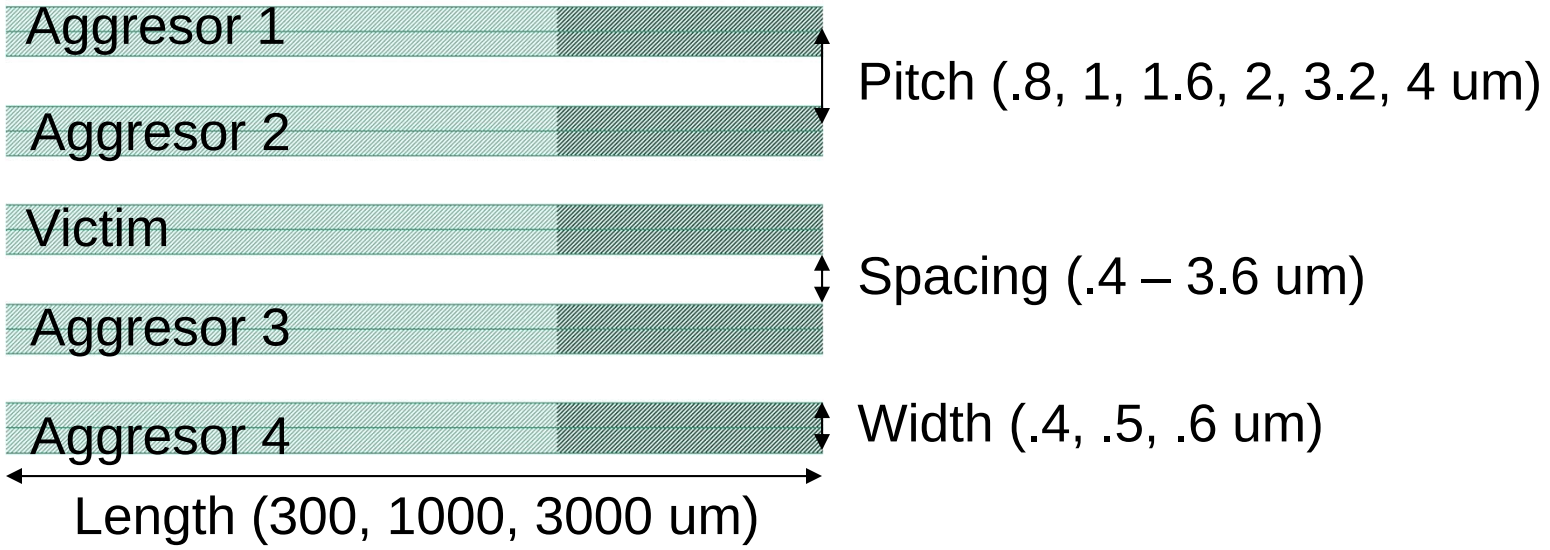
UIUC_SCOPE_01 (1450x1900um) UIUC_SCOPE_02

Measurement Protocol

Meas No.	Chip	DIP Switch	Pattern No.	Control Bits	Purpose	Notes
01	1	14	14	01000101?	delay, single	a2
02	1	13	13	01000101?	delay, single	a2
03	2	4	20	01000101?	delay, single	a2
04	1	6	6	01000101?	delay, single	a2
05	1	5	5	01000101?	delay, single	a2
06	2	2	18	01000101?	delay, single	a2
07	2	15	16	01000101?	delay, single	a2
08	2	9	25	01000011	delay, single, m3	a2
09	2	10	26	01000011	delay, single, m3	a2
10	2	5	21	01000011	metal1	a2
11	2	6	22	01000011	metal1	a2
12	2	7	23	01000011	metal2	a2
13	2	8	24	01000011	metal2,repeatab.	a2
25	1	7	7	01000101?	xtalk	a2
27	1	7	7	10000101?	xtalk	a1
28	1	8	8	01000101?	xtalk, width	a2
30	1	8	8	10000101?	xtalk	a1
31	1	13	13	01100011?	xdelay	v hi-lo, ag2&3 lo-hi
32	1	13	13	01100011?	xdelay	v hi-lo, ag2&3 lo-hi, van2=10mV
33	1	13	13	01100011?	xdelay	v hi-lo, ag2&3 lo-hi, van2=20mV
34	1	13	13	01100011?	xdelay	v hi-lo, ag2&3 lo-hi, van2=30mV
35	1	13	13	01100011?	xdelay	v hi-lo, ag2&3 lo-hi, van2=40mV
36	1	13	13	00100110	xdelay	v hi-lo, ag2 quiet, ag3 lo-hi
37	1	4	4	01001011	width	a2
38	1	12	12	01001011	width	a2
39	1	13	13	00000110	xdelay	v hi-lo, ag2&3 quiet
40	2	14	30	00100000?	modes	a3 hi-lo, v quiet at lo
41	2	14	30	00100011	modes	a3 hi-lo, v quiet at hi
42	2	16	31	00010000?	htree12	a4 hi-lo->a4' lo-hi
43	1	16	32	00010000?	htree56	a4 hi-lo->a4' lo-hi
44	2	7	23	00100000	metal5	a3
45	2	8	24	00100000	metal5	a3

Note: control bits: EnableAg1, EnableAg2, nableAg3, EnableAg4, FrontAg, EnVict, FrontVict, Select

Interconnect Configuration 1

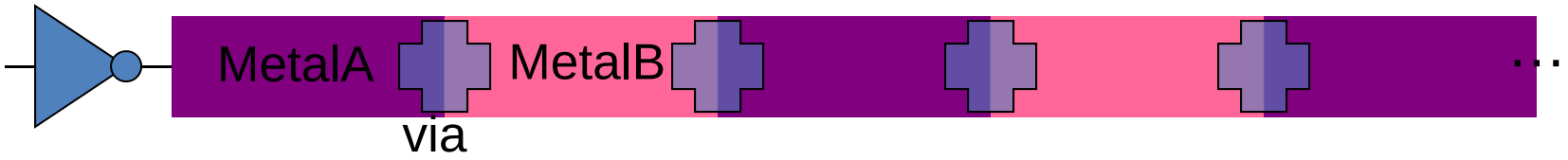


- A pattern: one victim line and four aggressor lines; all 5 can be switched on/off independently
  - 20 combinations of patterns in Metal3, varying width, spacing (pitch) and length
- Allows for complete characterization of the technology process (delay, crosstalk, crosstalk-induced delay)

Interconnect Configuration 2

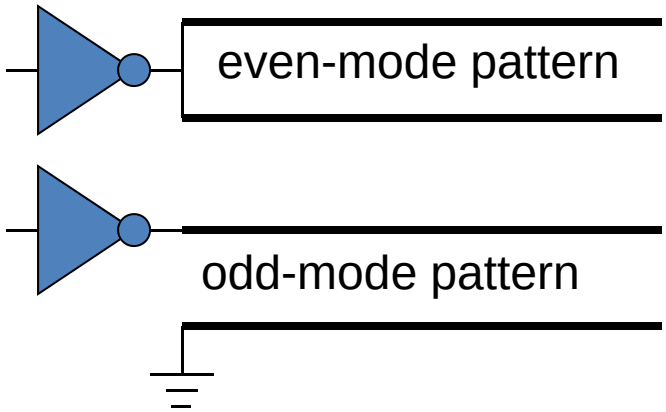
- Total of 12 single lines in Metal1 – Metal6:
  - width 0.4um, two lengths (500 and 900 um)
- Allows for characterization of dispersion and loss
- Allows to calibrate out effect of long probe lines

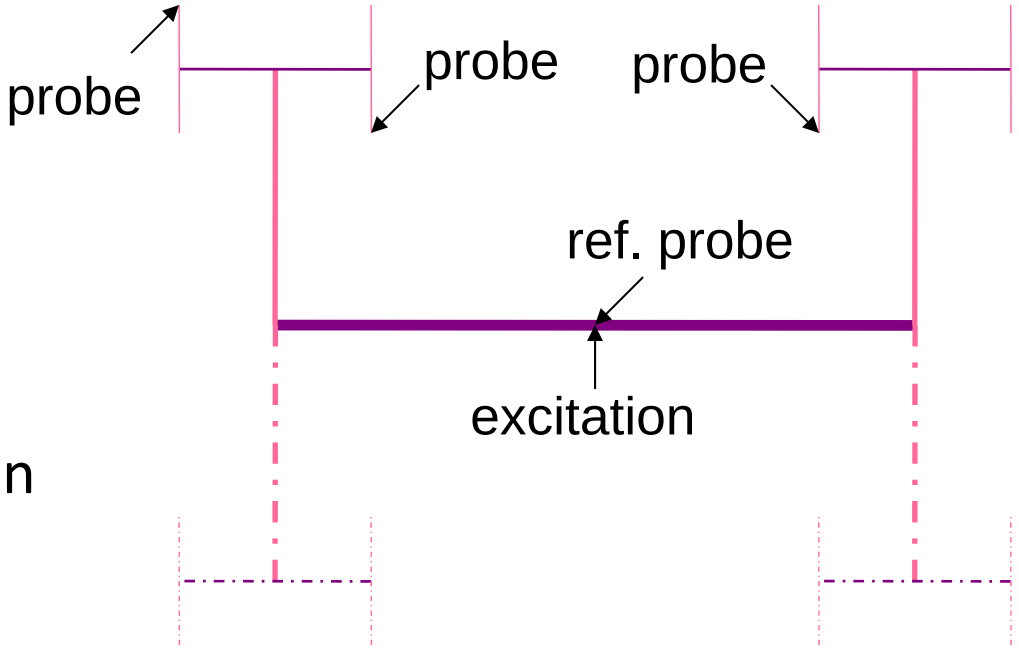
- Lines with vias in Metal1/2 and Metal5/6:
  - width 0.4um, total length 1800um
  - varying number of vias (16, 24, 32)
- Allows exploration of inductive effects of vias



Interconnect Configuration 3

- Odd- and even-mode propagation measurements
  - Width 0.5um, length 1000um, Metal3
- Allows exploration of differential signaling





- H-trees for clock distribution
  - Two configurations (Metal3/4 and 5/6)
- Allows exploration of process variations and clock signal integrity

Interface Specifications

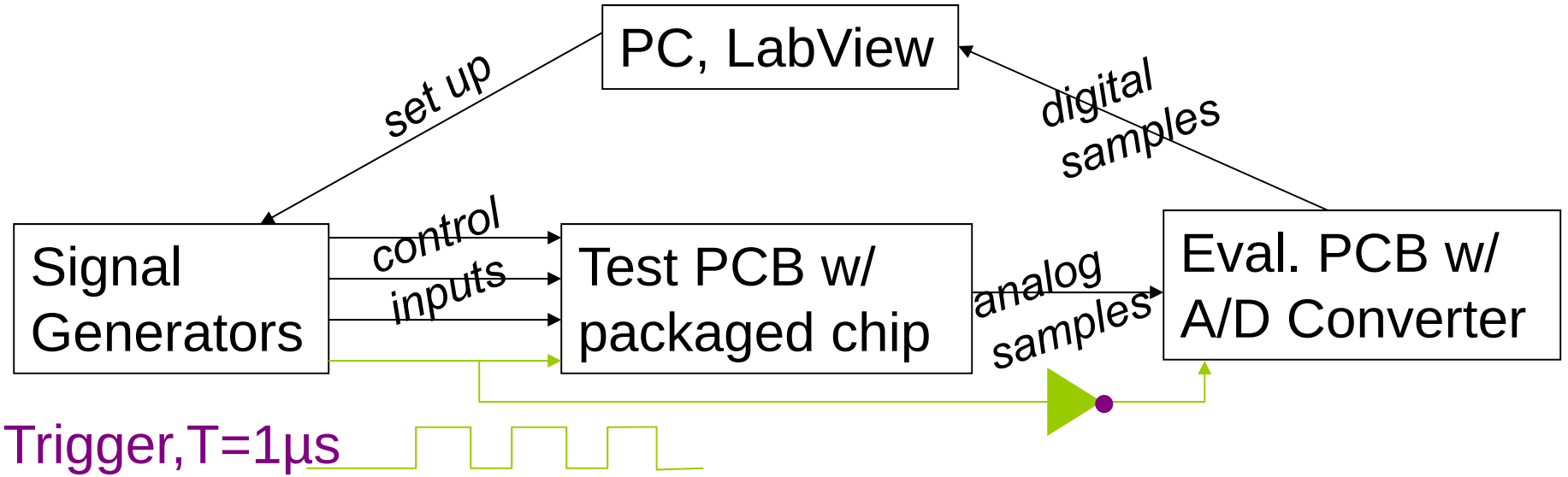
- Control Inputs:
  - Common for all patterns: 6 analog, 10 digital
  - Each pattern has its own Enable digital input
- Power Supplies:
  - VDD, GND, VDD_AOP, VSS_AOP
- Outputs:
  - 2 analog outputs towards ADC board
  - Asynchronous sampling controlled by external pulse train

➢ *Note: large number of inputs, packaging req'd*

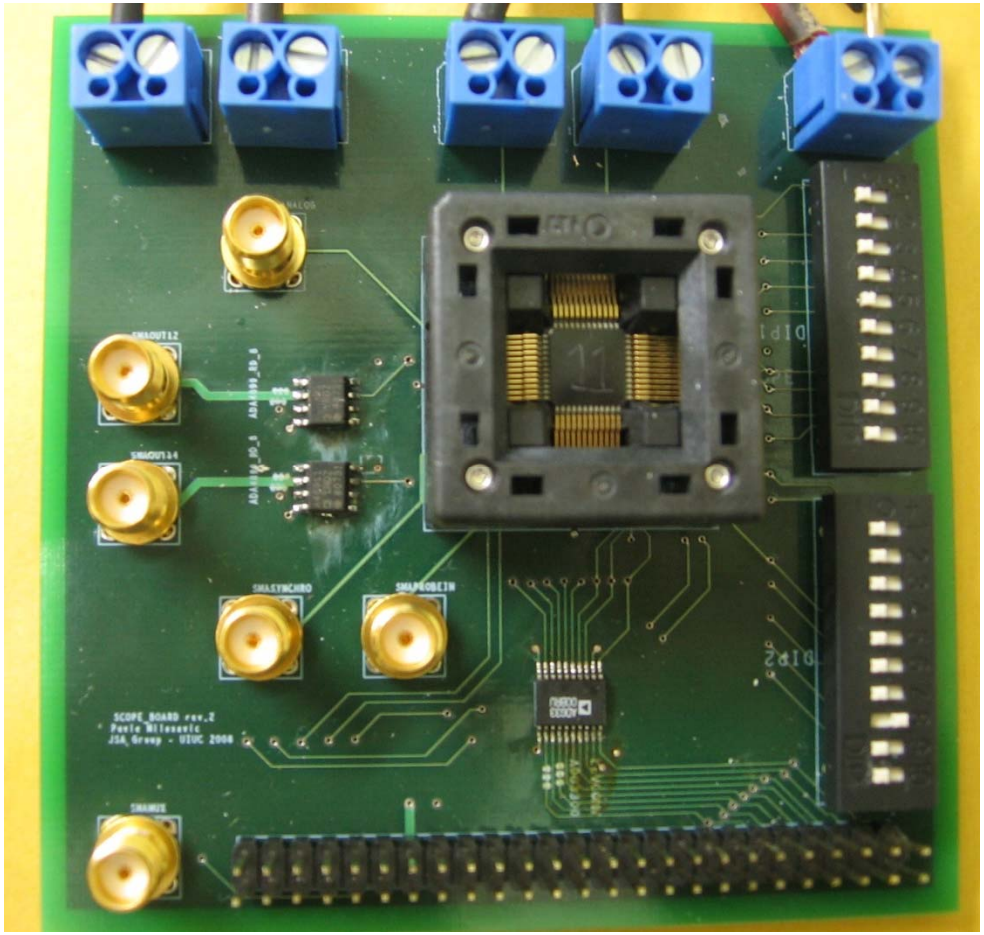
➢ direct on-chip probing doesn't seem practical (max 8 input signals per Cascade DC+RF probe)

Test Setup

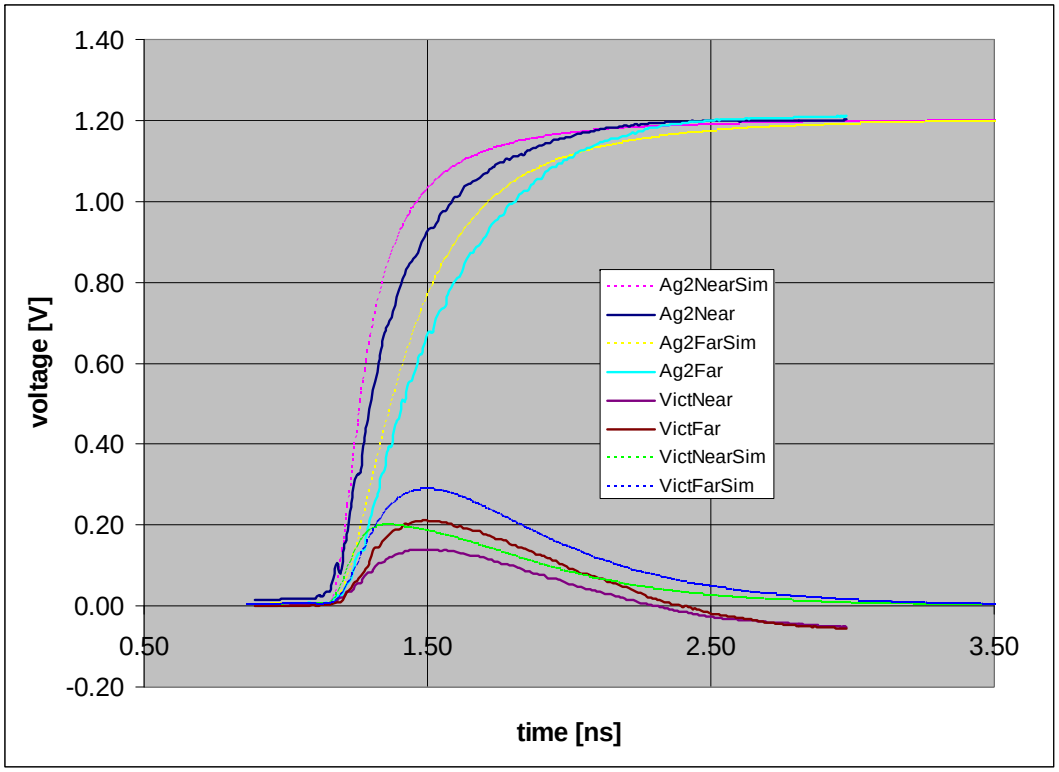
- A high performance package (low inductance and short bonding), placed on a test PCB;
- Control inputs generated externally;
- Outputs digitized using external ADC board;
- Inputs controlled by PC; data gathered and post-processed to quantify SI effects.



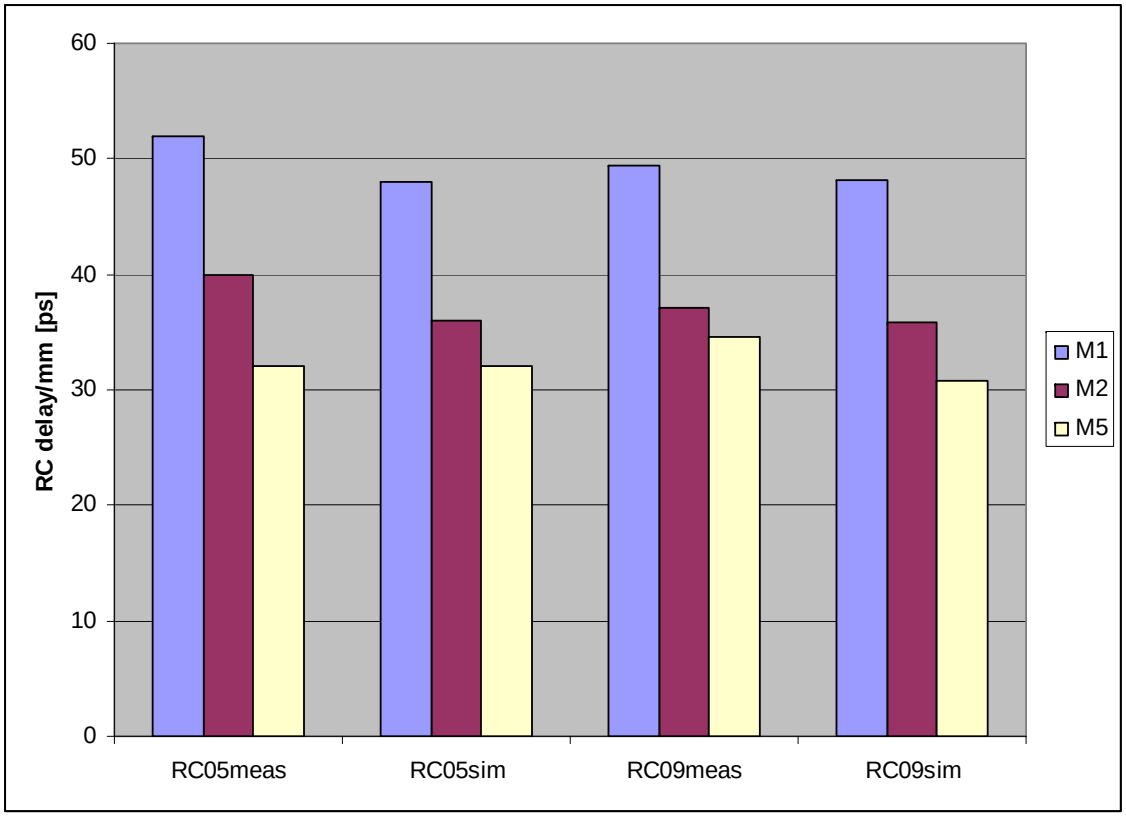
Test Board



Measurement vs Simulation

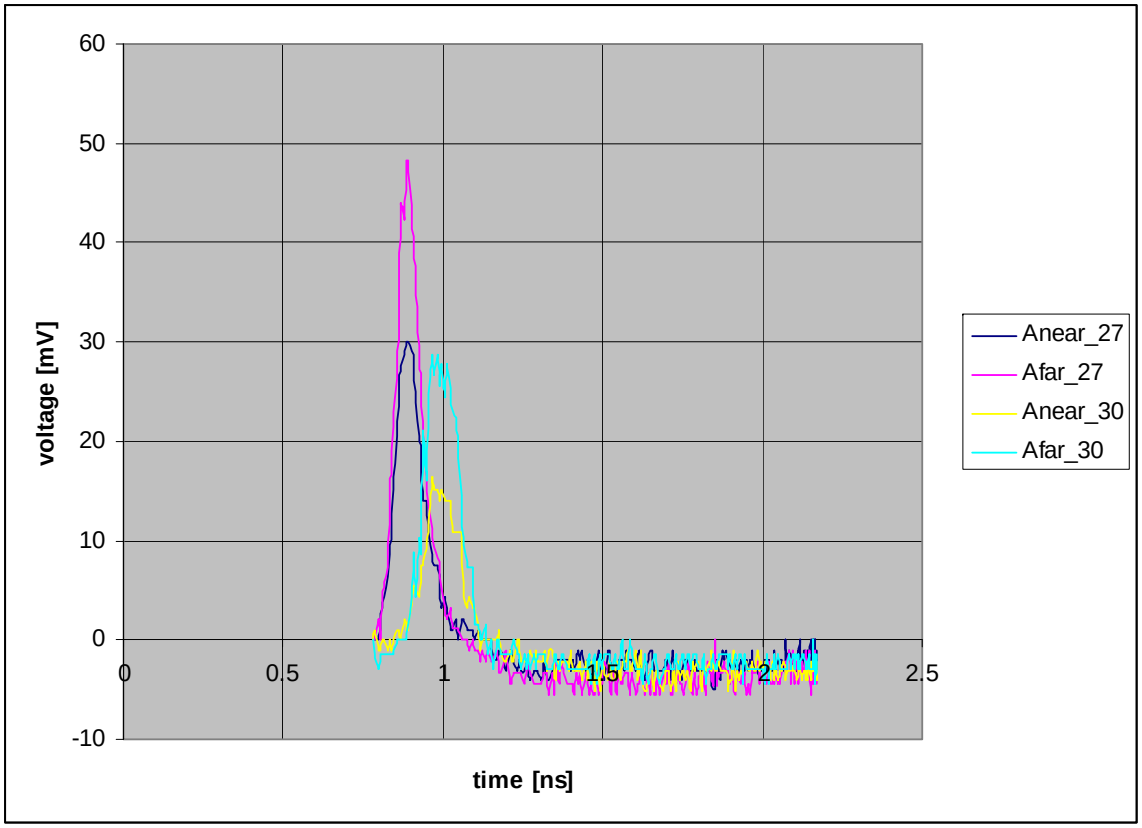


Propagation Delay (RC)



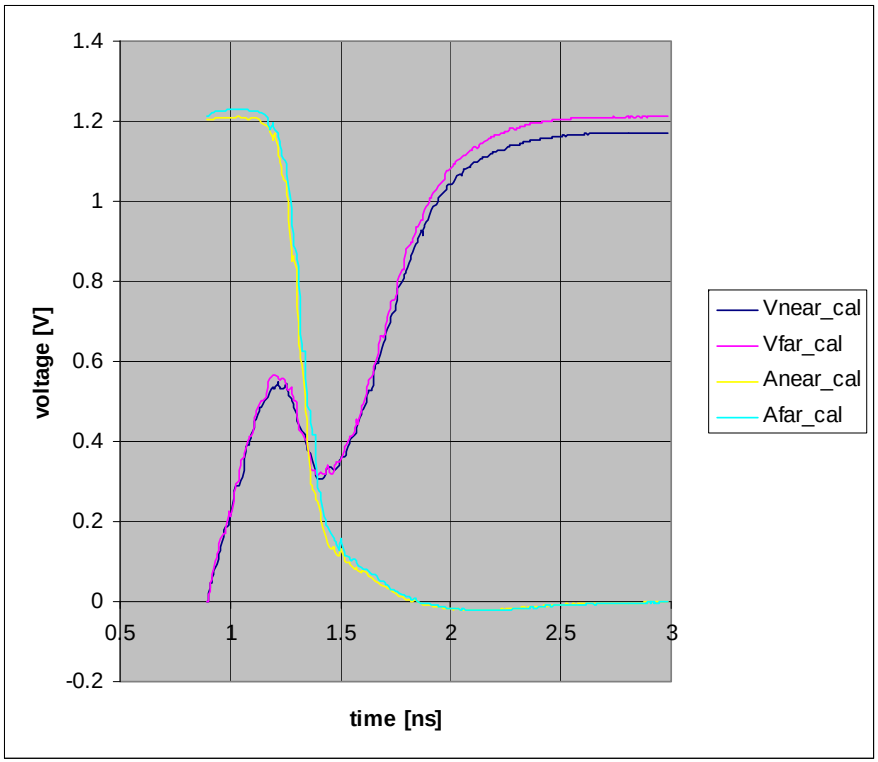
Measured and simulated values of RC delay for two line lengths, for three different metals.

Crosstalk



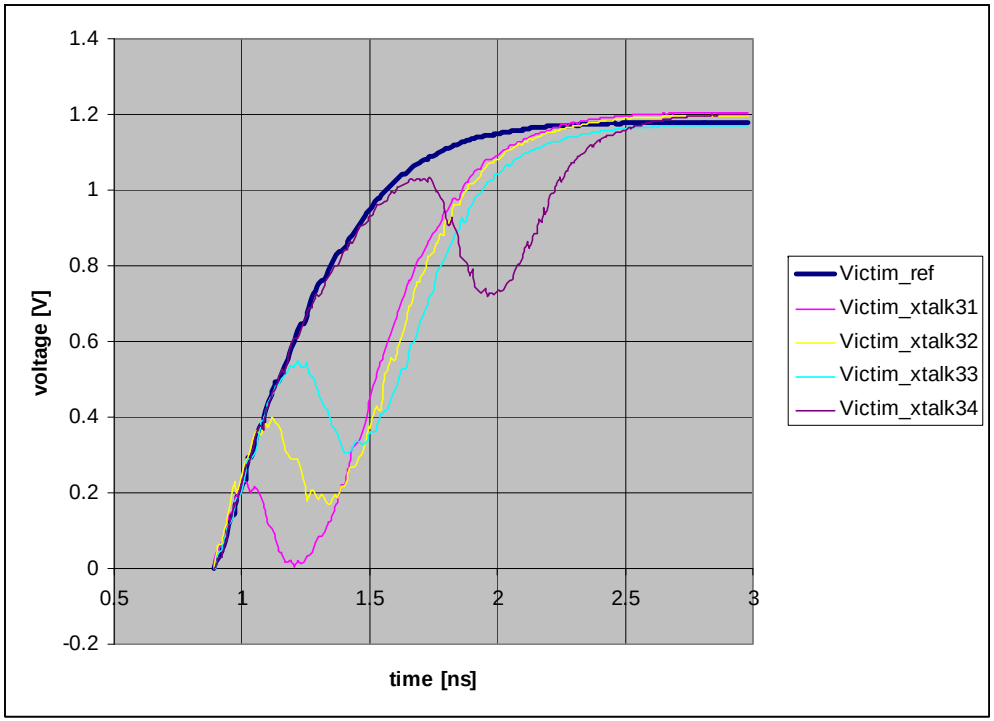
Crosstalk induced by switching of Aggresor1 on Aggressor2, for two different line spacings, shown at both near- and far-end

Crosstalk Induced Delay



Switching of victim and aggressor in opposite directions induces crosstalk delay

Crosstalk Induced Delay



Constant Crosstalk Delay induced on victim line by switching on the neighboring aggressor line in opposite direction, varying the relative switching moments of two lines

Applications

- Obtained results can be used at various stages of the design process:
  - Characterizing the interconnects and the vias (obtaining S-params from samples using FFT)
  - Deriving of critical design variables (dispersion, crosstalk tolerance margin, max coupling length, distance between repeaters, etc.)
  - Application to place & route aided design strategy
  - Application to chip-level global extraction
  - …

Electrical-Thermal AC Analysis

Electrical Analysis:

$$\nabla \times \left(\frac{1}{\mu_r} \nabla \times \mathbf{E} \right) - k_0{}^2 \epsilon_r \mathbf{E} = -j k_0 Z_0 \mathbf{J}$$

- Waveguide port boundary condition
- Absorbing boundary condition

Thermal Analysis:

$$\nabla \cdot k \nabla T = -P$$

$$T = T_c \qquad \text{on } \Gamma_{\text{tc}}$$

$$k \frac{\partial T}{\partial n} = -h(T - T_a) \qquad \text{on } \Gamma_{\text{conv}}$$

Electrical-Thermal DC Analysis

Electrical Analysis:

$$\nabla \cdot \sigma \nabla \phi = 0$$

$$\phi = \phi_c \quad \text{on } \Gamma_{\text{vc}}$$

$$\sigma \frac{\partial \phi}{\partial n} = \frac{\phi}{RS} \quad \text{on } \Gamma_{\text{load}}$$

Thermal Analysis:

$$\nabla \cdot k \nabla T = -P$$

$$T = T_c \quad \text{on } \Gamma_{\text{tc}}$$

$$k \frac{\partial T}{\partial n} = -h(T - T_a) \quad \text{on } \Gamma_{\text{conv}}$$

Electrical Analysis:

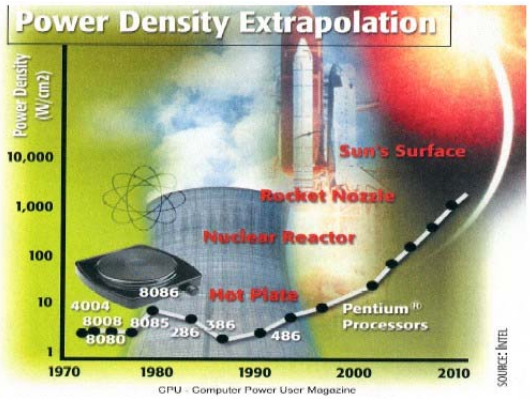
- DC
- AC
- Transient

Thermal Analysis:

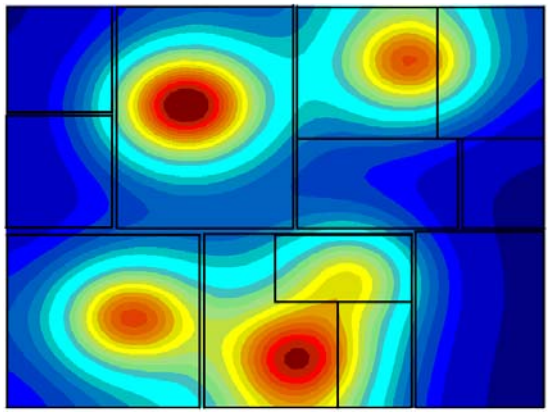
- steady-state
- Transient

Electro-Thermal Analysis. Motivation

- 3D integration technologies
  - 3D stacked IC designs
  - Increased power density
  - Heat removal difficulties



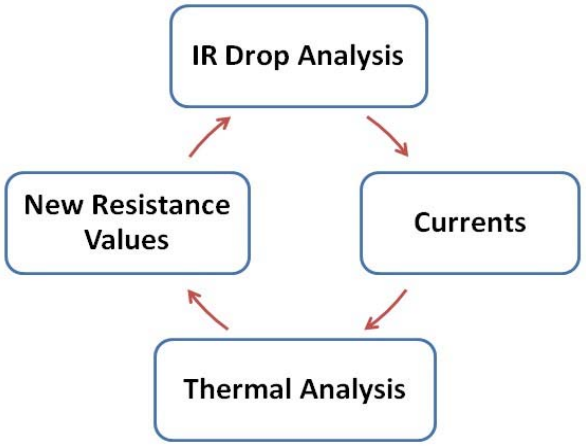
- Design challenges due to thermal issues
  - Electrical reliability (electro-migration)
  - Power delivery (IR drop)
  - Signal propagation (RC delay)
  - Memory retention time (Leakage)



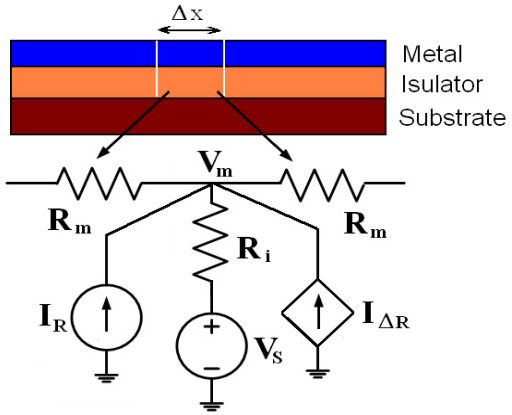
- Lack of suitable CAD tools
  - Thermal-aware design at the earliest stages
  - Using the floor plan and early power distribution analysis (know the current distribution – want to use that information)

Temperature-Dependent IR Drop

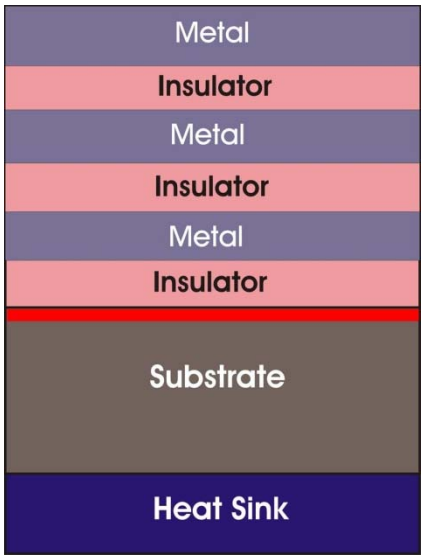
- Interconnect resistance depends on temperature → Current depends on resistance → Temperature depends on current → …
- Temperature-dependent phenomena must be accounted for
  - **Sources of heat**
    - **Self heating (Joule)**
    - **Heating from the substrate (from active devices)**



The flow of thermal-aware [8] IR drop analysis



Lumped model of the interconnect thermal system [9]

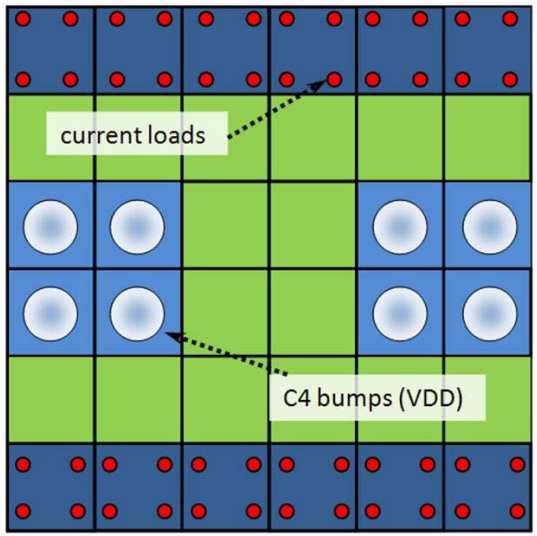


Multilayered structure of an IC

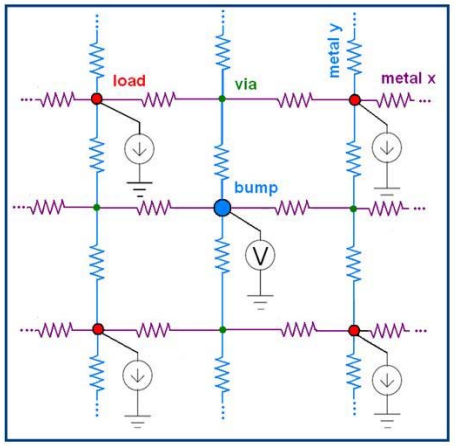
[8] Y. Zhong and M. D. F. Wong, "Thermal-aware IR drop analysis in large power grid," *IEEE ISQED*, 2008, pp. 194-199

[9] C. C. Teng, Y. K. Cheng, E. Rosenbaum, and S. M. Kang, "iTEM: A temperature-dependent electromigration reliability diagnosis tool," *IEEE Trans. Computer-Aided Design*, vol. 16, pp. 882–893, Aug. 1997.

Pre-Layout IR Drop Analysis



Floor plan and pad out

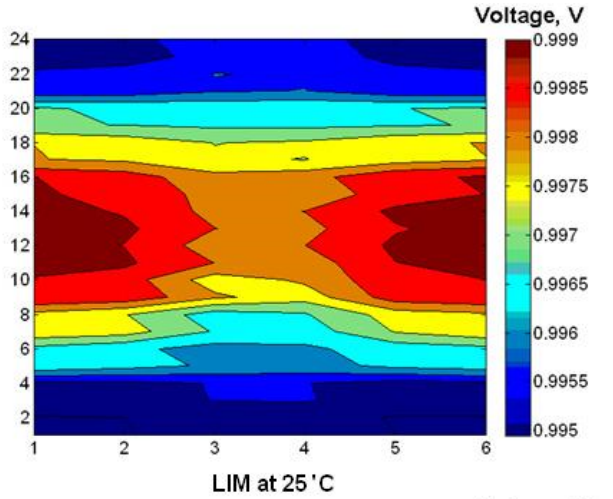


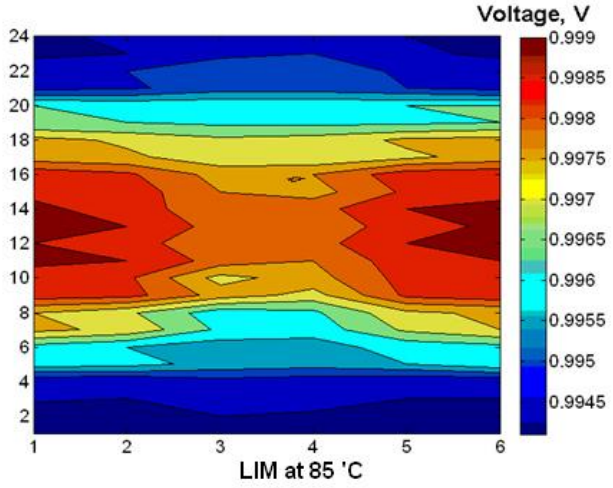
Equivalent circuit for a single segment

Example based on a segment of the actual Rambus test-chip

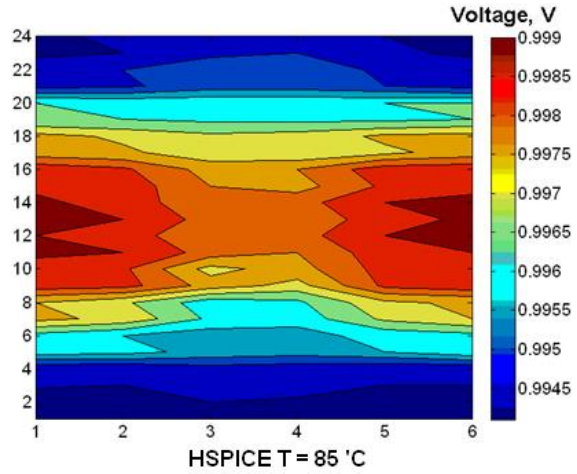
- PDN parameters are in the form of
  - process parameters
  - floor plan
  - pad out
  - current load
  - voltage budget
- Floor plan is divided into segments
- Each segment is modeled with a resistive grid
- A script is used to generate the equivalent circuit model
- Once the circuit representation is available a circuit solver can be used to perform static IR drop analysis

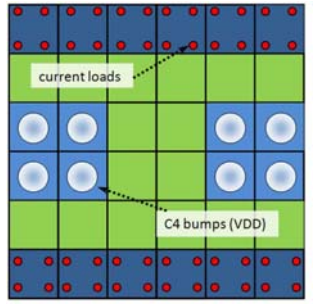
Pre-Layout IR Drop Analysis

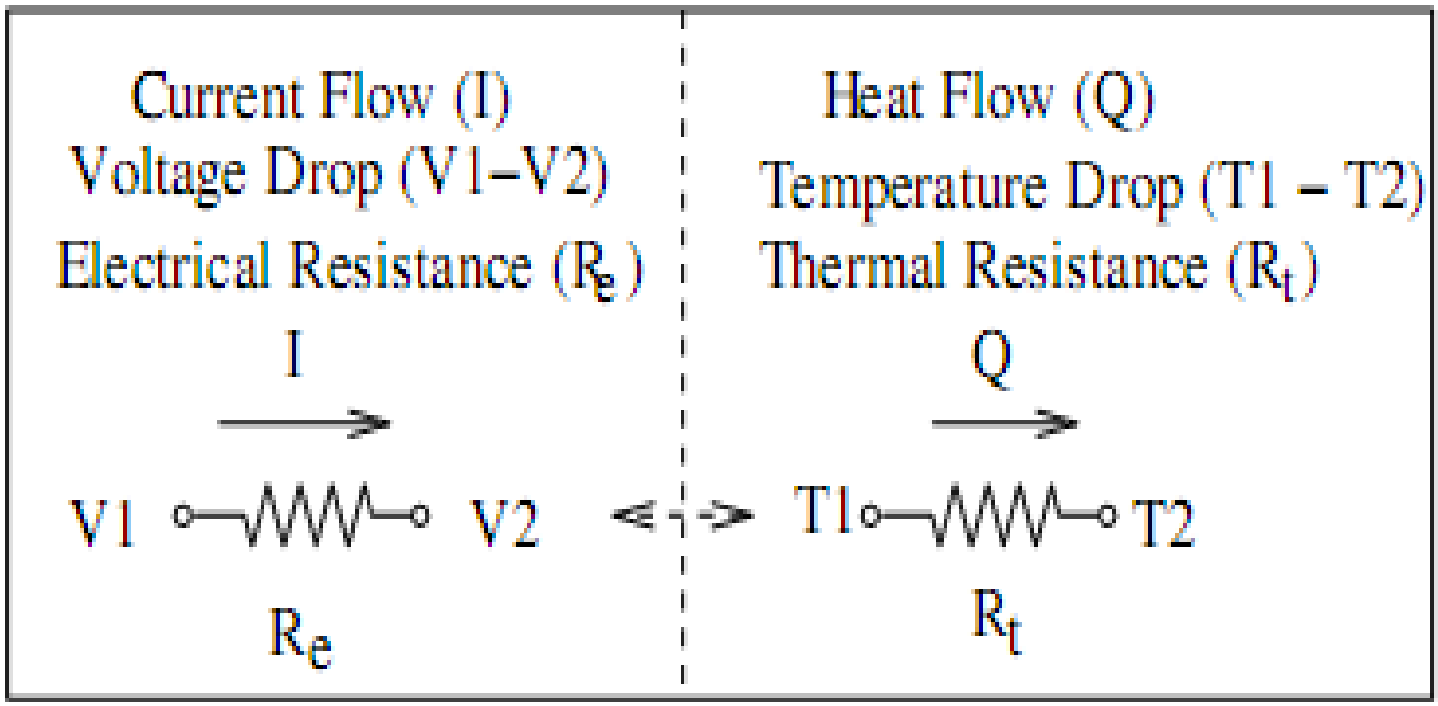




- Nominal VDD voltage of 1V is used
- Voltage drop is smaller at the locations of the bumps and becomes higher as the distance from the VDD pads increases
- Two simulations are performed at 25 °C and 85 °C
- LIM simulation at 85 °C is verified with HSPICE
- For this particular example temperature has noticeable but minor effect on the IR drop
- No thermal-electrical iterations are performed

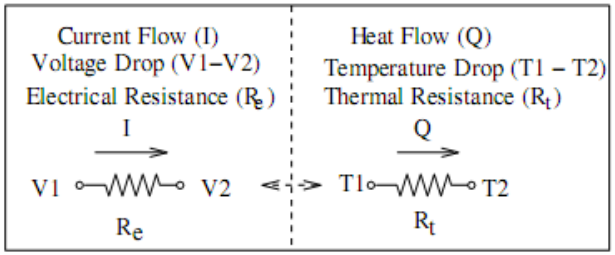





Current Flow (I)
Voltage Drop (V1–V2)
Electrical Resistance (R_e)
I
V1
V2
R_e
Heat Flow (Q)
Temperature Drop (T1 – T2)
Thermal Resistance (R_t)
Q
T1
T2
R_t

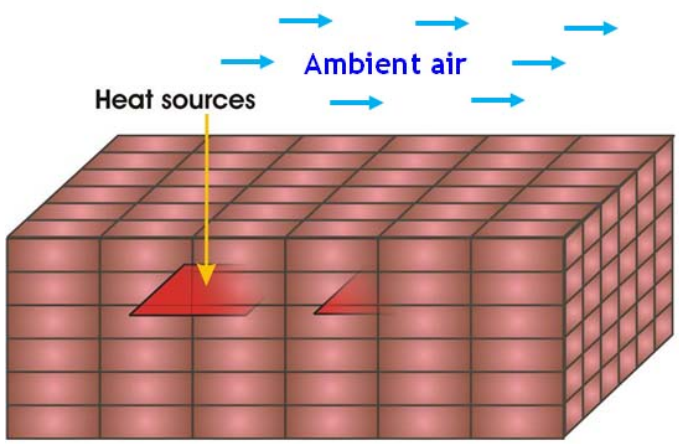
Temperature distribution in IC structure

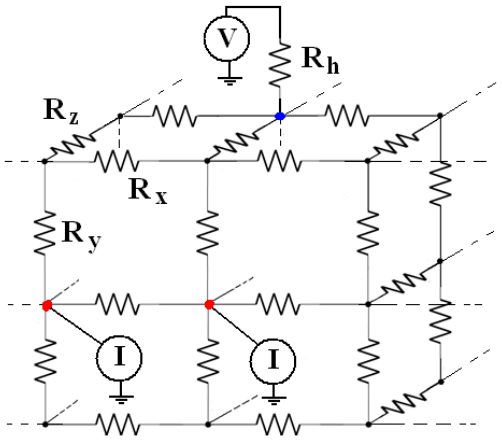
- **Modeling methodology**
  - Use thermal – electrical analogy
  - Thermal problem → electrical circuit
  - Bulk of the material → 3D Resistive network
  - Heat sources → Constant current sources
  - Convective boundaries → Effective resistances
  - Ambient temperature → Constant voltage sources



$$R_x = \frac{\Delta x}{kA}\left[\frac{^oC}{W}\right]$$

$$R_h = \frac{1}{h_e A}\left[\frac{^oC}{W}\right]$$



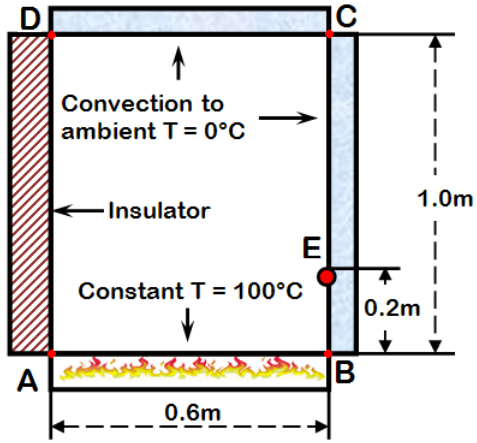


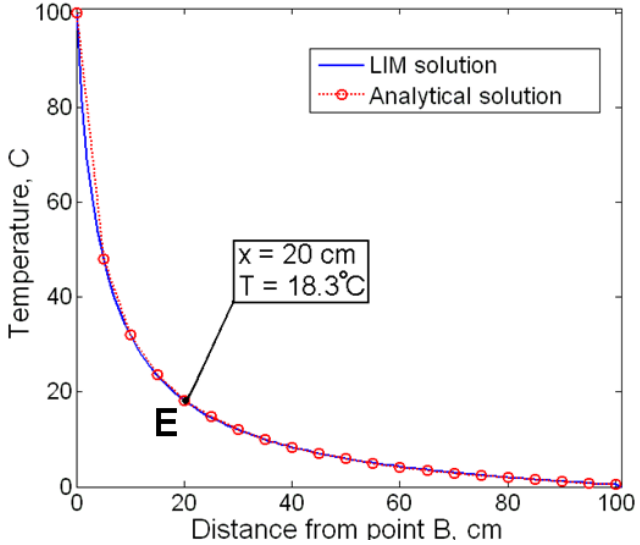
Apply circuit solver

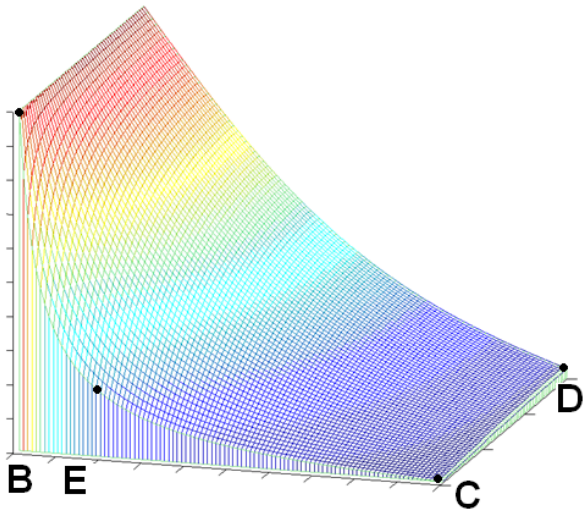
- **Solve the resulting network for node voltages**
  - A major issue – the SIZE of the model

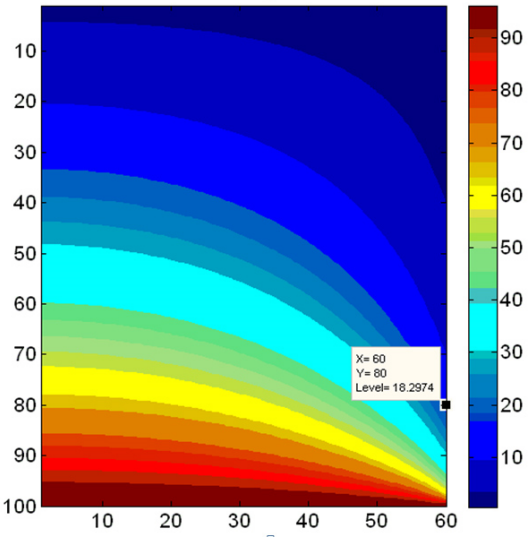
Benchmark Thermal Problem

- 2D benchmark problem (NAFEMS)
  - Simple geometry
  - Has all typical components
  - There is analytical solution
  - Target temperature at E is 18.3 °C



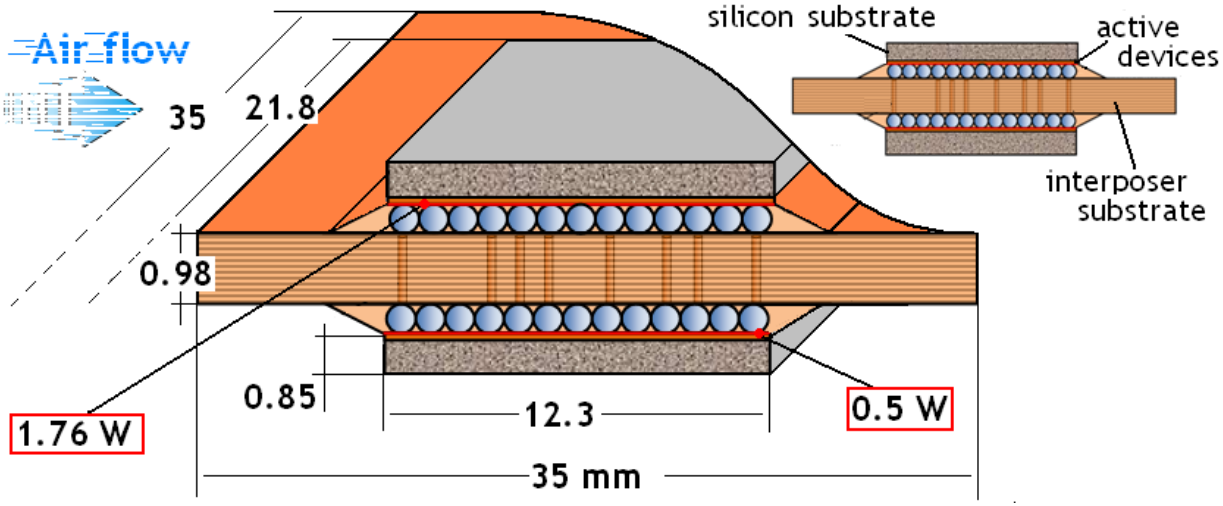


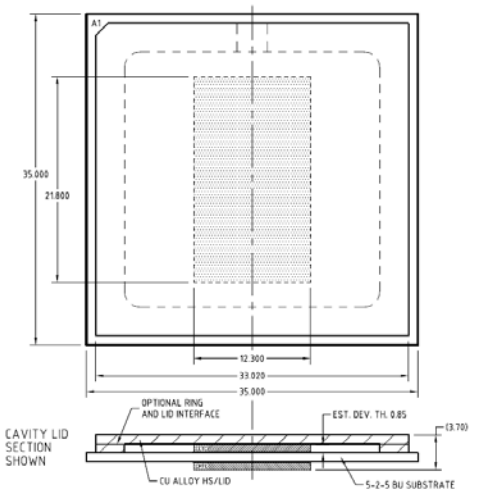




[10] Davies, G.A.O. and Fenner, R. T. and Lewis, R. W., *Background to benchmarks*, NAFEMS, 1993

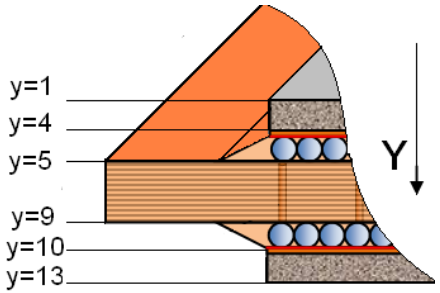
3D Structure. Chip-Interposer-Chip





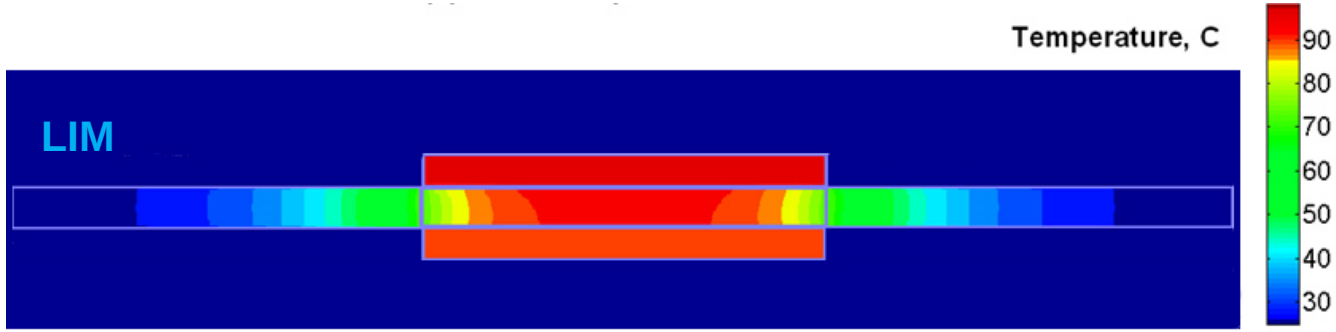
- How hot does the system get ?
- How much heat is transferred from the top chip (controller) to the bottom (memory) ?
- If the via density or distribution is changed, how does that affect the temperature distribution ?
- How much heat can be dissipated through the interposer substrate ?

Model parameters	
Unit cell size (cube)	Δx = 0.2833 mm
Number of nodes	135,089
Number of branches	326,168
Total number of elements	**461,257**

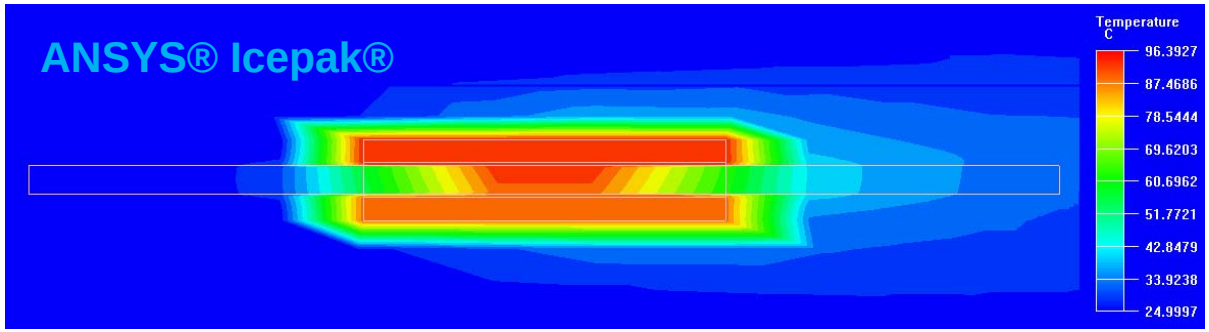


Results of the simulation

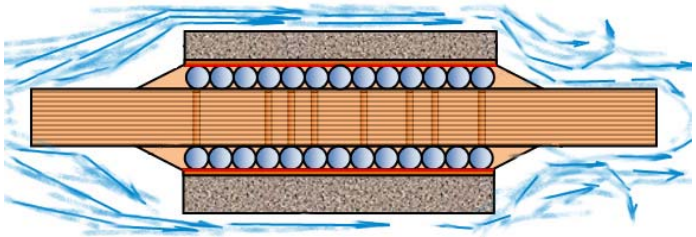
- **LIM simulation results in a symmetric temperature profile**



- **Icepak result is not symmetric**

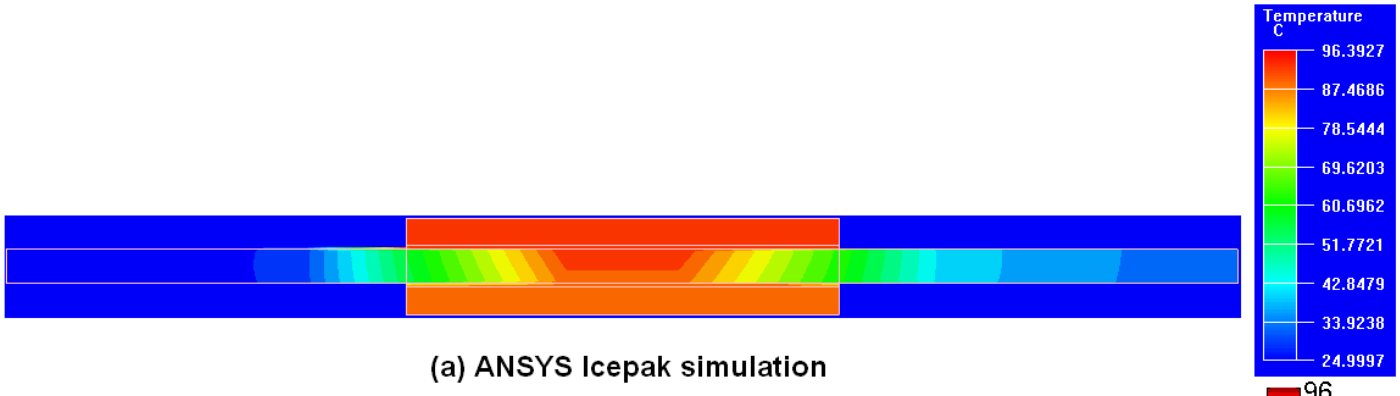


- **We need to account for non-uniform cooling**

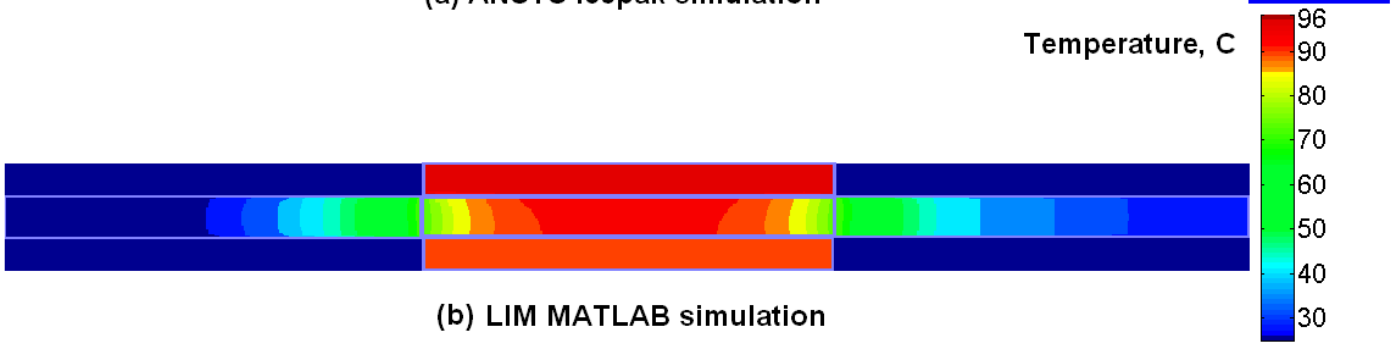


Results with non-uniform cooling

- Cross section of the 3D structure (center cut)
  - Comparison between two pictures from different tools
  - Looking for correct temperature range and general distribution (color maps used by the tools are not exactly the same)
  - In general, very good correlation is observed



(a) ANSYS Icepak simulation

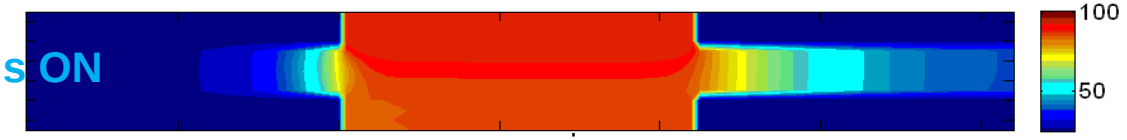


(b) LIM MATLAB simulation

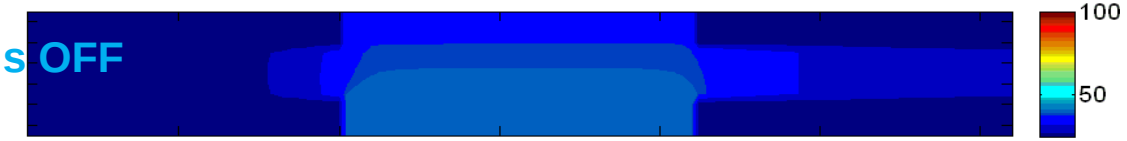
More Results

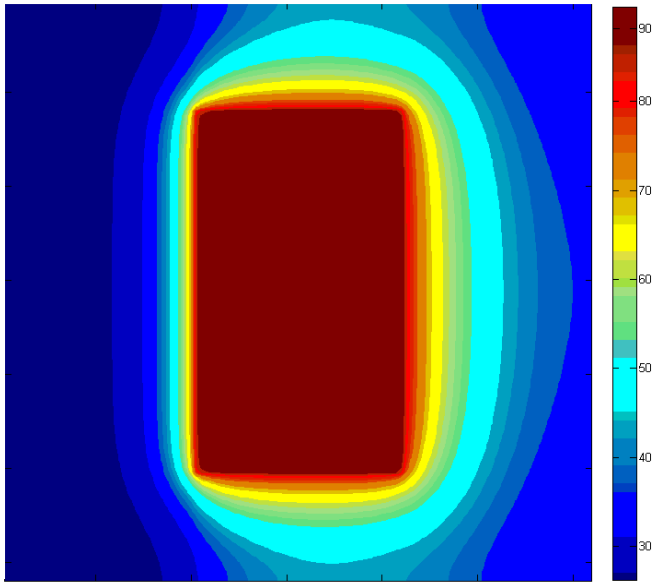
- Can look at two scenarios

Controller chip is ON

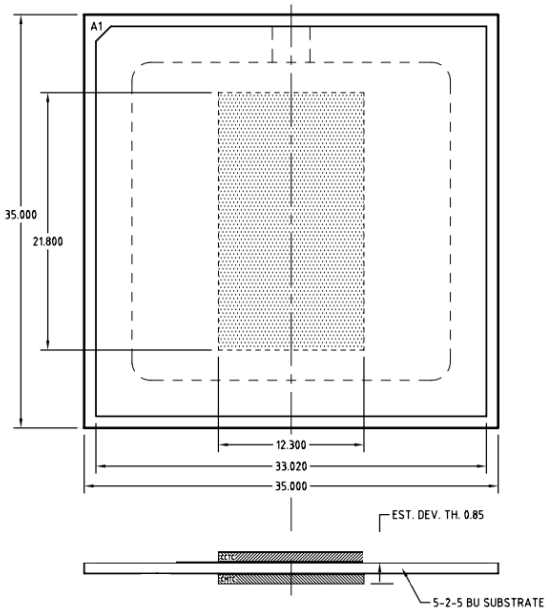


Controller chip is OFF





Steady-state temperature profile.
Top view of the structure



- In our 3D model we can observe any cross-section of the structure

Model Size Issues

- Mesh density considerations
  - coarse mesh results in errors in heat flux calculation
  - geometry of the structure
  - structure of the underlying PDN
  - sizes of elements of interest (TSVs, solder balls, etc.)

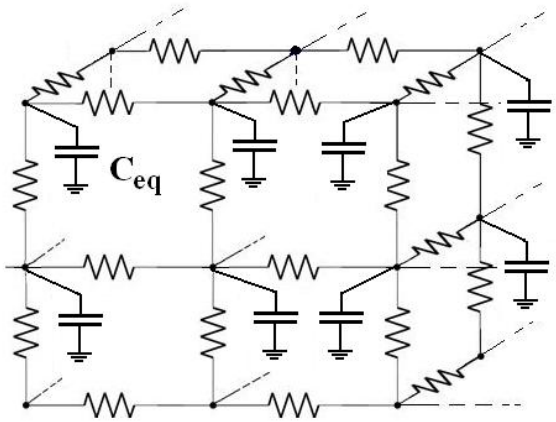
#	Elements	Run time LIM (C++)	Run time LIM (MATLAB)	Run time HSPICE 2010
1	461,257	7	16	27 (total)
2	3,514,400	65	154	949 (total)

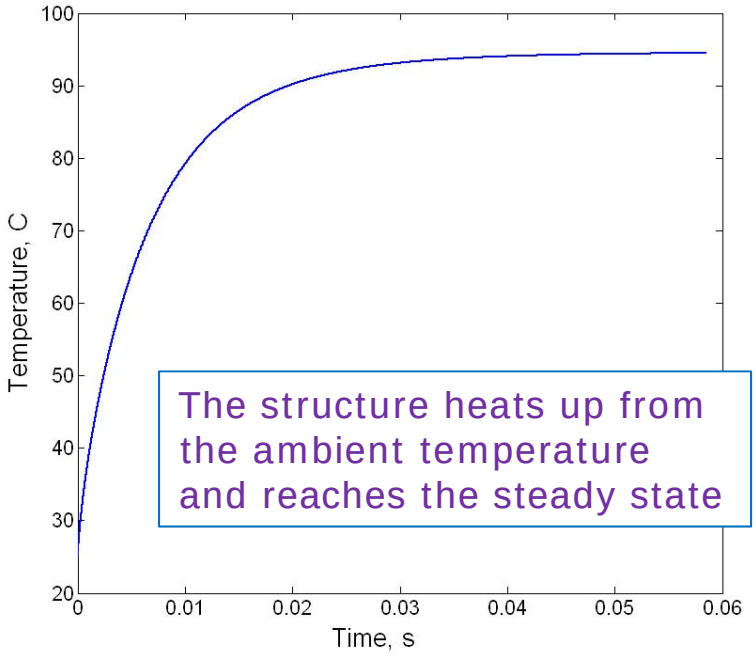
- Typically the size of the equivalent circuit is very large
- Traditional solvers (SPICE) do not scale well with the size of the model

Transient results

- Transient analysis is naturally performed by the LIM
- Insert the actual capacitance instead of fictitious

$$C_{eq} = c_p \cdot \rho \Delta x^3 \left[\frac{W \cdot s}{^oC} \right]$$





- Dynamic heat management through workload distribution
- Cooling management