ECE 546
Lecture 12
Integrated Circuits

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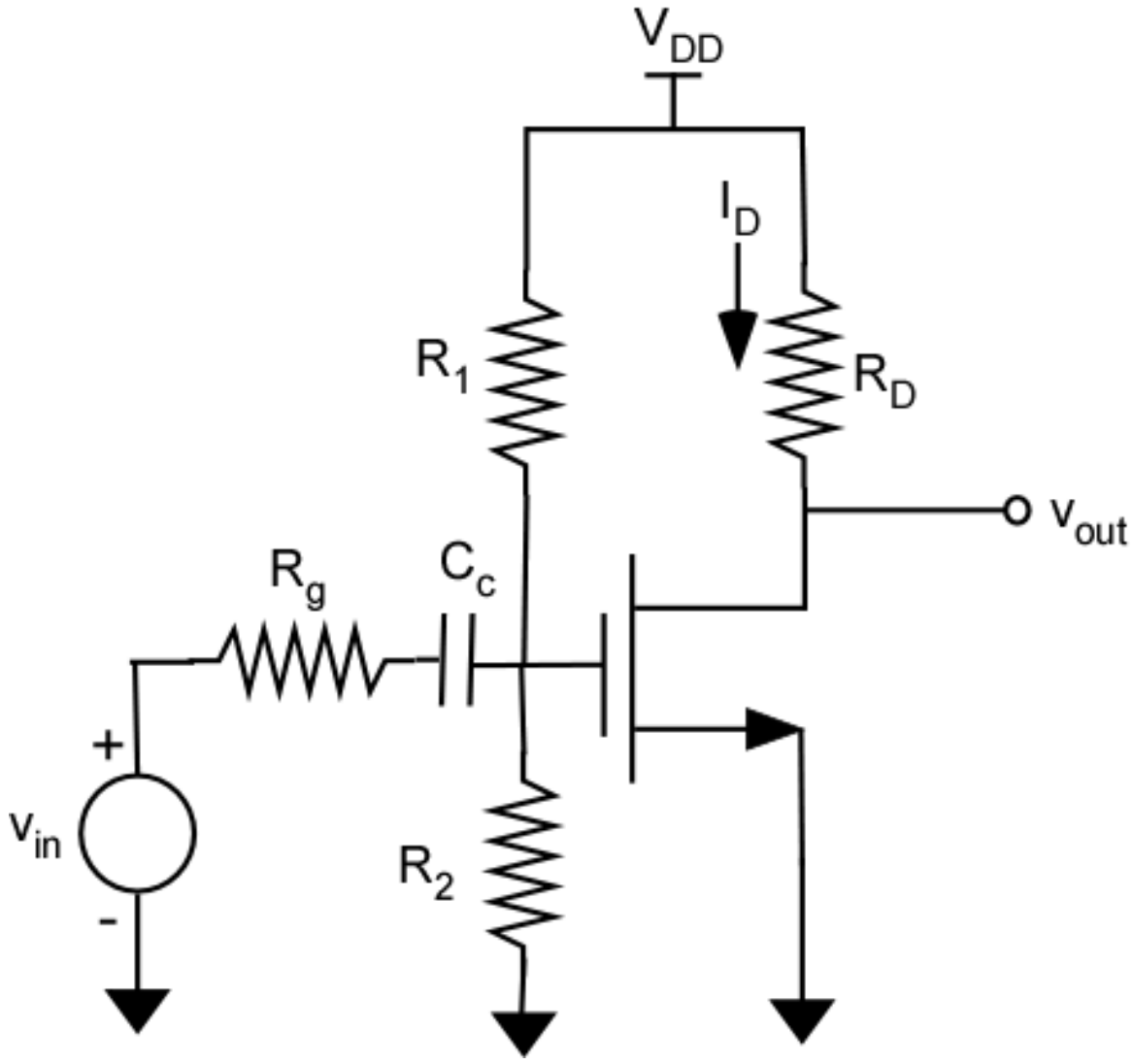
Integrated Circuits

- **IC Requirements**
  - Biasing of ICs is based on the use of constant current sources
  - Use current mirrors
  - Source circuits are used as loads

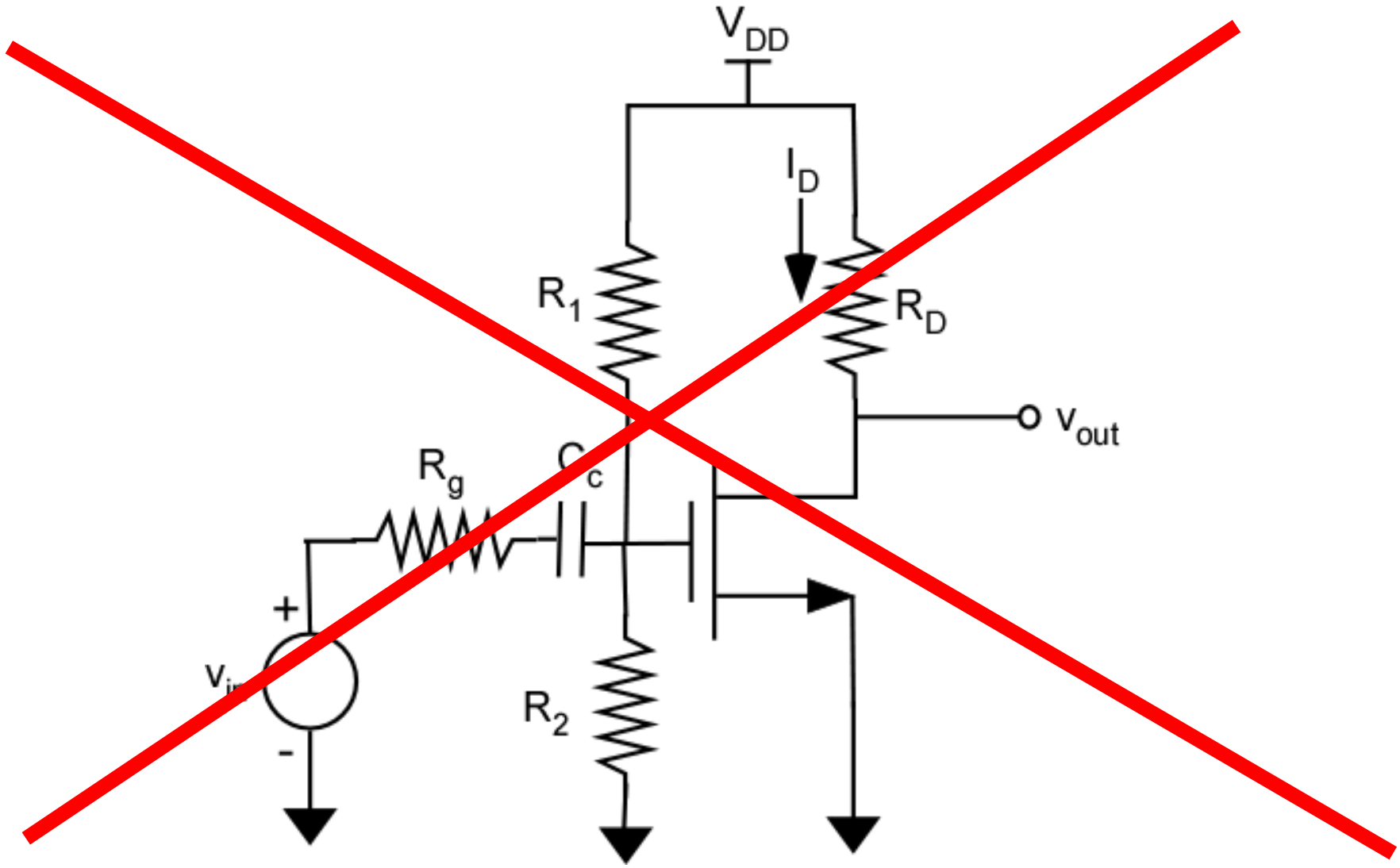
Integrated Circuits

- **Analog Design Requirements**
  - Analog ICs may need resistors and capacitors for the design of amplifiers
  - Resistors and capacitors occupy the space of tens or hundreds of MOS devices
  - It is important to minimize their use

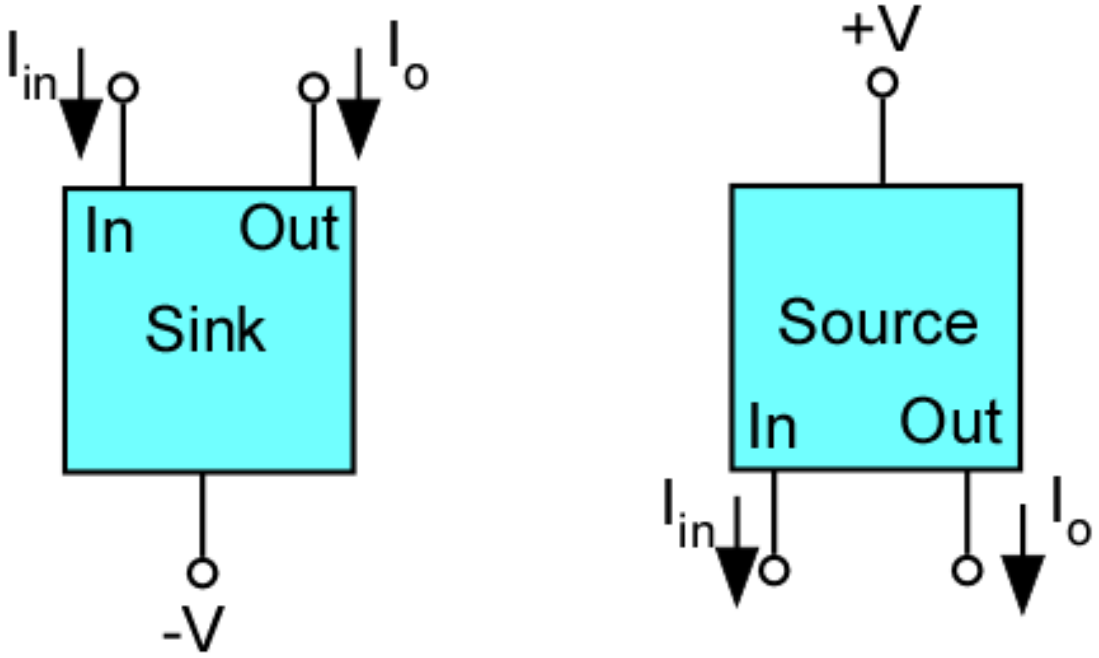
Transistor Biasing



Transistor Biasing

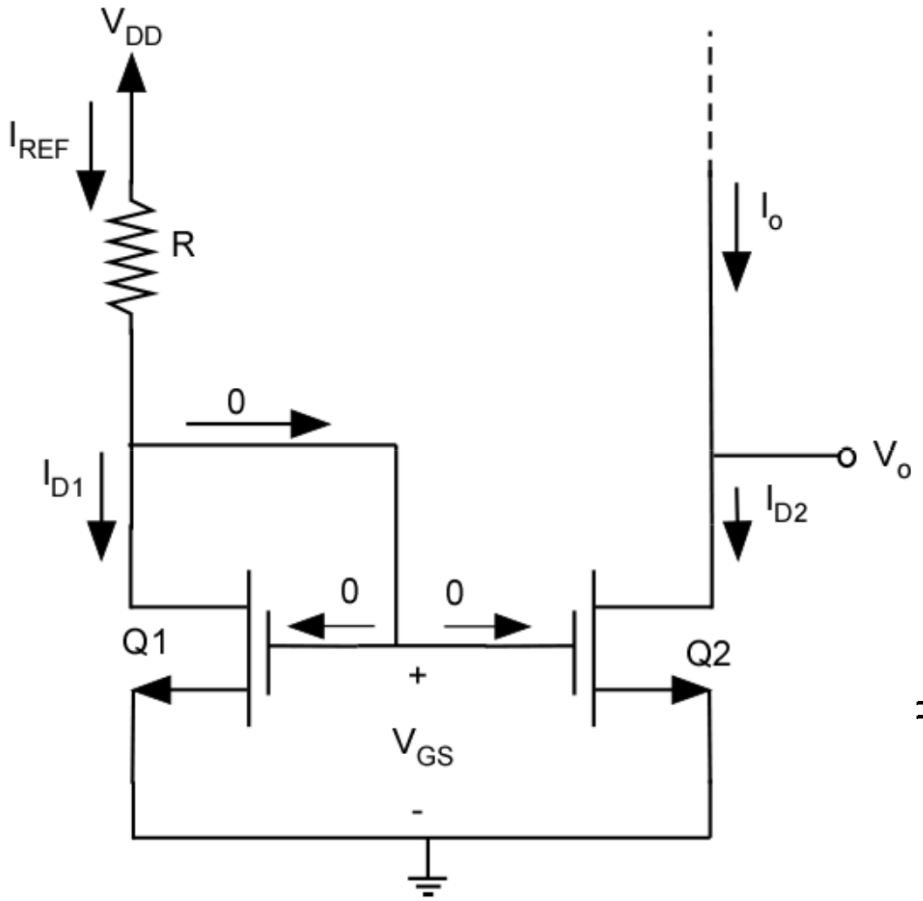


Current Mirrors



A current mirror will reproduce a reference current to the output while allowing the output voltage to assume any value within a specified range. $I_o=KI_{in}$ where K is a factor that can be less than or equal or greater than 1

MOS Current Mirror



$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L} \right)_1 \left(V_{GS} - V_{Tn} \right)^2$$

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

$$= I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L} \right)_2 \left(V_{GS} - V_{Tn} \right)^2$$

R is usually external to IC

MOS Current Mirror

Assuming that the transistors are using the same process

$$\frac{I_o}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} = \frac{W_2 L_1}{W_1 L_2}$$

- **Can be limited by**
  - Channel length modulation (λ)
  - Threshold voltage mismatch
  - Imperfect geometrical matching

MOS Current Mirror

$$\frac{I_o}{I_{REF}} = \frac{W_2 L_1}{W_1 L_2}\left[\frac{1+\lambda\left(V_{DS2}-V_{DSP2}\right)}{1+\lambda\left(V_{DS1}-V_{DSP1}\right)}\right]$$

- **Some Properties**
  1. MOS current mirrors draw zero control current➔better than BJT's
  2. Matching of threshold voltages harder than in BJT's

Example

A matched pair of MOSFETs are used in a current mirror witl λ = 0.032 V^{-1}, μC_{ox}=70 μA/V^2, $W/2L$ =10, and V_T = 0.9 V. Find the value of R to create an input current of 100 μA. Calculate the output current when V_o = 3 V.

Use drain current equation in active region to calculate

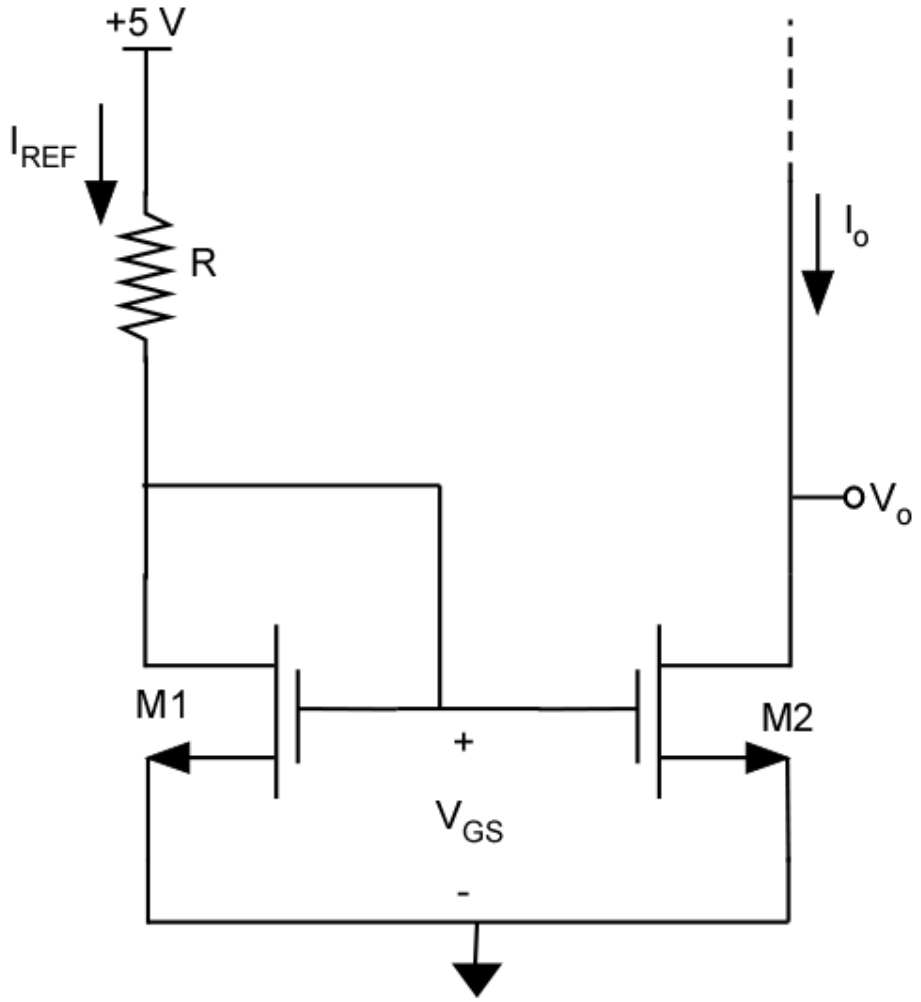
$$I_{D1} = \frac{\mu C_{ox} W}{2L}\left[V_{GS} - V_T\right]^2\left(1 + \lambda V_{DS1}\right)$$

$$I_{D1} = 100 = 700\left[V_{GS} - 0.9\right]^2\left(1 + 0.032 * V_{GS}\right)$$

We can now solve for the value of V_{GS}

Example

MOS Current Mirror



Example

V_{GS} = 1.272 V

The resistance needed is:

$$R = \frac{5 - V_{DS1}}{I_{D1}} = \frac{5 - 1.272}{0.1} = 37.2\ k\Omega$$

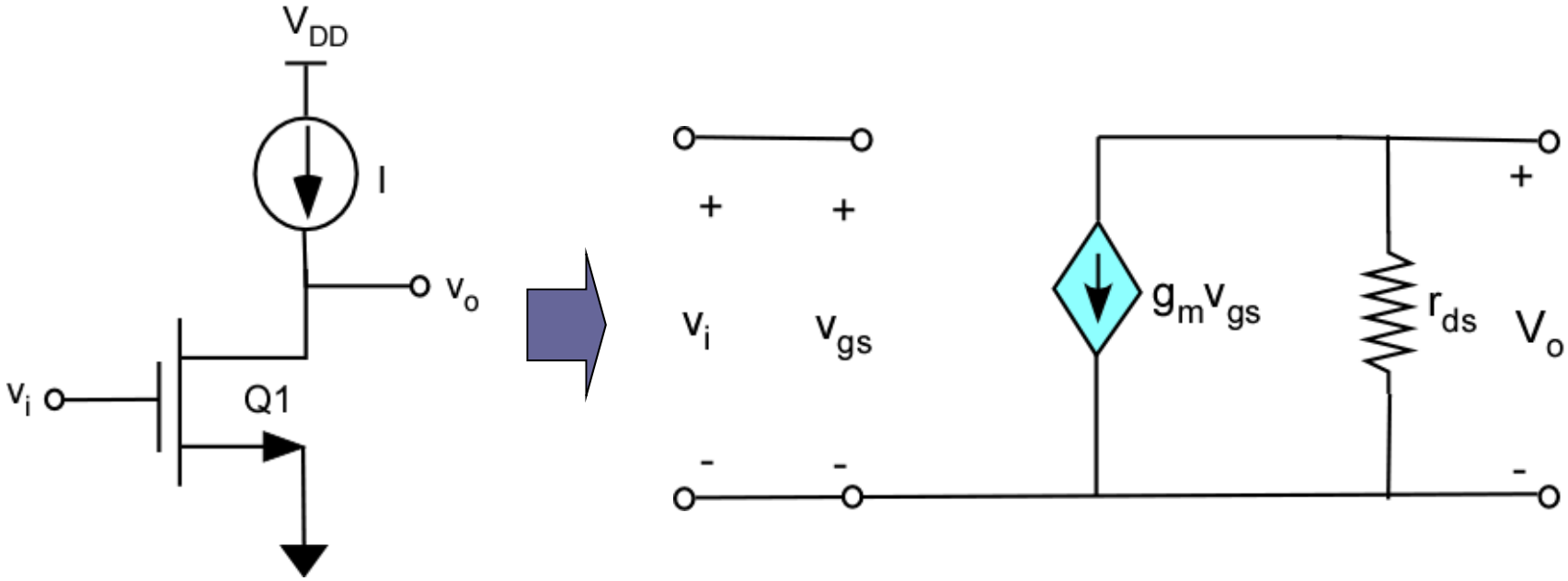
The output current is calculated from:

$$I_{D2} = \frac{\mu C_{ox} W}{2L}\left[V_{GS} - V_T\right]^2 \left(1 + \lambda V_{DS1}\right)$$

$$I_{D2} = 700\left[1.272 - 0.9\right]^2 \left(1 + 0.032 \times 3\right) = 106\ \mu A$$

$$I_{D2} = 106\ \mu A$$

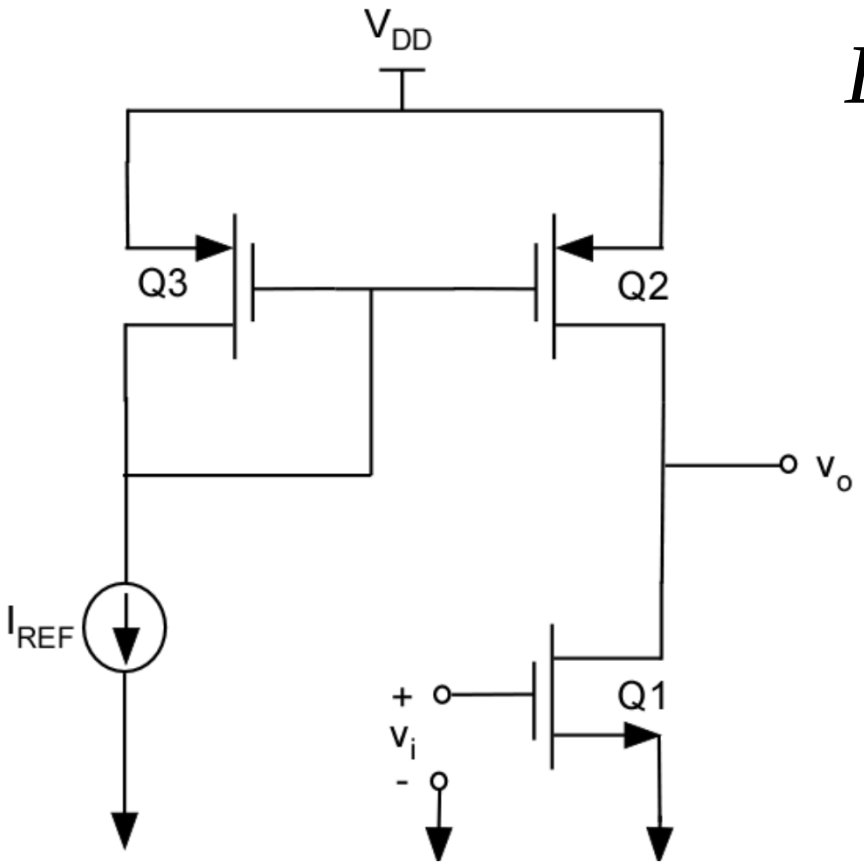
Ideal MOS Common Source CKT



$$R_i = \infty, \quad A_{vo} = -g_m r_{ds}, \quad R_o = r_{ds}$$

Intrinsic gain is $g_m r_{ds}$

PMOS Implementation of Active Load



$$Let\ r_{ds1} = r_{o1}\ \ for\ Q_1$$

$$r_{ds2} = r_{o2}\ \ for\ Q_2$$

$$then,\ R_{out} = r_{o1} \| r_{o2}$$

$$A_{MB} = -g_{m1} R_{out}$$

$$Let\ g_{o1} = \frac{1}{r_{o1}} = g_{ds1}$$

$$g_{o2} = \frac{1}{r_{o2}} = g_{ds2}$$

PMOS Implementation of Active Load

Can show that the 3dB point is given:

$$f_{2o} = \frac{\left(g_{01} + g_{02}\right)}{2\pi\left(C_{db1} + C_{db2} + C_{gd1} + C_{gd2}\right)}$$

Large incremental load leads to high gain while maintaining acceptable DC current (resistor would not work)

Background

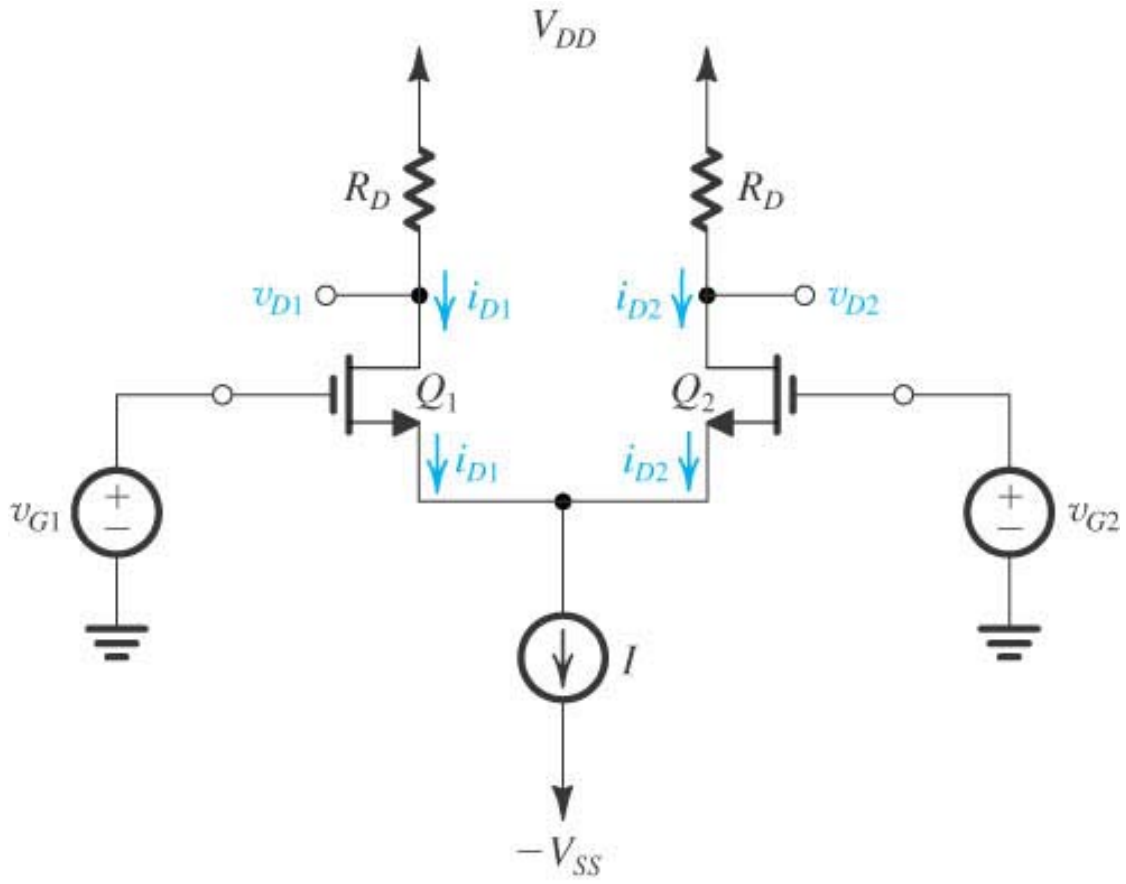
- **Differential Amplifiers**
  - The input stage of every op amp is a differential amplifier
  - Immunity to temperature effects
  - Ability to amplify dc signals
  - Well-suited for IC fabrication because
    - (a) they depend on matching of elements
    - (b) they use more components
  - Less sensitive to noise and interference
  - Enable to bias amplifier and connect to other stage without the use of coupling capacitors

Differential Amplifiers

- **Practical Considerations**
  - Both inputs to a differential amplifier may have different voltages applied to them
  - In the ideal situation with perfectly symmetric stages, the common-mode input would lead to zero output
  - Temperature drifts in each stage are often common-mode signals
  - Power supply noise is a common-mode signal and has little effect on the output signal

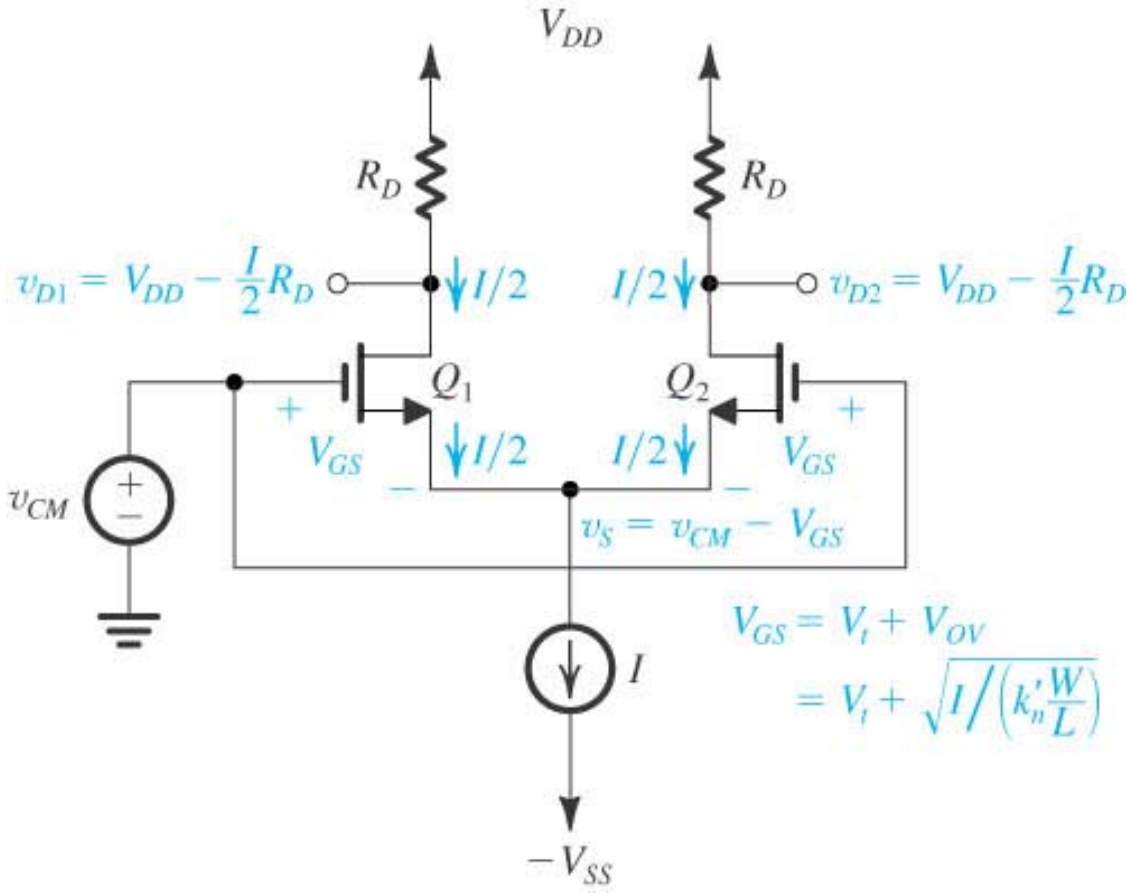
MOS Differential Pair

- Assume current source is ideal
- Transistors should not enter triode region



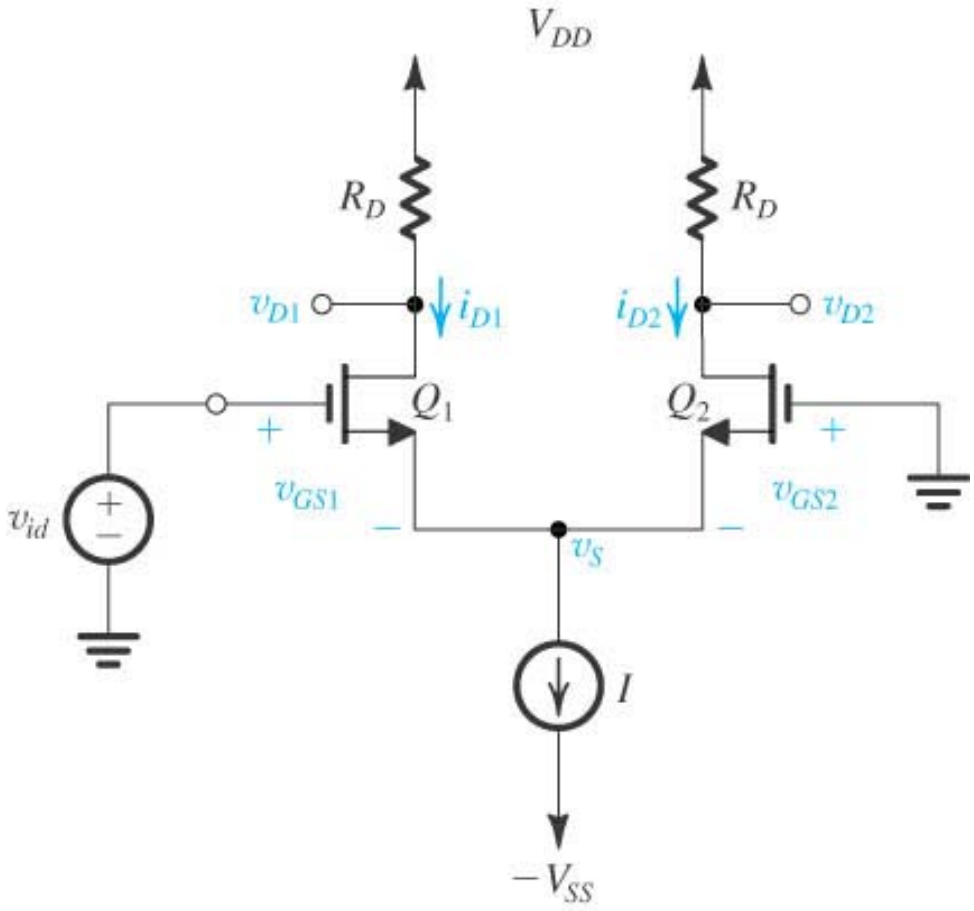
Common-Mode Operation

- Input voltage v_{cm} to both gates
- Difference in voltage between the two drains is zero

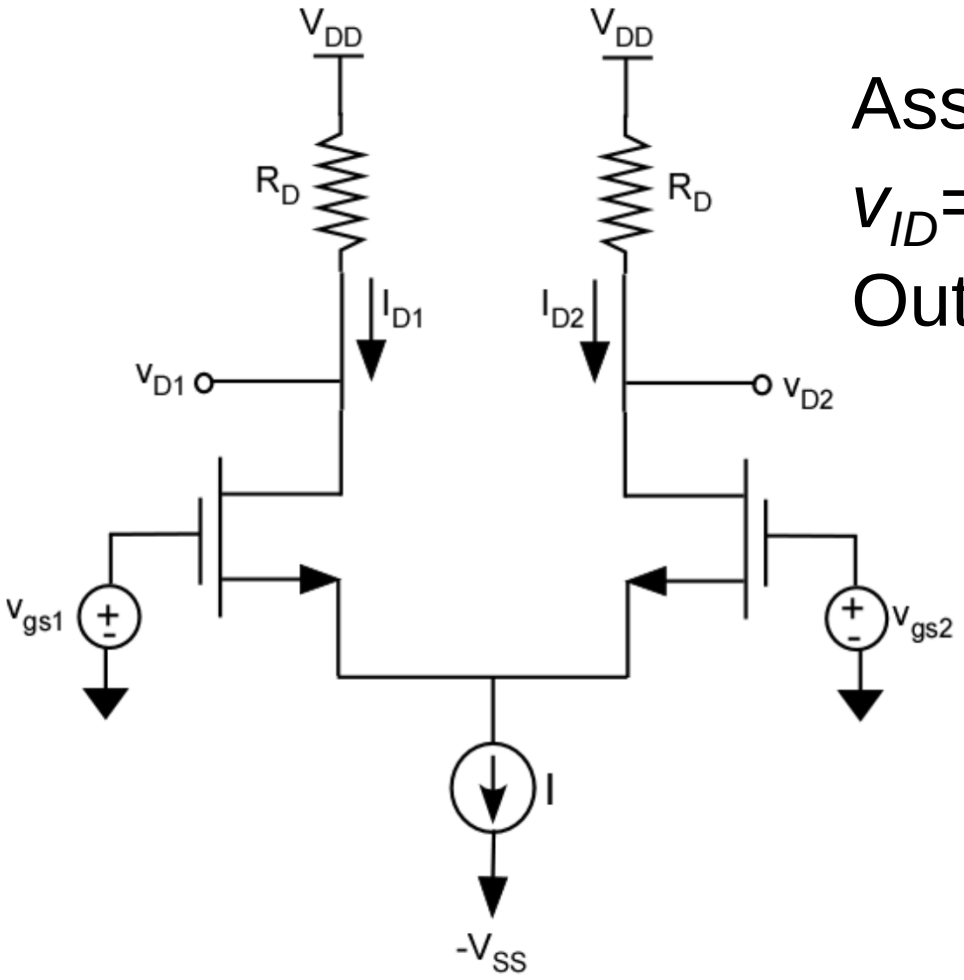


Differential Input Voltage

- Differential pair responds to differntial input signals by providing corresponding differential output signal between the two drains.



MOS Differential Pair

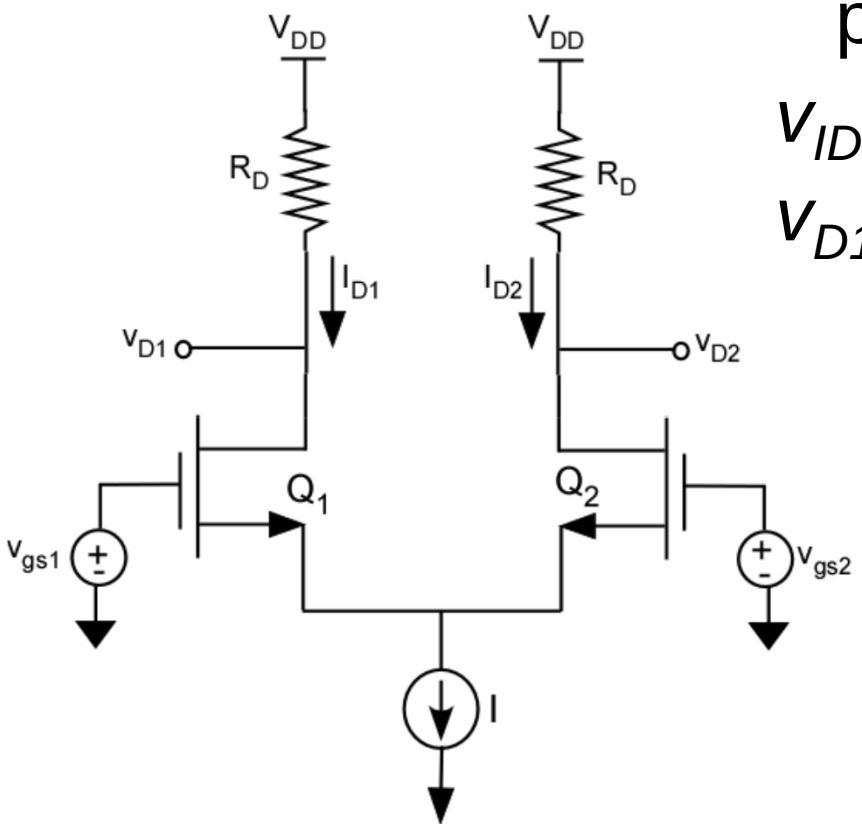


Assume current source is ideal

$v_{ID}=v_{gs1}-v_{gs2}$

Output is collected as $v_{D2}-v_{D1}$

MOS Differential Pair



- If v_{ID} is positive, v_{D2}-v_{D1} is positive

$v_{ID}>0 \rightarrow v_{gs1}>v_{gs2} \rightarrow I_{D1} > I_{D2}$

v_{D1} lower voltage point than v_{D2}

For proper operation, MOSFETS should not enter triode region

DC Analysis

$$V_{D1} = V_{DD} - \frac{IR_D}{2} \qquad V_{D2} = V_{DD} - \frac{IR_D}{2}$$

$$I_D = \frac{\mu C_{ox} W}{2L}\left(V_{GS} - V_T\right)^2 \qquad I_D = \frac{I}{2}$$

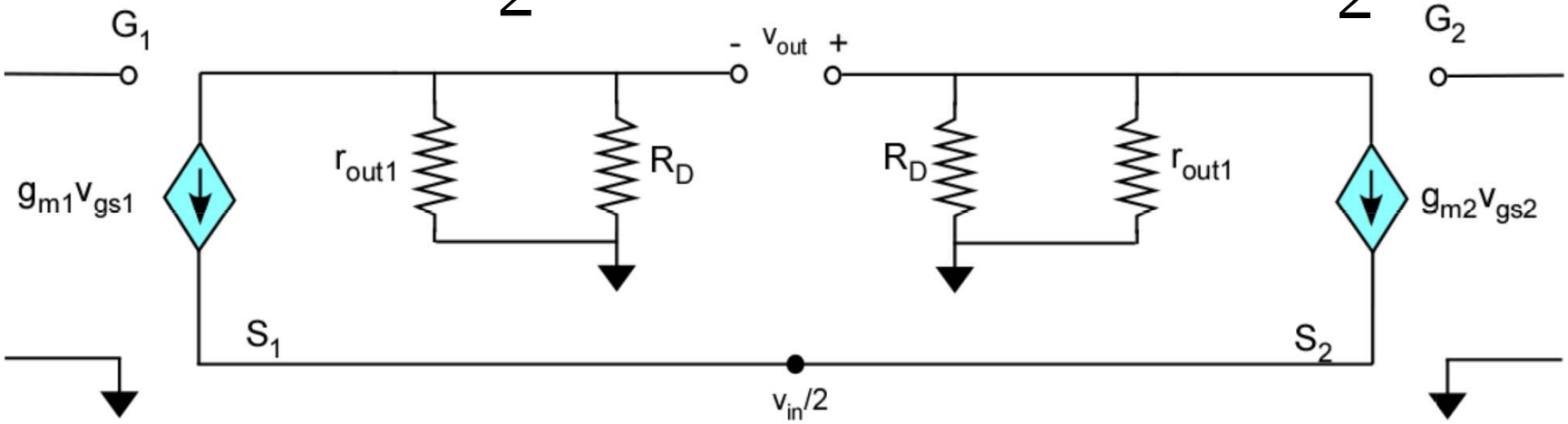
$$V_{GS} = V_T + \sqrt{\frac{LI}{\mu C_{ox} W}} \qquad V_{SQ} = -\left[V_T + \sqrt{\frac{LI}{\mu C_{ox} W}}\right]$$

Incremental Analysis

$$v_{g1} = v_{cm} + \frac{1}{2}v_{id} \qquad v_{g2} = v_{cm} - \frac{1}{2}v_{id}$$

Neglecting the body effect

$$v_{o1} = -g_m R_D' \frac{v_{in}}{2} \qquad v_{o2} = g_m R_D' \frac{v_{in}}{2}$$



$$R_D' = R_D \| r_{out} \qquad A_D = \frac{v_{o2} - v_{o1}}{v_{in}} = g_m R_D'$$

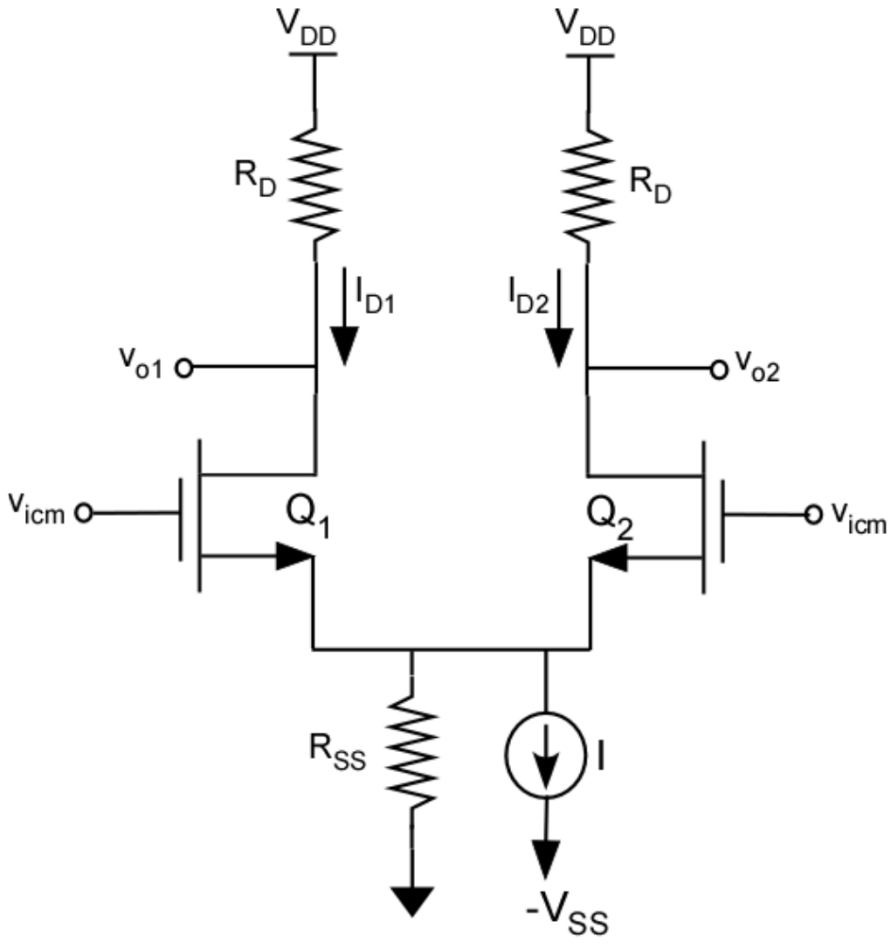
Frequency Response

When driven by a low-impedance signal source, the upper corner frequency is determined by the output circuit

$$f_{high} = \frac{1}{2\pi C_{out} R_D^{'}}$$

Common-Mode Rejection Ratio

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = \frac{R_D}{\frac{1}{g_m} + 2R_{SS}}$$



Assume $R_{SS} >> 1/g_m$

Common-Mode Rejection Ratio

(a) For ***single-ended*** output:

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \approx \frac{R_D}{2R_{SS}}$$

$$\left|A_{cm}\right| = \frac{R_D}{2R_{SS}}, \quad \left|A_d\right| = \frac{1}{2} g_m R_D$$

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| = g_m R_{SS}$$

Common-Mode Rejection Ratio

(b) For ***differential*** output:

$$A_{cm} = \frac{v_{o2} - v_{o1}}{v_{icm}} = 0$$

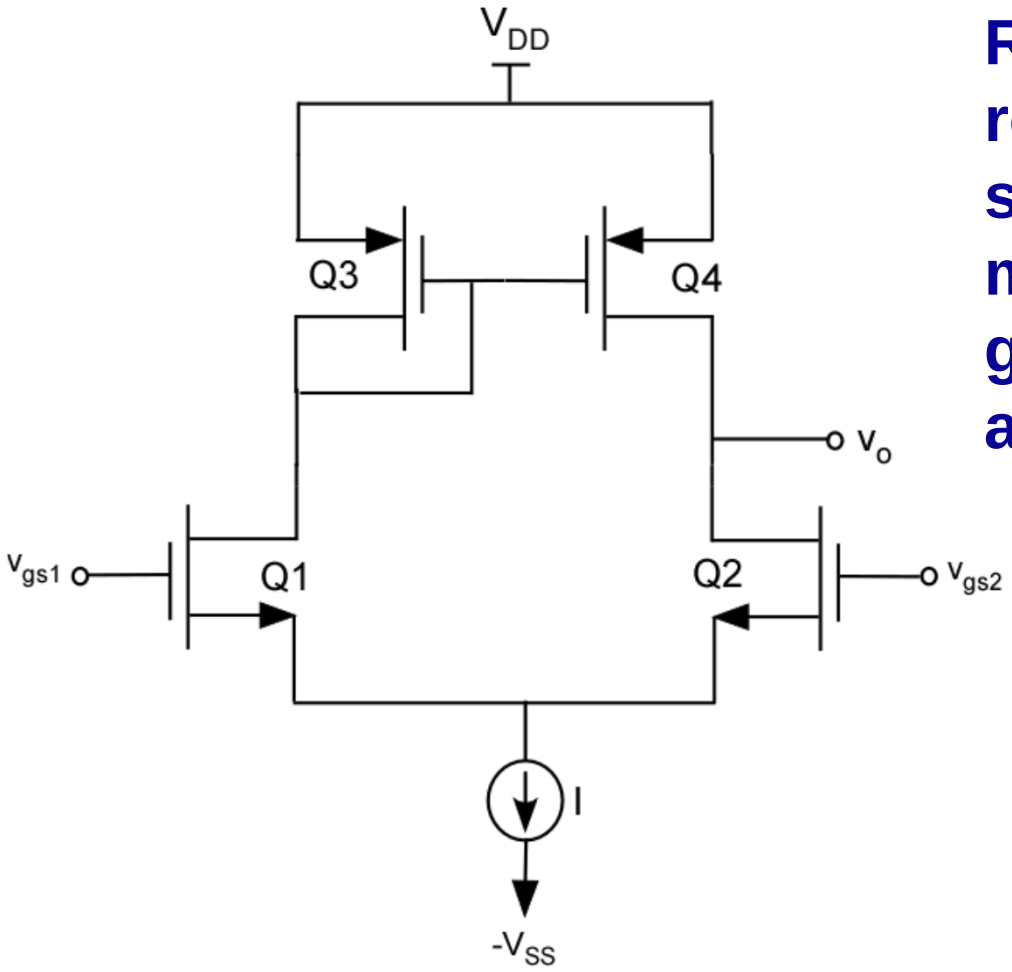
$$A_d = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

$$CMRR = \infty$$

Differential Amplifiers - Observations

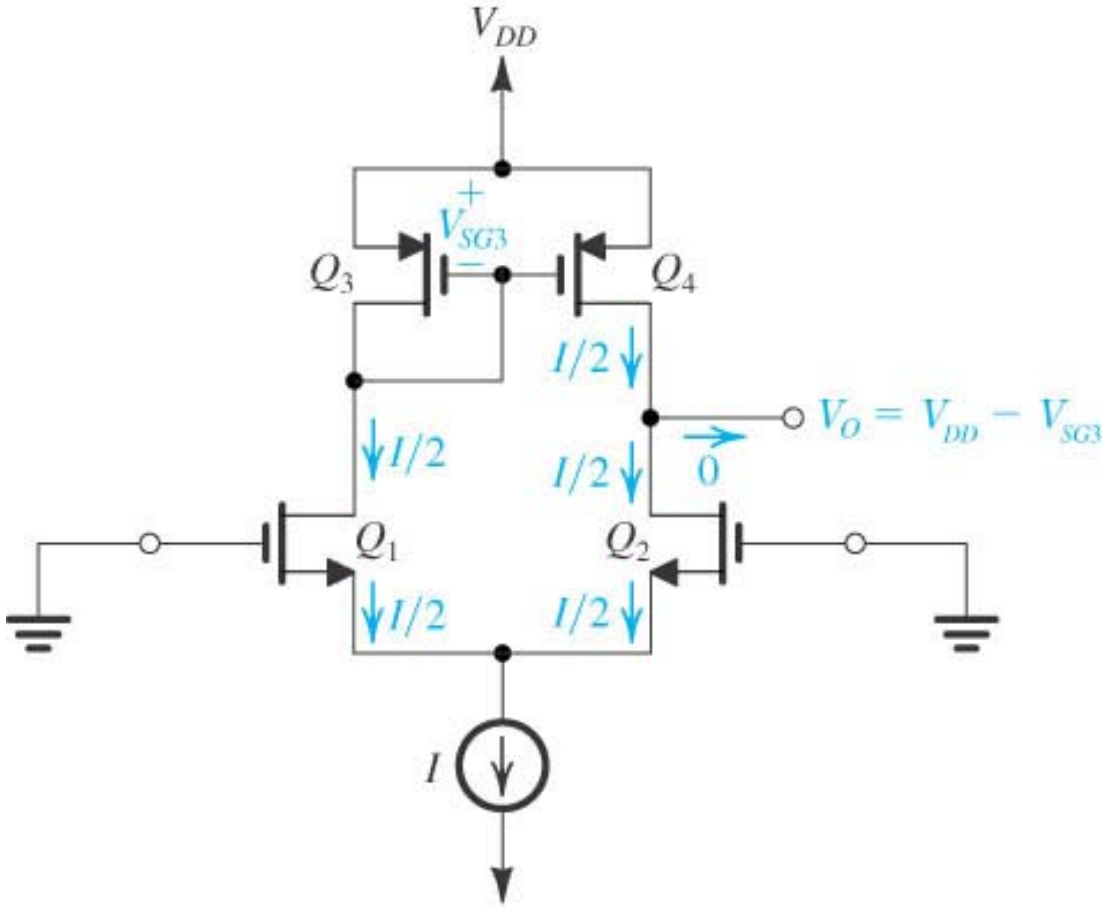
- **Observations**
  - The differential pair attenuates the input signal of each stage by a factor of one-half cutting the gain of each stage by one-half
  - The double-ended output causes the two single-ended gains to be additive
  - Thus, the voltage gain of a perfectly matched differential stage is equal to that of a single stage

MOS Differential Amp with Active Load



Replacing drain resistances with current sources, results in much higher voltage gain and savings in chip area in diff amp

MOS Differential Amp - Equilibrium



MOS Differential Amp with Active Load

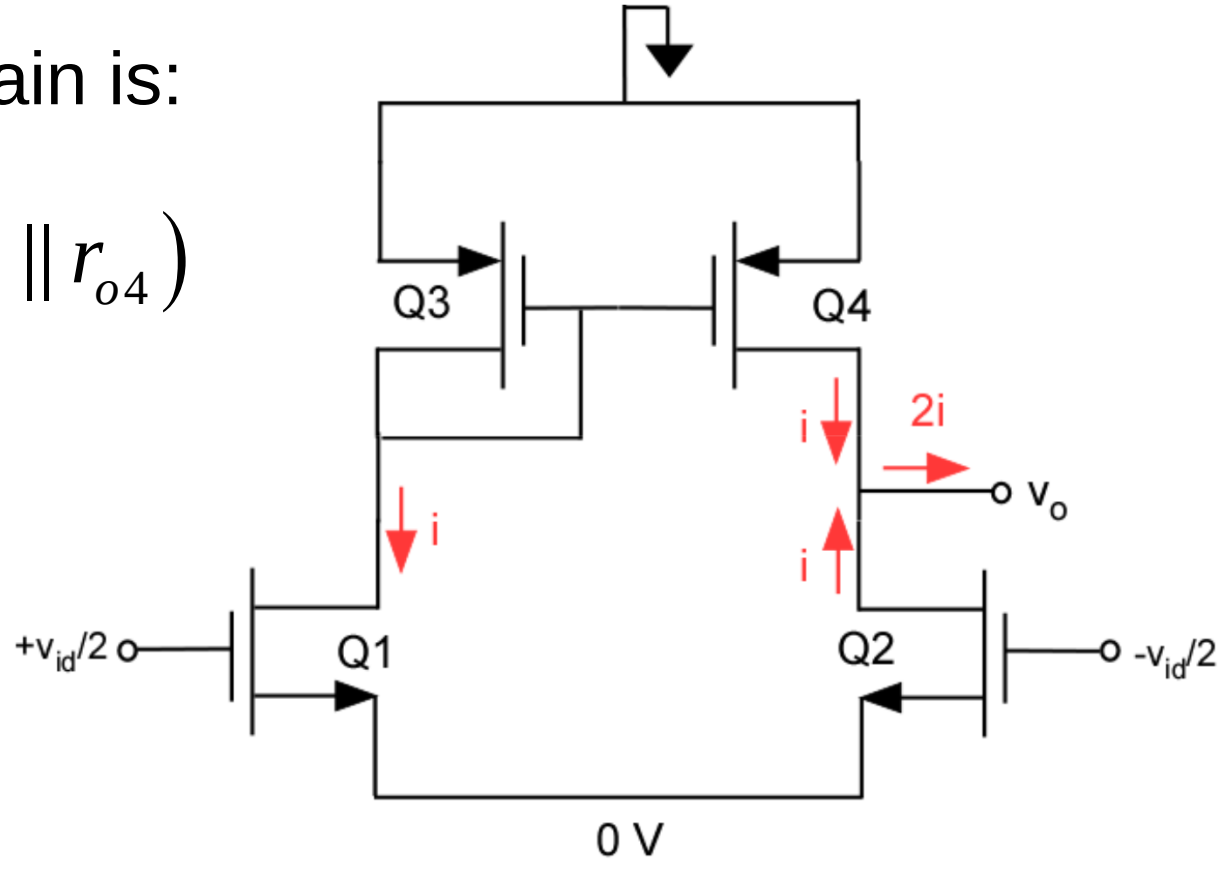
Current mirror action makes it possible to convert the signal to single-ended form without loss of gain.

The differential gain is:

$$A_d \equiv \frac{v_o}{v_{id}} = g_m \left(r_{o2} \parallel r_{o4} \right)$$

$$If \;\; r_{o2} = r_{o4} = r_o$$

$$A_d = \frac{1}{2} g_m r_o$$



MOS Differential Amp with Active Load

The active-loaded MOS differential amplifier has a low common-mode gain ➔ high CMRR

The common-mode gain is:

$$A_{cm} \equiv \frac{v_o}{v_{icm}} = -\frac{1}{2R_{SS}} \frac{r_{o4}}{1+g_{m3}r_{o3}}$$

R_{SS} is internal impedance of current source

$$Usually,\ g_{m3}r_{o3} >> 1\ \ and\ \ r_{o3} = r_{o4}$$

$$A_{cm} = -\frac{1}{2g_{m3}R_{SS}}$$

MOS Differential Amp with Active Load

Since R_{SS} is large, A_{cm} will be small

$$CMRR \equiv \frac{|A_d|}{|A_{cm}|} = \left[g_m \left(r_{o2} \| r_{o4} \right) \right] \left[2 g_{m3} R_{SS} \right]$$

$$If \quad r_{o2} = r_{o4} = r_o \quad and \quad g_{m3} = g_m$$

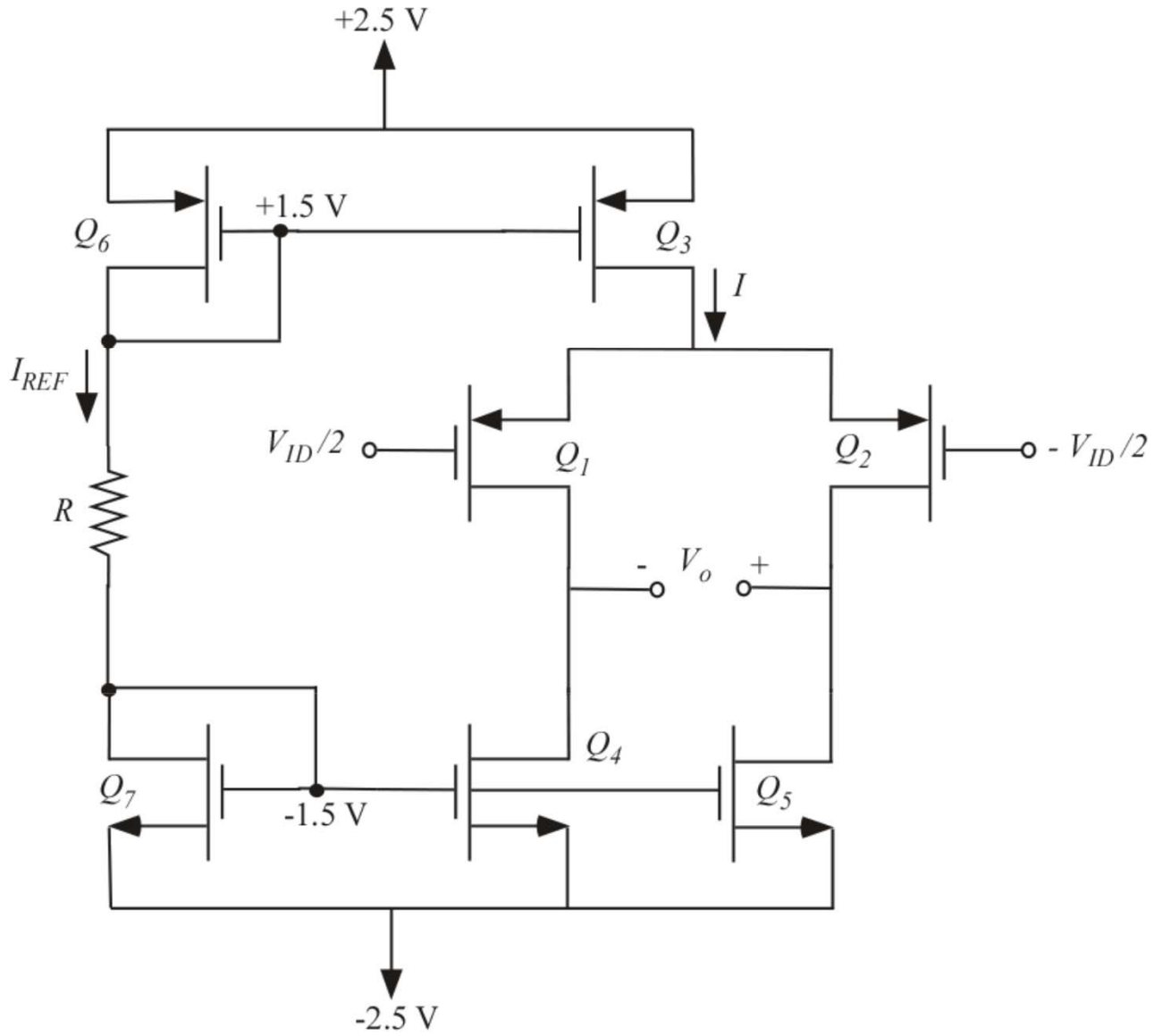
$$CMRR = \left(g_m r_o \right) \left(g_m R_{SS} \right)$$

CMOS OP Amp Example

In the differential amplifier shown, Q_1 and Q_2 form the differential pair while the current source transistors Q_4 and Q_5 form the active loads for Q_1 and Q_2 respectively. The dc bias circuit that establishes an appropriate dc voltage at the drains of Q_1 and Q_2 is not shown. The following specifications are desired: differential gain A_d = 80V/V, I_{REF} = 100 μA, the dc voltage at the gates of Q_6 and Q_3 is +1.5V; the dc voltage at the gates of Q_7, Q_4 and Q_5 is –1.5V.

The technology available is specified as follows: $\mu_n C_{ox} = 3\mu_p C_{ox}$ = 90μA/V^2; $V_{tn} = |V_{tp}| = 0.7$V, $V_{An} = |V_{Ap}|$ = 20V. Specify the required value of R and the W/L ratios for all transistors. Also, specify I_D and V_{GS} at which each transistor is operating. For dc bias calculations, you may neglect channel-length modulation. Fill in the entries in the table provided to show your results.

CMOS OP Amp Example



CMOS OP Amp Example

$$I_{REF} = 100\mu A = \frac{1.5-(-1.5)}{R} \Rightarrow R = \frac{3V}{0.1mA} = 30k\Omega$$

Drain currents are determined by symmetry and inspection V_{GS} values are also determined by inspection for all transistors except Q_1 and Q_2. To determine V_{GS} for Q_1 and Q_2, we do the following: the equivalent load resistance will consist of r_{o1} in parallel with r_{o4} for Q_1 and r_{o2} in parallel with r_{o5} for Q_5. Since the r_o's are equal, this corresponds to $r_o/2$. We have:

$$g_m \frac{r_o}{2} = A_d \Rightarrow g_m = \frac{2A_d}{r_o} = \frac{2\times 80}{400k\Omega} = 0.4mA/V$$

CMOS OP Amp Example

$$g_m = \frac{2I_D}{V_{ov}} \Rightarrow V_{ov} = \frac{2I_D}{g_m} = \frac{2 \times 0.05}{0.4} = 0.25$$

Take polarity into account for PMOS

$$V_{GS1,2} = -0.25 - V_T = -0.95$$

To find W/L ratios, use

$$I_D = \mu C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2 \Rightarrow \frac{W}{L} = \frac{2I_D}{\mu C_{ox}(V_{GS} - V_T)^2}$$

taking into account PMOS and NMOS devices separately

CMOS OP-AMP DESIGN TABLE

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Units
μC_{ox}	30	30	30	90	90	30	90	$\mu A/V^2$
I_D	50	50	100	50	50	100	100	μA
V_{GS}	-.95	-.95	-1	+1	+1	-1	+1	V
W/L	57.3	57.3	74 1.	12.3	12.3	73.1	24.7	