ECE 546
Lecture -17
Latency Insertion Method

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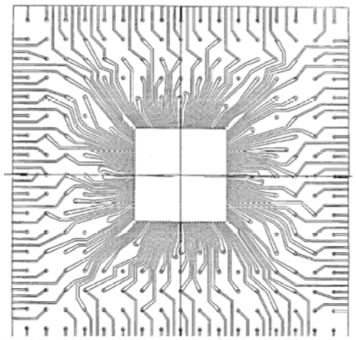
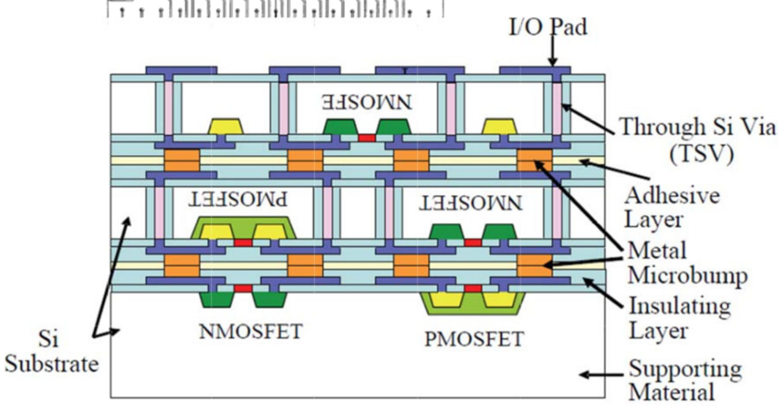
Jose E. Schutt-Aine
Electrical & Computer Engineering
University of Illinois
jesa@illinois.edu

Challenges in Integration

Packaging Complexity



- Up to 16 layers
- Hundreds of vias
- Thousands of TLs
- High density
- Nonuniformity

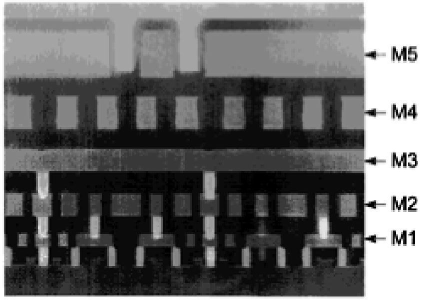


TSV Density: $10/cm^2$ - $10^8/cm^2$

Mitsumasa Koyanagi," High-Density Through Silicon Vias for 3-D LSIs" Proceedings of the IEEE, Vol. 97, No. 1, January 2009

Chip Complexity

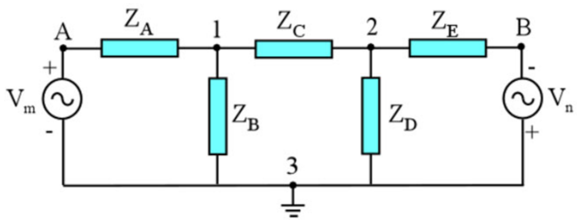
Vertical parallel-plate capacitance	0.05 fF/μm^2
Vertical parallel-plate capacitance (min width)	0.03 fF/μm
Vertical fringing capacitance (each side)	0.01 fF/μm
Horizontal coupling capacitance (each side)	0.03



Source: M. Bohr and Y. El-Mansy - *IEEE TED Vol. 4, March 1998*

Modified Nodal Analysis (MNA)

The Node Voltage method consists in determining potential differences between nodes and ground (reference) using KCL



$$\left(\frac{1}{Z_A}+\frac{1}{Z_B}+\frac{1}{Z_C}\right)V_1-\left(\frac{1}{Z_C}\right)V_2=\left(\frac{1}{Z_A}\right)V_m$$

$$-\left(\frac{1}{Z_C}\right)V_1+\left(\frac{1}{Z_C}+\frac{1}{Z_D}+\frac{1}{Z_E}\right)V_2=-\left(\frac{1}{Z_E}\right)V_n$$

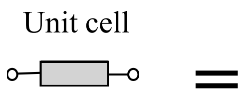
Arrange in matrix form: [G][V]=[I]

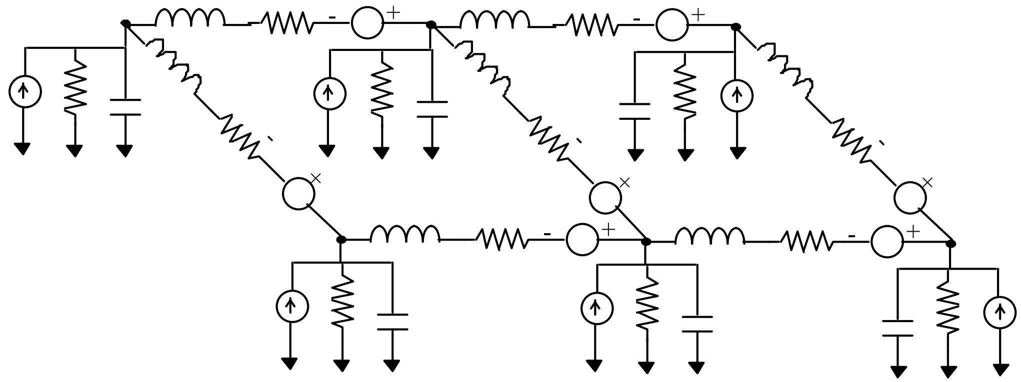
$$\begin{bmatrix} (G_A+G_B+G_C) & -G_C \\ -G_C & (G_C+G_D+G_E) \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}=\begin{bmatrix} G_A V_m \\ -G_E V_m \end{bmatrix}$$

Solve for V_1, V_2 using backward substitution

When matrix G is large process becomes intractable

PDN Modeling



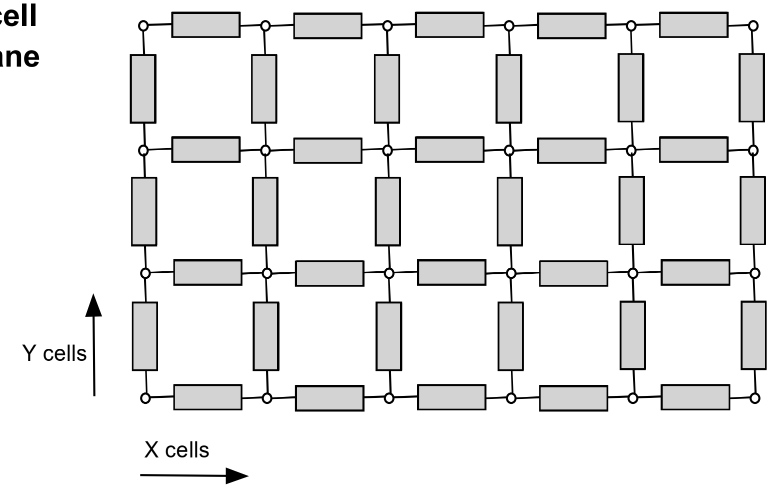


Modeling

- Determine R,L,G,C parameters and define cell
- Synthesize 2-D circuit model for ground plane
- Use SPICE (MNA) to simulate transient

Typical workstation simulation time for a 1200-cell network is 2 h 40 min.

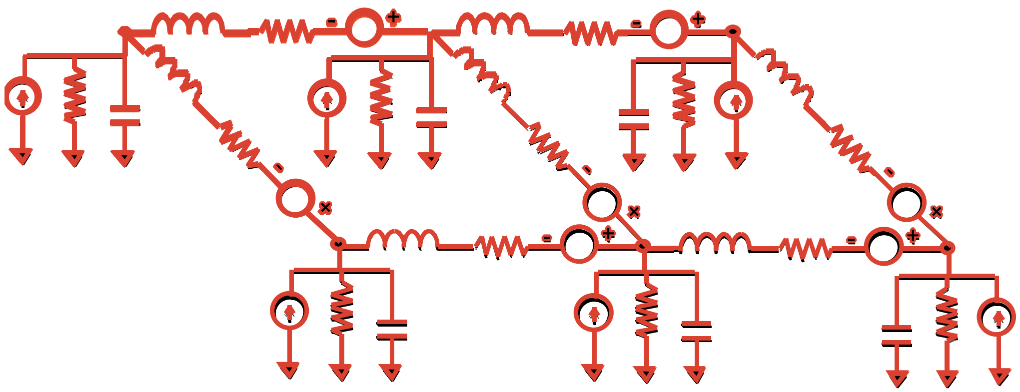
Too time consuming!



Why LIM?

- MNA has <u>super-linear</u> numerical complexity
- LIM has <u>linear</u> numerical complexity
- LIM has no matrix ill-conditioning problems
- Accuracy and stability in LIM are easily controlled
- LIM is much faster than MNA for large circuits

Latency Insertion Method



Latency Insertion Method

Each branch must have an inductor*

Each node must have a shunt capacitor*

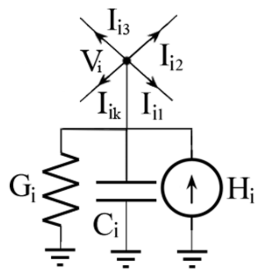
Express branch current in terms of <u>history</u> of adjacent node voltages

Express node voltage in terms of <u>history</u> of adjacent branch currents

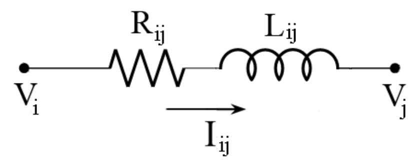
** If branch or node has no inductor or capacitor, insert one with very small value*

LIM Algorithm

- Represents network as a grid of nodes and branches



Node structure



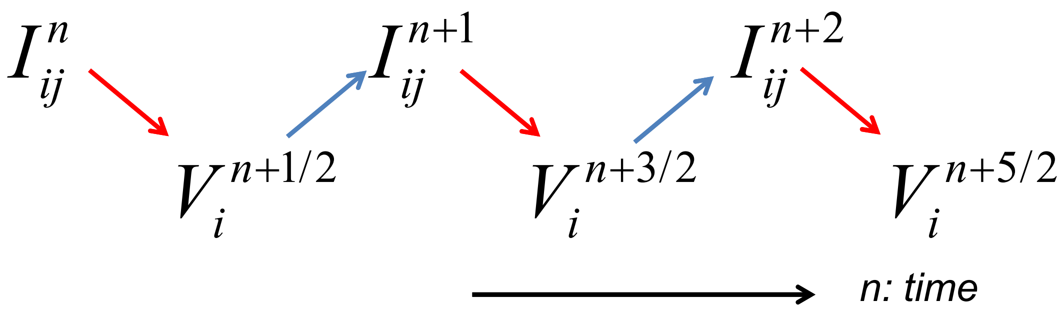
Branch structure

- Discretizes Kirchhoff's current and voltage equations

$$V_i^{n+1/2} = \frac{\dfrac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \displaystyle\sum_{k=1}^{N_a} I_{ik}^n}{\dfrac{C_i}{\Delta t} + G_i} \qquad I_{ij}^{n+1} = I_{ij}^n + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^n\right)$$

- Uses ”leapfrog” scheme to solve for node voltages and branch currents
- Presence of reactive elements is required to generate latency

LIM: Leapfrog Method



$$V_i^{n+1/2} = \frac{\dfrac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \displaystyle\sum_{k=1}^{N_a} I_{ik}^n}{\dfrac{C_i}{\Delta t} + G_i}$$

$$I_{ij}^{n+1} = I_{ij}^{n} + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^{n}\right)$$

Leapfrog method achieves second-order accuracy, i.e., error is proportional to Δt^2

LIM Code

time loop

For time=1, N_t

branch loop

For branch =1, N_b

Update current as per Equation:

$$I_{ij}^{n+1} = I_{ij}^{n} + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^{n} + E_{ij}^{n+1/2}\right)$$

Next branch;

node loop

For node=1, N_n

Update voltage as per Equation

$$V_i^{n+1/2} = \frac{\dfrac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \sum_{k=1}^{M_i} I_{ik}^n - \sum_{q=1}^{N} J_q^n}{\dfrac{C_i}{\Delta t} + G_i}$$

Next node;

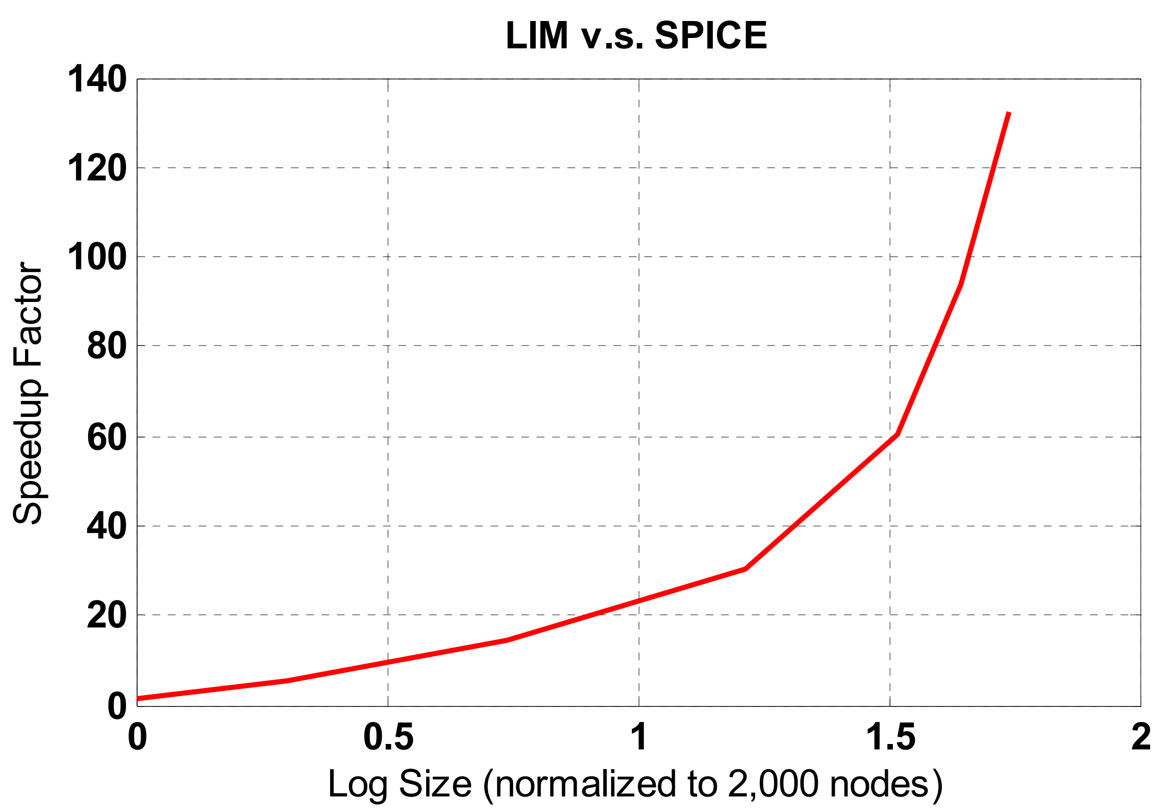
Next time;

Standalone LIM vs SPICE

Simulation Times

No of Nodes	20,000	30,000	40,000	50,000
SPICE (sec)	1224	2935	4741	7358
LIM (sec)	9	13	17	21
Speedup	136	225	278	350

LIM vs SPICE



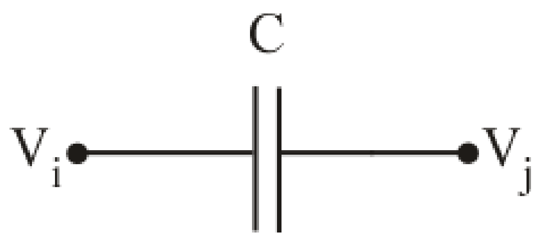
LIM v.s. SPICE
Speedup Factor
0
20
40
60
80
100
120
140
0
0.5
1
1.5
2
Log Size (normalized to 2,000 nodes)

LIM: Problem Elements

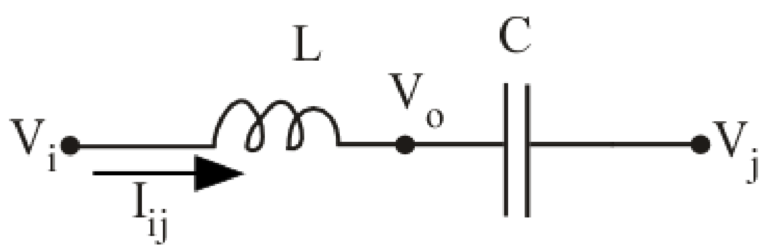
- Mutual inductance → use reluctance (1/L)
- Branch capacitors → special formulation
- Shunt inductors → special formulation
- Dependent sources → account for dependencies
- Frequency dependence → use macromodels

LIM Branch capacitor

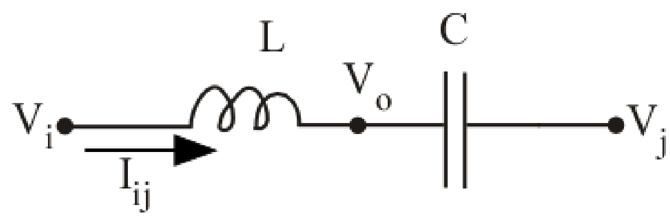
We wish to determine the current update equations for that branch.



In order to handle the branch capacitor with LIM, we introduce a series inductor *L*.



LIM Branch capacitor



In the augmented circuit, we have:

$$I_{ij}^{n} = C\left(\frac{V_c^{n+1/2} - V_c^{n-1/2}}{\Delta t}\right)$$

where V_c is the voltage drop across the capacitor; V_c=V_o-$V_{j.}$ Solving for $V_c^{n+1/2}$

$$V_c^{n+1/2} = V_c^{n-1/2} + \frac{\Delta t}{C} I_{ij}^{n}$$

LIM Branch capacitor

The voltage drop across the inductor is given by:

$$V_L^{n+1/2} = L\left(\frac{I_{ij}^{n+1} - I_{ij}^{n}}{\Delta t}\right)$$

so that

$$V_L^{n+1/2} = V_i^{n+1/2} - V_j^{n+1/2} - V_c^{n+1/2} = L\left(\frac{I_{ij}^{n+1} - I_{ij}^{n}}{\Delta t}\right)$$

which leads to

$$I_{ij}^{n+1} = I_{ij}^{n} + \frac{\Delta t}{L}\left(V_i^{n+1/2} - V_j^{n+1/2} - V_c^{n+1/2}\right)$$

LIM Branch capacitor

After substitution and rearrangement, we get:

$$I_{ij}^{n+1} = I_{ij}^{n}\left(1+\frac{\Delta t^2}{LC}\right)+\frac{\Delta t}{L}\left(V_i^{n+1/2}-V_j^{n+1/2}-V_c^{n-1/2}\right)$$

In order to minimize the effect of L while maintaining stability, we see that

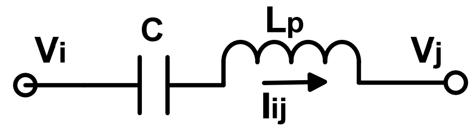
- L must be very small

- L must be $\gg \dfrac{\Delta t^2}{C}$

A large branch capacitor helps as well as small time steps.

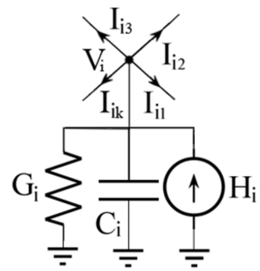
LIM Branch capacitor

Apply the difference equation directly to branch



$$\begin{cases} I_{ij} = C\dfrac{dV_c}{dt} \\ V_L = L_p\dfrac{dI_{ij}}{dt} \end{cases} \Rightarrow \begin{cases} V_c^{n+1/2} = \displaystyle\sum_{k=0}^{n}\left(\frac{I_{ij}^k C}{\Delta t}\right) \equiv T_{ij}^n \\ V_L^{n+1/2} = L_p\dfrac{I_{ij}^{n+1} - I_{ij}^n}{\Delta t} \\ T_{ij}^n = T_{ij}^{n-1} + \dfrac{I_{ij}^n C}{\Delta t} \end{cases} \Rightarrow \left\{ I_{ij}^{n+1} = I_{ij}^n + \frac{\Delta t}{L_p}V_{ij}^{n+1/2} - \frac{\Delta t}{L_p}T_{ij}^n \right.$$

LIM Node Formulations

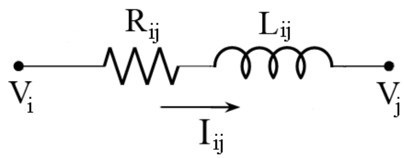


$$C_i\left(\frac{V_i^{n+1/2}-V_i^{n-1/2}}{\Delta t}\right)+G_iV_i^{n-1/2}-H_{ij}^n=-\sum_{k=1}^{M_i}I_{ik}^n$$ **Explicit**

$$C_i\left(\frac{V_i^{n+1/2}-V_i^{n-1/2}}{\Delta t}\right)+G_iV_i^{n+1/2}-H_{ij}^n=-\sum_{k=1}^{M_i}I_{ik}^n$$ **Implicit**

$$C_i\left(\frac{V_i^{n+1/2}-V_i^{n-1/2}}{\Delta t}\right)+\frac{G_i}{2}\left(V_i^{n+1/2}+V_i^{n-1/2}\right)-H_{ij}^n=-\sum_{k=1}^{M_i}I_{ik}^n$$ **Semi-Implicit**

LIM Branch Formulations

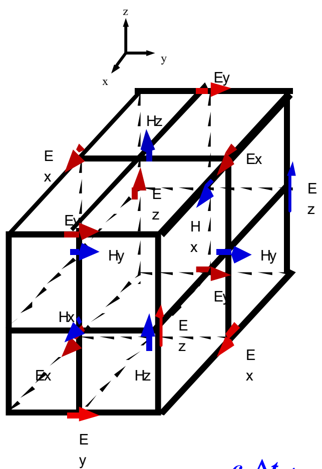


$$V_i^{n+1/2} - V_j^{n+1/2} = L_{ij}\left(\frac{I_{ij}^{n+1} - I_{ij}^{n}}{\Delta t}\right) + R_{ij} I_{ij}^{n} - E_{ij}^{n+1/2}$$ **Explicit**

$$V_i^{n+1/2} - V_j^{n+1/2} = L_{ij}\left(\frac{I_{ij}^{n+1} - I_{ij}^{n}}{\Delta t}\right) + R_{ij} I_{ij}^{n+1} - E_{ij}^{n+1/2}$$ **Implicit**

$$V_i^{n+1/2} - V_j^{n+1/2} = L_{ij}\left(\frac{I_{ij}^{n+1} - I_{ij}^{n}}{\Delta t}\right) + \frac{R_{ij}}{2}\left(I_{ij}^{n+1} + I_{ij}^{n}\right) - E_{ij}^{n+1/2}$$ **Semi-Implicit**

FDTD & LIM

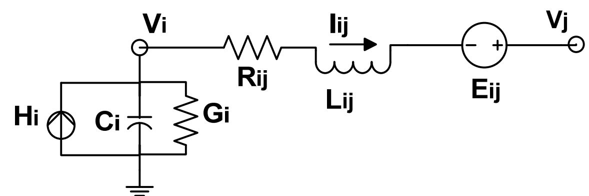


Field Solution

Yee Algorithm

Circuit Solution

Latency Insertion Method (LIM)



$$E_x^n(i,j,k) = E_x^{n-1} + \frac{c}{\varepsilon}\frac{\Delta t}{\Delta y}\left(H_z^{n-1/2}(i,j,k) - H_z^{n-1/2}(i,j-1,k)\right) - \frac{c}{\varepsilon}\frac{\Delta t}{\Delta z}\left(H_y^{n-1/2}(i,j,k) - H_y^{n-1/2}(i,j,k-1)\right)$$

$$V_i^{n+1/2} = \frac{\dfrac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \sum_{k=1}^{M_i} I_{ik}^n}{\dfrac{C_i}{\Delta t} + G_i}$$

$$H_x^{n+1/2}(i,j,k) = H_x^{n-1/2} - \frac{c}{\mu}\frac{\Delta t}{\Delta y}\left(E_z^n(i,j+1,k) - E_z^n(i,j,k)\right) - \frac{c}{\mu}\frac{\Delta t}{\Delta z}\left(H_y^n(i,j,k+1) - E_y^n(i,j,k)\right)$$

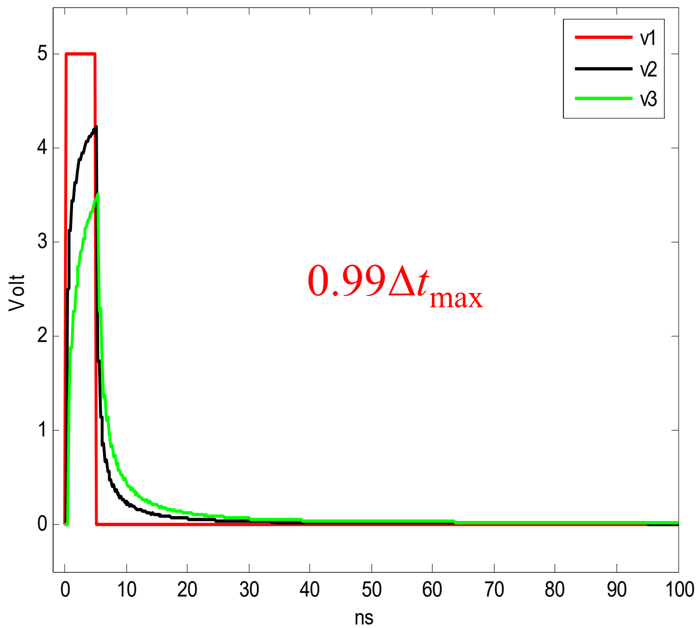
$$I_{ij}^{n+1} = I_{ij}^n + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^n + E_{ij}^{n+1/2}\right)$$

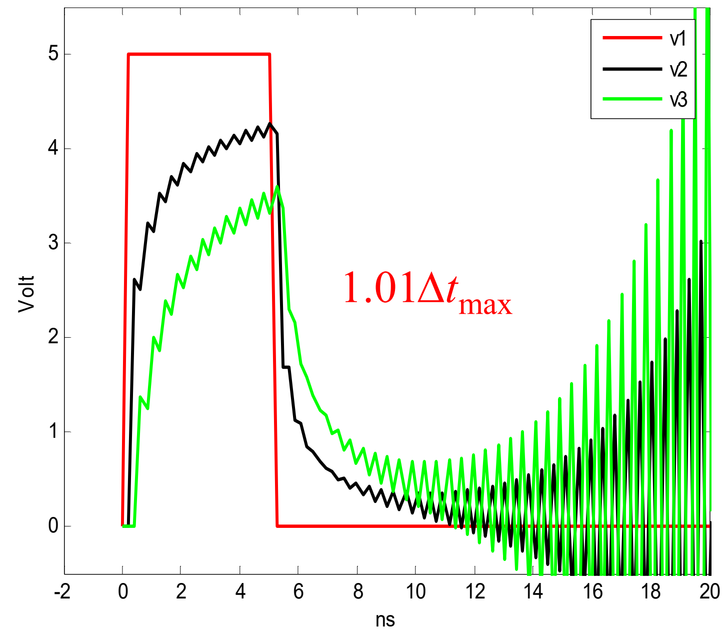
Courant-Friedrichs-Lewy criteria **stability condition**

$$\Delta t < \sqrt{LC}$$

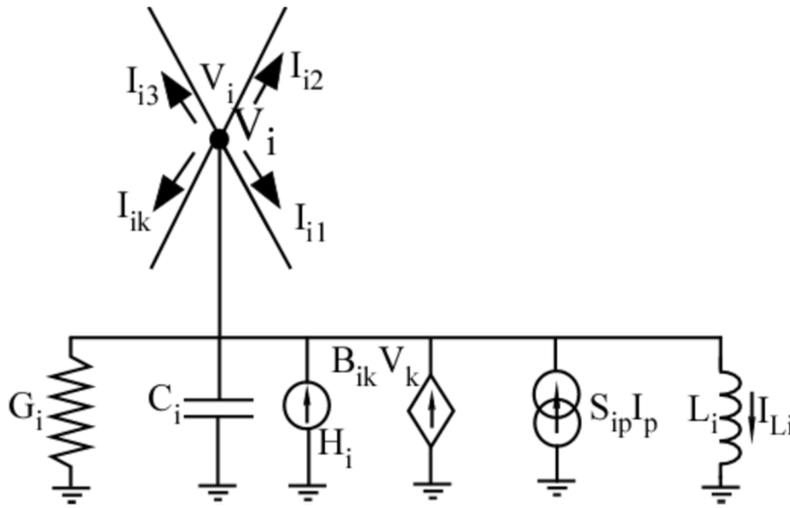
LIM: Stability Analysis

$\Delta t_{max} = 0.20099505$ ns





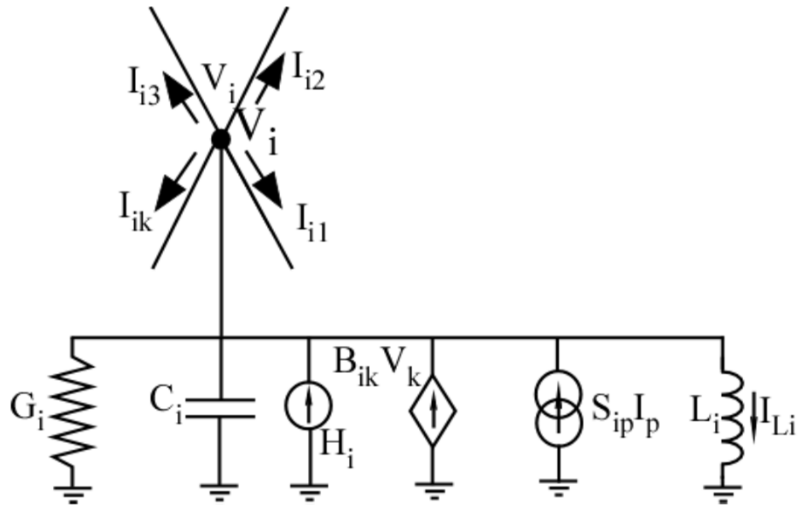
LIM and Dependent Sources



$$C_i\left(\frac{V_i^{n+1/2}-V_i^{n-1/2}}{\Delta t}\right)+\frac{G_i}{2}\left(V_i^{n+1/2}+V_i^{n-1/2}\right)-H_i^n+I_{Li}^n$$

$$-\frac{B_{ik}}{2}\left(V_k^{n+1/2}+V_k^{n-1/2}\right)-S_{ip}I_p^n=-\sum_{j=1}^{M_i}I_{ij}^n$$

LIM and Dependent Sources



$$\mathbf{C}\left(\frac{\mathbf{v}^{n+1/2} - \mathbf{v}^{n-1/2}}{\Delta t}\right) + \frac{1}{2}\mathbf{G}\left(\mathbf{v}^{n+1/2} + \mathbf{v}^{n-1/2}\right) - \mathbf{h}^{n} + \mathbf{i}_{L}^{n}$$

$$-\frac{1}{2}\mathbf{B}\left(\mathbf{v}^{n+1/2} + \mathbf{v}^{n-1/2}\right) - \mathbf{S}\mathbf{i}^{n} = -\mathbf{M}\mathbf{i}^{n}$$

LIM and Dependent Sources

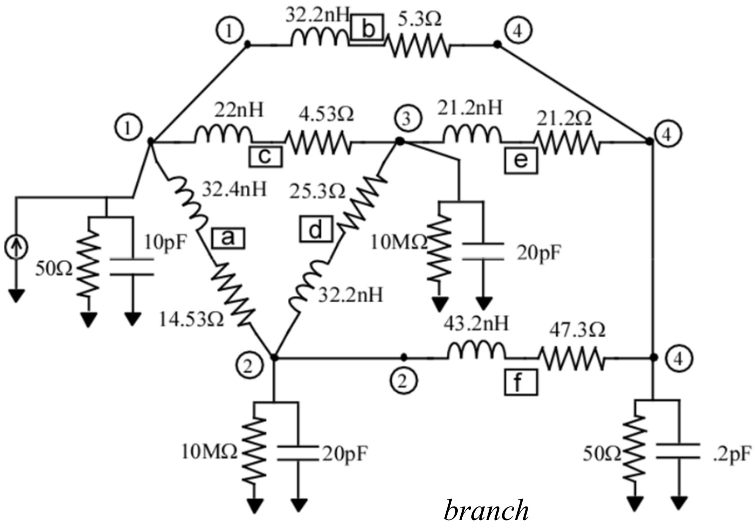
where $\boldsymbol{M}$ is the incidence matrix. $\boldsymbol{M}$ is defined as follows

$$M_{qp} = 1 \; if \; branch \;\; p \; is \; incident \; at \; node \; q \; and \; the$$
$$current \;\; flows \; away \;\; from \; node \; q.$$

$$M_{qp} = -1 \; if \; branch \;\; p \; is \; incident \; at \; node \; q \; and \; the$$
$$current \;\; flows \; into \; node \; q.$$

$$M_{qp} = 0 \; if \; branch \;\; p \; is \; not \; incident \; at \; node \; q.$$

Incidence Matrix



$$
\mathbf{M} = \begin{matrix} & \overbrace{\begin{matrix} a & b & c & d & e & f \end{matrix}}^{branch} \\ \begin{matrix} node\,1 \\ node\,2 \\ node\,3 \\ node\,4 \end{matrix} & \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & -1 & -1 & 1 & 0 \\ 0 & -1 & 0 & 0 & -1 & -1 \end{bmatrix} \end{matrix}
$$

LIM and Dependent Sources

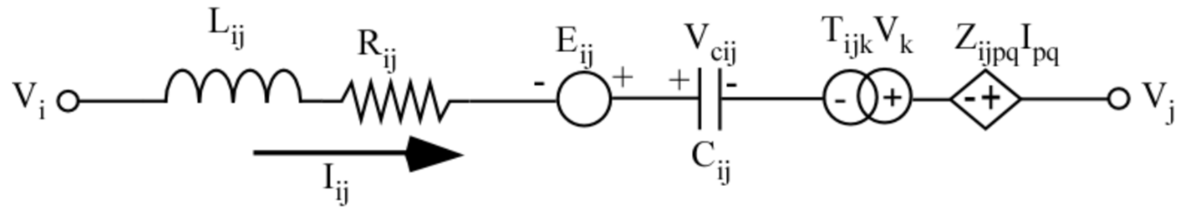
$$\mathbf{i}_L^{n+1} = \mathbf{i}_L^{n} + \Delta t \mathbf{L}_n^{-1} \mathbf{v}^{n+1/2}$$

$$\mathbf{C}\left(\frac{\mathbf{v}^{n+1/2} - \mathbf{v}^{n-1/2}}{\Delta t}\right) + \frac{1}{2}\mathbf{G}'\left(\mathbf{v}^{n+1/2} + \mathbf{v}^{n-1/2}\right) - \mathbf{h}^n + \mathbf{i}_L^n = -\mathbf{M}'\mathbf{i}^n$$

$$\mathbf{G}' = \mathbf{G} + \mathbf{B} \qquad \mathbf{M}' = \mathbf{M} + \mathbf{S}$$

$$\mathbf{v}^{n+1/2} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}'}{2}\right)^{-1}\left[\left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G}'}{2}\right)\mathbf{v}^{n-1/2} + \mathbf{h}^n - \mathbf{i}_L^n - \mathbf{M}'\mathbf{i}^n\right]$$

LIM and Dependent Sources



$$V_i^{n+1/2} - V_j^{n+1/2} = L_{ij}\left(\frac{I_{ij}^{n+1} - I_{ij}^{n}}{\Delta t}\right) + \frac{R_{ij}}{2}\left(I_{ij}^{n+1} + I_{ij}^{n}\right) - E_{ij}^{n+1/2} + V_{cij}^{n+1/2}$$

$$- T_{ijk}V_k^{n+1/2} - \frac{Z_{ijpq}}{2}\left(I_{pq}^{n+1} + I_{pq}^{n}\right)$$

$$\mathbf{M}^{\mathbf{T}}\mathbf{v}^{\mathbf{n+1/2}} = \frac{\mathbf{L}}{\Delta t}\left(\mathbf{i}^{\mathbf{n+1}} - \mathbf{i}^{\mathbf{n}}\right) + \frac{\mathbf{R}}{2}\left(\mathbf{i}^{\mathbf{n+1}} + \mathbf{i}^{\mathbf{n}}\right) - \mathbf{e}^{\mathbf{n+1/2}} + \mathbf{v}_{\mathbf{c}}^{\mathbf{n+1/2}}$$

$$- \mathbf{T}\mathbf{v}^{\mathbf{n+1/2}} - \frac{\mathbf{Z}}{2}\left(\mathbf{i}^{\mathbf{n+1}} + \mathbf{i}^{\mathbf{n}}\right)$$

LIM and Dependent Sources

$$\mathbf{v}_{\mathbf{c}}^{\mathbf{n+1/2}} = \mathbf{v}_{\mathbf{c}}^{\mathbf{n-1/2}} + \Delta t \mathbf{C}_{\mathbf{b}}^{\mathbf{-1}} \mathbf{i}^{\mathbf{n}}$$

$$\mathbf{i}_{\mathbf{L}}^{\mathbf{n+1}} = \mathbf{i}_{\mathbf{L}}^{\mathbf{n}} + \Delta t \mathbf{L}_{\mathbf{n}}^{\mathbf{-1}} \mathbf{v}^{\mathbf{n+1/2}}$$

$$\mathbf{i}^{\mathbf{n+1}} = \left(\frac{\mathbf{L}}{\Delta t} + \frac{\mathbf{R}'}{2} \right)^{-1} \left[\left(\frac{\mathbf{L}}{\Delta t} - \frac{\mathbf{R}'}{2} \right) \mathbf{i}^{\mathbf{n}} + \mathbf{e}^{\mathbf{n+1/2}} - \mathbf{v}_{\mathbf{c}}^{\mathbf{n+1/2}} + \mathbf{M}^{\mathbf{T}'} \mathbf{v}^{\mathbf{n+1/2}} \right]$$

$$\mathbf{v}^{\mathbf{n+1/2}} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}'}{2} \right)^{-1} \left[\left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G}'}{2} \right) \mathbf{v}^{\mathbf{n-1/2}} + \mathbf{h}^{\mathbf{n}} - \mathbf{i}_{\mathbf{L}}^{\mathbf{n}} - \mathbf{M}' \mathbf{i}^{\mathbf{n}} \right]$$

LIM and Dependent Sources

$$\mathbf{i}^{n+1} = \left(\frac{\mathbf{L}}{\Delta t} + \frac{\mathbf{R'}}{2}\right)^{-1} \left(\frac{\mathbf{L}}{\Delta t} - \frac{\mathbf{R'}}{2}\right)\mathbf{i}^{n} + \left(\frac{\mathbf{L}}{\Delta t} + \frac{\mathbf{R'}}{2}\right)^{-1} \mathbf{M}^{T'}\mathbf{v}^{n+1/2}$$

$$-\left(\frac{\mathbf{L}}{\Delta t} + \frac{\mathbf{R'}}{2}\right)^{-1} \mathbf{v}_{c}^{n+1/2}$$

$$\mathbf{v}^{n+1/2} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G'}}{2}\right)^{-1} \left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G'}}{2}\right)\mathbf{v}^{n-1/2} - \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G'}}{2}\right)^{-1} \mathbf{M'}\mathbf{i}^{n}$$

$$-\left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G'}}{2}\right)^{-1} \mathbf{i}_{L}^{n}$$

Stability Analysis

DEFINE:

$$\mathbf{P}_+ = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G'}}{2}\right)^{-1} \qquad \mathbf{P}_- = \left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G'}}{2}\right)$$

$$\mathbf{Q}_+ = \left(\frac{\mathbf{L}}{\Delta t} + \frac{\mathbf{R'}}{2}\right)^{-1} \qquad \mathbf{Q}_- = \left(\frac{\mathbf{L}}{\Delta t} - \frac{\mathbf{R'}}{2}\right)$$

so that

$$\mathbf{i}^{n+1} = \mathbf{Q}_+\mathbf{Q}_-\mathbf{i}^{n} + \mathbf{Q}_+\mathbf{M}^{T'}\mathbf{v}^{n+1/2} \qquad \mathbf{v}^{n+1/2} = \mathbf{P}_+\mathbf{P}_-\mathbf{v}^{n-1/2} - \mathbf{P}_+\mathbf{M'}\mathbf{i}^{n}$$

$$\mathbf{i}^{n+1} = \mathbf{Q}_+\mathbf{Q}_-\mathbf{i}^{n} + \mathbf{Q}_+\mathbf{M}^{T'}\mathbf{P}_+\mathbf{P}_-\mathbf{v}^{n-1/2} - \mathbf{Q}_+\mathbf{M}^{T'}\mathbf{P}_+\mathbf{M'}\mathbf{i}^{n}$$

Stability Analysis

$$\mathbf{v}^{n+1/2} = \mathbf{P}_+\mathbf{P}_-\mathbf{v}^{n-1/2} - \mathbf{P}_+\mathbf{M}'\mathbf{i}^n$$

$$\mathbf{i}^{n+1} = \mathbf{Q}_+\mathbf{M}^{T'}\mathbf{P}_+\mathbf{P}_-\mathbf{v}^{n-1/2} + \left[\mathbf{Q}_+\mathbf{Q}_- - \mathbf{Q}_+\mathbf{M}^{T'}\mathbf{P}_+\mathbf{M}'\right]\mathbf{i}^n$$

The 2 matrix equations can be combined in a single matrix equation that reads

$$\begin{bmatrix}\mathbf{v}^{n+1/2}\\ \mathbf{i}^{n+1}\end{bmatrix} = \begin{bmatrix}\mathbf{P}_+\mathbf{P}_- & -\mathbf{P}_+\mathbf{M}'\\ \mathbf{Q}_+\mathbf{M}^{T'}\mathbf{P}_+\mathbf{P}_- & \mathbf{Q}_+\mathbf{Q}_- - \mathbf{Q}_+\mathbf{M}^{T'}\mathbf{P}_+\mathbf{M}'\end{bmatrix}\begin{bmatrix}\mathbf{v}^{n-1/2}\\ \mathbf{i}^{n}\end{bmatrix}$$

or

$$\begin{bmatrix}\mathbf{v}^{n+1/2}\\ \mathbf{i}^{n+1}\end{bmatrix} = \mathbf{A}\begin{bmatrix}\mathbf{v}^{n-1/2}\\ \mathbf{i}^{n}\end{bmatrix}$$

Amplification Matrix

$$\mathbf{A} = \begin{bmatrix} \mathbf{P_+P_-} & \mathbf{-P_+M'} \\ \mathbf{Q_+M^{T'}P_+P_-} & \mathbf{Q_+Q_- - Q_+M^{T'}P_+M'} \end{bmatrix}$$

$$\mathbf{A_{11} = P_+P_-}$$

$$\mathbf{A_{12} = -P_+M'}$$

$$\mathbf{A_{21} = Q_+M^{T'}P_+P_-}$$

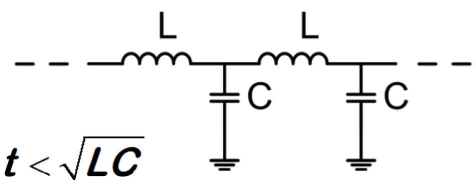
$$\mathbf{A_{22} = Q_+Q_- - Q_+M^{T'}P_+M'}$$

A is the ***amplification matrix***. **All the eigenvalues of A must be less than 1 in order to guarantee stability**. Therefore to insure stability, we must choose Δt such that all the eigenvalues of **A** are less than 1

Stability Methods for LIM

- LIM is conditionally stable → upper bound on the time step Δt.

- For uniform 1-D LC circuits [2]:



$$\Delta t < \sqrt{LC}$$

- For RLC/GLC circuits [3]:

$$\Delta t \le \sqrt{2}\,\min_{i=1}^{N_n}\left(\sqrt{\frac{C_i}{N_b^i}\min_{p=1}^{N_b^i}(L_{i,p})}\right)$$

- For general circuits [4]:

$$A = \begin{bmatrix} \mathbf{P_+P_-} & -\mathbf{P_+M} \\ \mathbf{Q_+M^TP_+P_-} & \mathbf{Q_+Q_-} - \mathbf{Q_+M^TP_+M} \end{bmatrix}$$

Amplification matrix.

[2] Z. Deng and J. E. Schutt-Ainé, *IEEE EPEPS*, Oct. 2004.
[3] S. N. Lalgudi and M. Swaminathan, *IEEE TCS II*, vol. 55, no. 9, Sep. 2008.
[4] J. E. Schutt-Ainé, *IEEE EDAPS*, Dec. 2008.

VinC – Voltage in Current*

$$V_i^{n+1} = \frac{\dfrac{C_i V_i^{n-1}}{\Delta t} + H_i^{n+1/2} - \sum_{k=1}^{N_a} I_{ik}^{n+1/2}}{\dfrac{C_i}{\Delta t} + G_i} = \Gamma_i V_i^n + Z_{ni} H_i^{n+1/2} - Z_{ni} \sum_{k=1}^{N_a} I_{ik}^{n+1/2}$$

$$I_{ij}^{n+1/2} = I_{ij}^{n-1/2} + \frac{\Delta t}{L_{ij}} \left(V_i^{n+1} - V_j^{n+1} - R_{ij} I_{ij}^{n-1/2} \right)$$

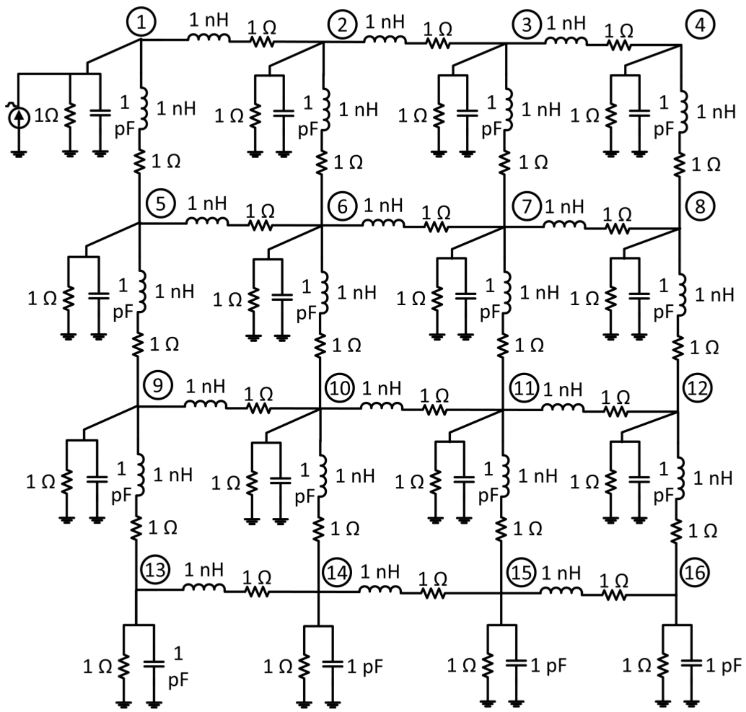
Algebraic sum of all currents incident at node *i* except that of branch ***ij***

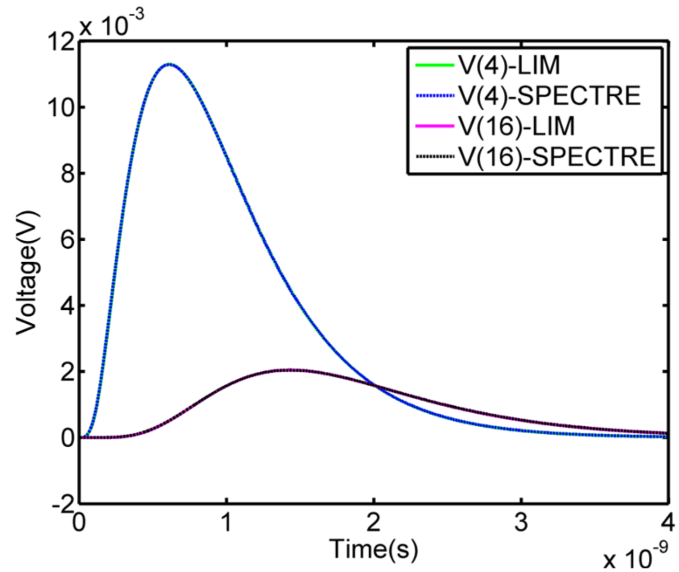
$$I_{ij}^{n+1/2} = \frac{I_{ij}^{n-1/2} + \dfrac{\Delta t}{L_{ij}} \left(\Gamma_i V_i^n + Z_{ni} H_i^{n+1/2} - Z_{ni} \sum_{k=1, k\neq j}^{N_a} I_{ik}^{n+1/2} - \Gamma_j V_j^n - Z_{nj} H_j^{n+1/2} + Z_{nj} \sum_{k=1, k\neq j}^{N_a} I_{jk}^{n+1/2} - R_{ij} I_{ij}^{n-1/2} \right)}{\left[1 + Z_{ni} \dfrac{\Delta t}{L_{ij}} + Z_{nj} \dfrac{\Delta t}{L_{ij}} \right]}$$

VinC formulation achieves higher accuracy and stability

* K.H. Tan, P. Goh and M.F. Ain, "Voltage-in-current formulation for the latency insertion method for improved stability", *Electronics Letters*, vol. 52, no. 23, Nov. 2016, pp. 1904-1906.

Example – RLGC Grid





* Current excitation with amplitude of 6A, rise and fall times of 10 ps and pulse width of 100 ps.

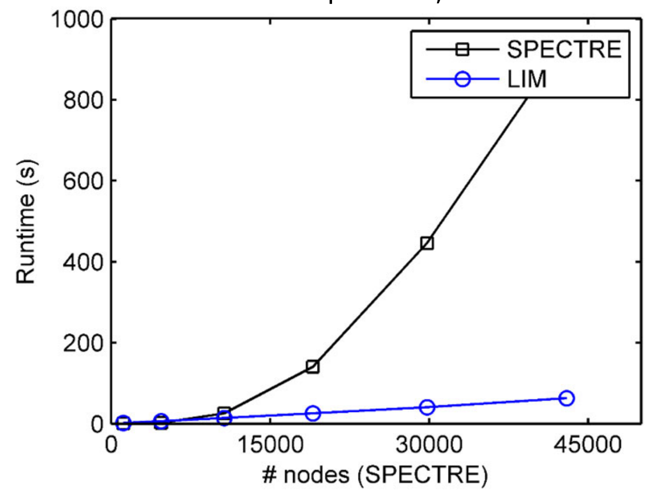
* SPECTRE – A SPICE-like simulator from Cadence Design Systems Inc.

Example – RLGC Grid

- Comparison of runtime for LIM and SPECTRE*.

Circuit Size	# nodes (SPECTRE)	SPECTRE (s)	LIM (s)
20 × 20	1160	0.15	1.53
40 × 40	4720	2.14	6.25
60 × 60	10680	25.73	14.23
80 × 80	19040	140.59	25.71
100 × 100	29800	445.77	40.64
120 × 120	42960	945.00	62.89

* Intel 3.16 GHz processor, 32 GB RAM.



- LIM exhibits linear numerical complexity!
  - Outperforms conventional SPICE-like simulators.
- Expand on LIM as a multi-purpose circuit simulator.

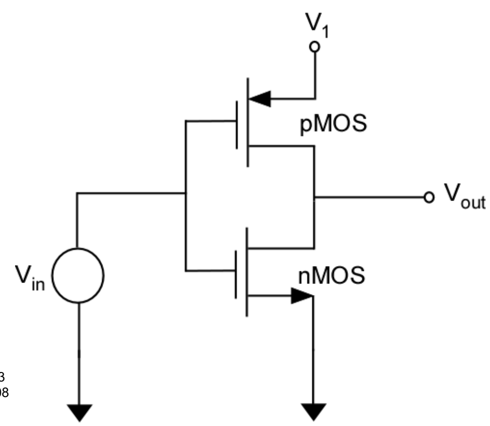
Transistor Models

- Level 1
- BSIM4
- BSIM-CMG
- VBIC

Predictive Technology Model

NMOS

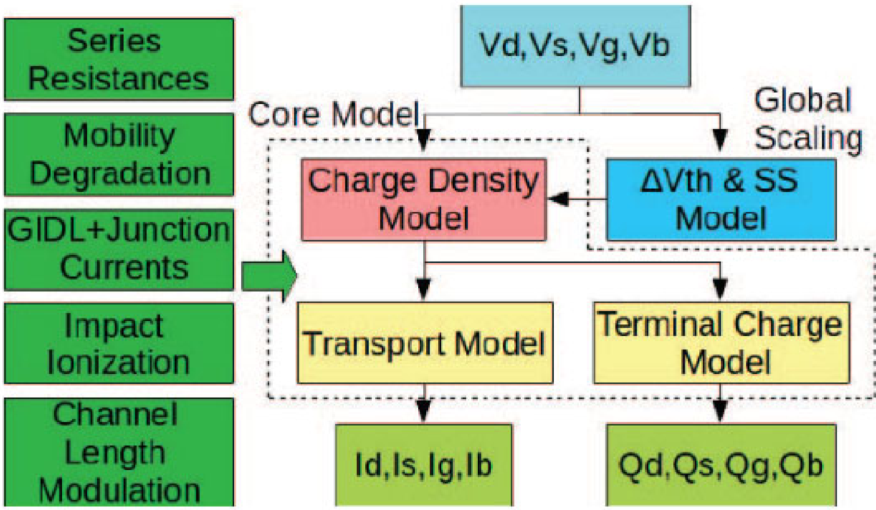
```
* Predictive Technology Model Beta Version
* 130nm NMOS SPICE Parametersv (normal one)
*

.model NMOS NMOS
+Level = 49

+Lint = 2.5e-08 Tox = 3.3e-09
+Vth0 = 0.332 Rdsw = 200

+lmin=1.3e-7 lmax=1.3e-7 wmin=1.3e-7 wmax=1.0e-4 Tref=27.0 version =3.1
+Xj= 4.5000000E-08      Nch= 5.6000000E+17
+lln= 1.0000000         lwn= 0.00          wln= 0.00
+wwn= 1.0000000         ll= 0.00
+lw= 0.00               lwl= 0.00          wint= 0.00
+wl= 0.00               ww= 0.00           wwl= 0.00
+Mobmod= 1              binunit= 2         xl= 0
+xw= 0                  binflag= 0
+Dwg= 0.00              Dwb= 0.00

+K1= 0.3661500          K2= 0.00
+K3= 0.00               Dvt0= 8.7500000    Dvt1= 0.7000000
+Dvt2= 5.0000000E-02    Dvt0w= 0.00        Dvt1w= 0.00
+Dvt2w= 0.00            Nlx= 3.5500000E-07 W0= 0.00
+K3b= 0.00              Ngate= 5.0000000E+20

+Vsat= 1.3500000E+05    Ua= -1.8000000E-09    Ub= 2.2000000E-18
+Uc= -2.9999999E-11     Prwb= 0.00
+Prwg= 0.00             Wr= 1.0000000         U0= 1.3400000E-02
+A0= 2.1199999          Keta= 4.0000000E-02   A1= 0.00
+A2= 0.9900000          Ags= -0.1000000       B0= 0.00
+B1= 0.00

+Voff= -7.9800000E-02   NFactor= 1.1000000    Cit= 0.00
+Cdsc= 0.00             Cdscb= 0.00           Cdscd= 0.00
+Eta0= 4.0000000E-02    Etab= 0.00            Dsub= 0.5200000

+Pclm= 0.1000000        Pdiblc1= 1.2000000E-02   Pdiblc2= 7.5000000E-03
+Pdiblcb= -1.3500000E-02   Drout= 0.2800000      Pscbe1= 8.6600000E+08
+Pscbe2= 1.0000000E-20  Pvag= -0.2800000         Delta= 1.0100000E-02
+Alpha0= 0.00           Beta0= 30.0000000

+kt1= -0.3400000        kt2= -5.2700000E-02   At= 0.00
+Ute= -1.2300000        Ua1= -8.6300000E-10   Ub1= 2.0000001E-18
+Uc1= 0.00              Kt1l= 4.0000000E-09   Prt= 0.00

+Cj= 0.0015             Mj= 0.7175511         Pb= 1.24859
+Cjsw= 2E-10            Mjsw= 0.3706993       Php= 0.7731149
+Cta= 9.290391E-04      Ctp= 7.456211E-04     Pta= 1.527748E-03
+Ptp= 1.56325E-03       JS=2.50E-08           JSW=4.00E-13
+N=1.0                  Xti=3.0               Cgdo=2.75E-10
+Cgso=2.75E-10          Cgbo=0.0E+00          Capmod= 2
+NQSMOD= 0              Elm= 5                Xpart= 1
+Cgsl= 1.1155E-10       Cgdl= 1.1155E-10      Ckappa= 0.8912
+Cf= 1.113e-10          Clc= 5.475E-08        Cle= 6.46
+Dlc= 2E-08             Dwc= 0                Vfbcv= -1
```



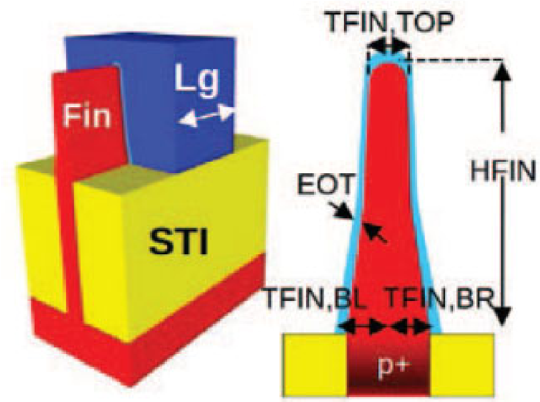
PMOS

```
* Predictive Technology Model Beta Version
* 130nm PMOS SPICE Parametersv (normal one)
*

.model PMOS PMOS
+Level = 49

+Lint = 2.e-08 Tox = 3.3e-09
+Vth0 = -0.3499 Rdsw = 400

+lmin=1.3e-7 lmax=1.3e-7 wmin=1.3e-7 wmax=1.0e-4 Tref=27.0 version =3.1
+Xj= 4.5000000E-08      Nch= 6.8500000E+18
+lln= 0.00              lwn= 0.00          wln= 0.00
+wwn= 0.00              ll= 0.00
+lw= 0.00               lwl= 0.00          wint= 0.00
+wl= 0.00               ww= 0.00           wwl= 0.00
+Mobmod= 1              binunit= 2         xl= 0
+xw= 0                  binflag= 0
+Dwg= 0.00              Dwb= 0.00

+K1= 0.4087000          K2= 0.00
+K3= 0.00               Dvt0= 5.0000000    Dvt1= 0.2600000
+Dvt2= -1.0000000E-02   Dvt0w= 0.00        Dvt1w= 0.00
+Dvt2w= 0.00            Nlx= 1.6500000E-07 W0= 0.00
+K3b= 0.00              Ngate= 5.0000000E+20

+Vsat= 1.0500000E+05    Ua= -1.4000000E-09    Ub= 1.9499999E-18
+Uc= -2.9999999E-11     Prwb= 0.00
+Prwg= 0.00             Wr= 1.0000000         U0= 5.2000000E-03
+A0= 2.1199999          Keta= 3.0300001E-02   A1= 0.00
+A2= 0.4000000          Ags= 0.1000000        B0= 0.00
+B1= 0.00

+Voff= -9.10000000E-02  NFactor= 0.1250000    Cit= 2.7999999E-03
+Cdsc= 0.00             Cdscb= 0.00           Cdscd= 0.00
+Eta0= 80.0000000       Etab= 0.00            Dsub= 1.8500000

+Pclm= 2.5000000        Pdiblc1= 4.8000000E-02   Pdiblc2= 5.0000000E-05
+Pdiblcb= 0.1432509     Drout= 9.0000000E-02     Pscbe1= 1.0000000E-20
+Pscbe2= 1.0000000E-20  Pvag= -6.0000000E-02     Delta= 1.0100000E-02
+Alpha0= 0.00           Beta0= 30.0000000

+kt1= -0.3400000        kt2= -5.2700000E-02   At= 0.00
+Ute= -1.2300000        Ua1= -8.6300000E-10   Ub1= 2.0000001E-18
+Uc1= 0.00              Kt1l= 4.0000000E-09   Prt= 0.00

+Cj= 0.0015             Mj= 0.7175511         Pb= 1.24859
+Cjsw= 2E-10            Mjsw= 0.3706993       Php= 0.7731149
+Cta= 9.290391E-04      Ctp= 7.456211E-04     Pta= 1.527748E-03
+Ptp= 1.56325E-03       JS=2.50E-08           JSW=4.00E-13
+N=1.0                  Xti=3.0               Cgdo=2.75E-10
+Cgso=2.75E-10          Cgbo=0.0E+00          Capmod= 2
+NQSMOD= 0              Elm= 5                Xpart= 1
+Cgsl= 1.1155E-10       Cgdl= 1.1155E-10      Ckappa= 0.8912
+Cf= 1.113e-10          Clc= 5.475E-08        Cle= 6.46
+Dlc= 2E-08             Dwc= 0                Vfbcv= -1
```

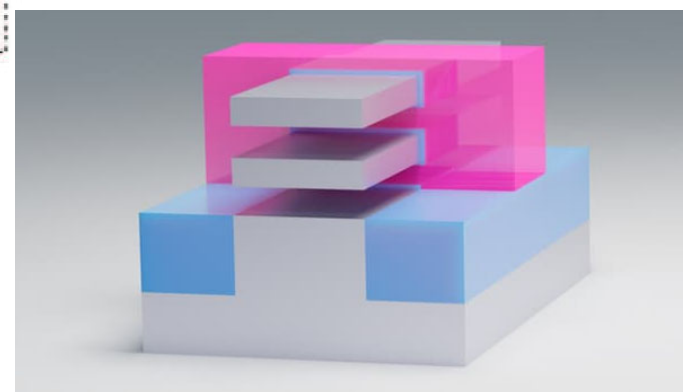
BSIM-CMG Model



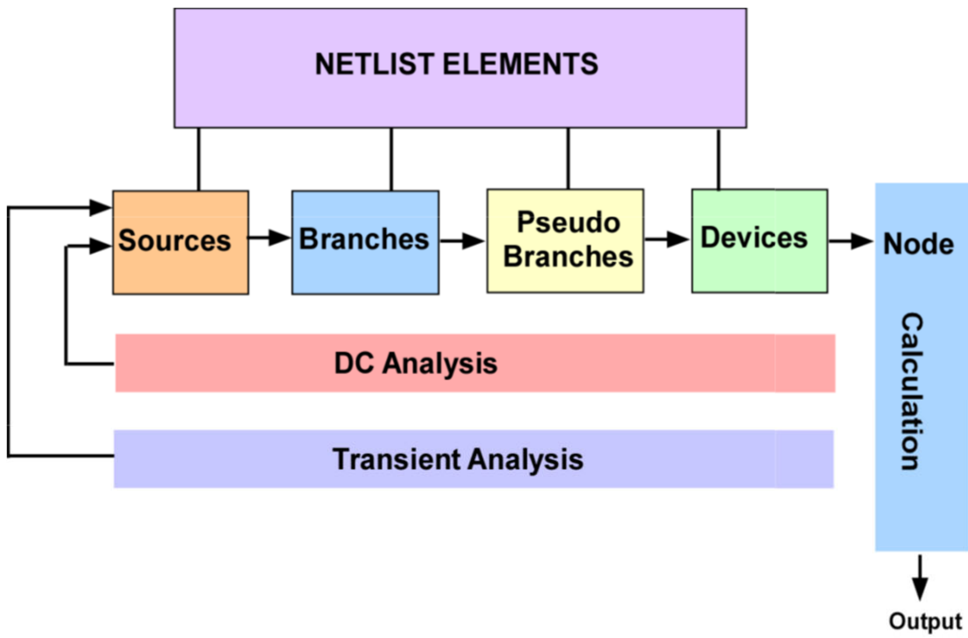
FinFET Transistor



Nanosheet Transistor



Simulator Flow



LIM Simulator Development

ELEMENTARY DEVICES
Resistors
Capacitors
Inductors
Mutual Inductors

INDEPENDENT SOURCES
Pulse
Sinusoidal
Exponential
Piece-Wise Linear
Pseudo-random Bit Sequence

DEPENDENT SOURCES
Voltage-Controlled Current Sources
Voltage-Controlled Voltage Sources
Current-Controlled Current Sources
Current-Controlled Voltage Sources

TRANSMISSION LINES
Lossless Single Transmission Lines
Lossy Single Transmission Lines
Lossless Multiconductor Transmission Lines
Lossy Multiconductor Transmission Lines

MACROMODELS
Model-Order Reduction
Convolution Model

DEVICES
Junction Diodes
Bipolar Junction Transistors (BJTs)
Junction Field-Effect Transistors (JFETs)
MOSFETs
MESFETs

Done
In Development

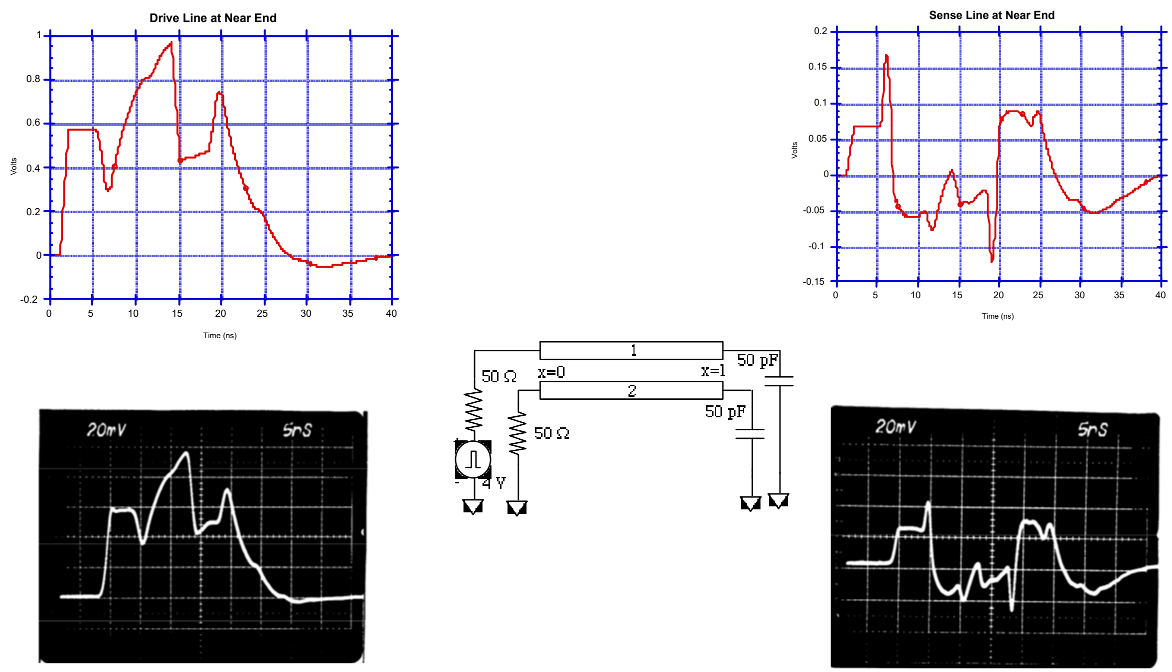
Analyses

TYPES OF ANALYSIS

DC Analysis
AC Small-Signal Analysis
Transient Analysis
Pole-Zero Analysis
Small-Signal Distortion Analysis
Sensitivity Analysis
Noise Analysis

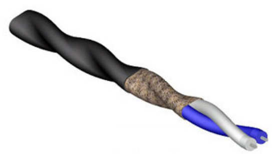
Done
In Development

LIM Simulations



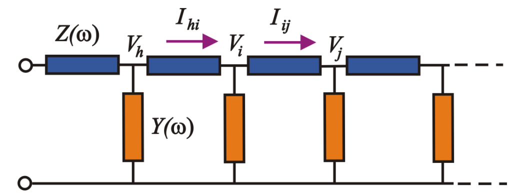
Computer simulations of distributed model (top) and experimental waveforms of coupled microstrip lines (bottom) for the transmission-line circuit shown at the near end (x=0) for line 1 (left) and line 2 (right). The pulse characteristics are magnitude = 4 V; width = 12 ns; rise and fall times = 1 ns. The photograph probe attenuation factors are 40 (left) and 10 (right).

LIM Simulation Examples

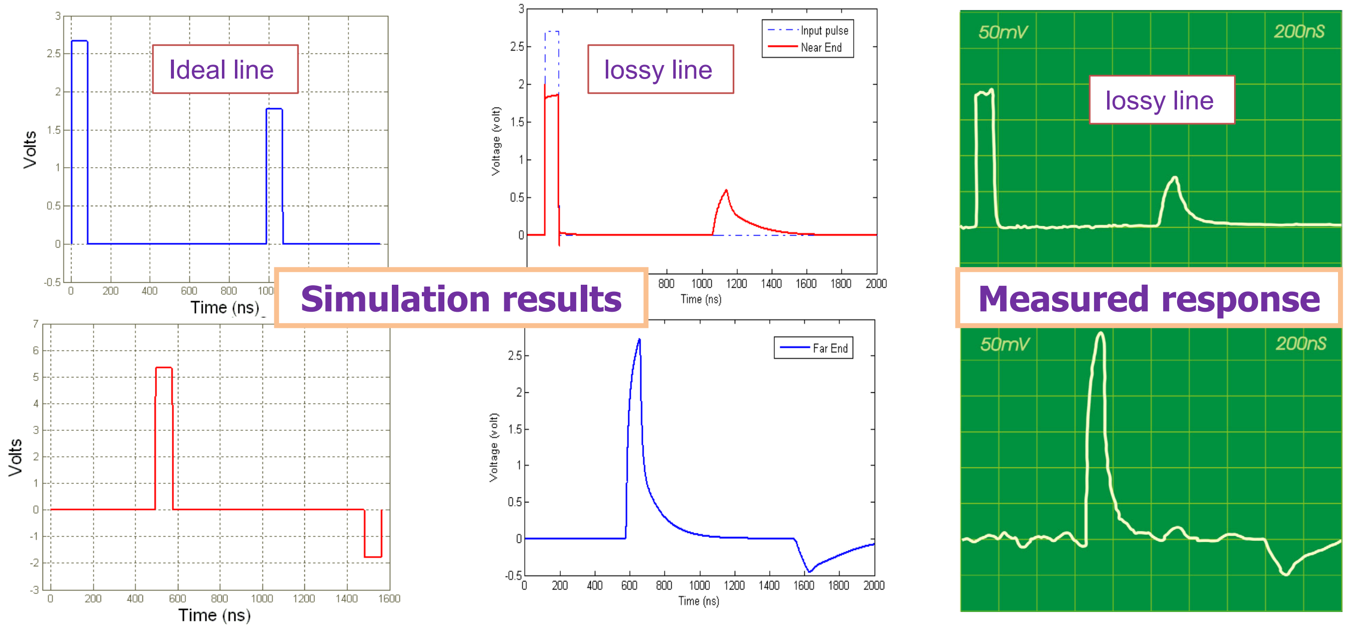


Twisted-pair cable

Simulation setup

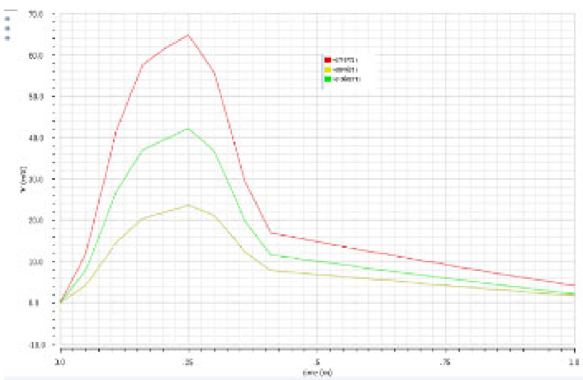


Generalized model [3]

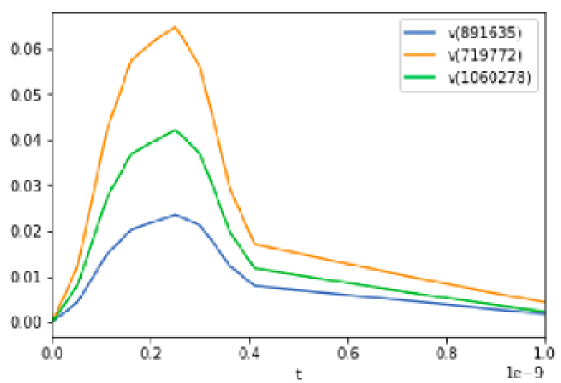


Large Circuit Results

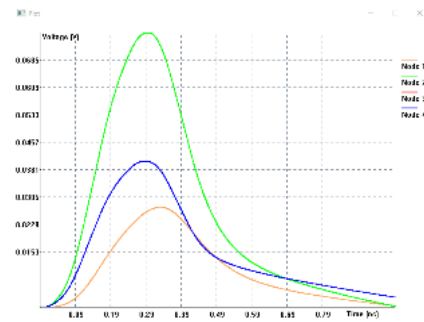
SPECTRE



NGSPICE



LIM



- 2,029,744 series resistors
- 380,742 shunt resistors
- 380,742 series capacitors
- 380,742 shunt capacitors
- 381 series inductors
- 835,858 series voltage sources
- 381 shunt voltage sources
- 761,484 shunt current sources

SPECTRE: 1 day 20 hours 44 minutes

NGSPICE: 3 days 2 hours 57 minutes

LIM: 2 hours 37 minutes 39 seconds

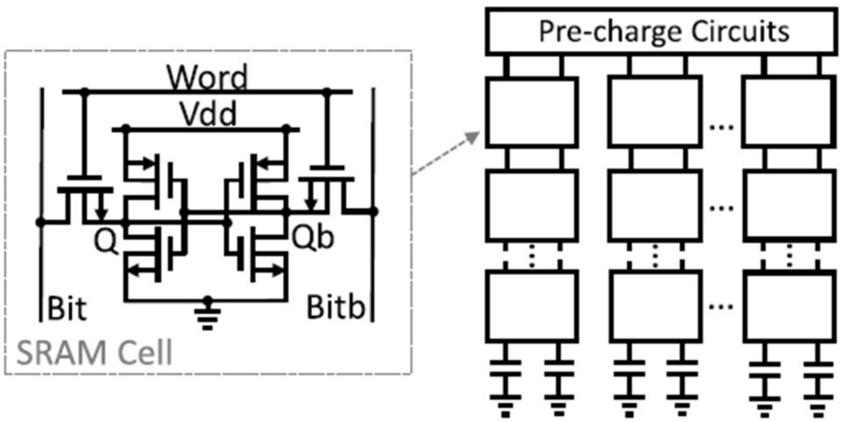
Large Circuit Results*

TABLE 3. Time spent per iteration for SmartSpice and VinC LIM in full TFT FPD circuits.

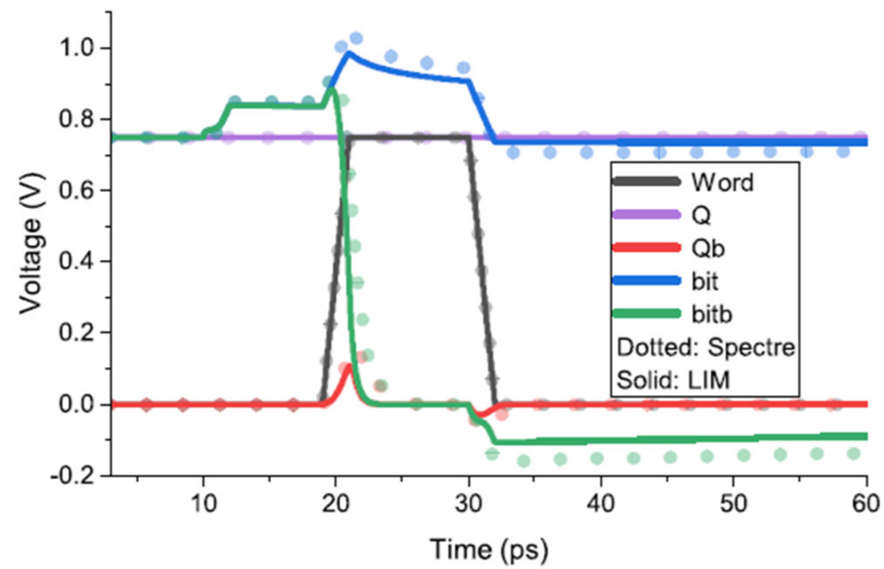
Circuit size (in pixels)	No. of nodes	No. of TFTs	Time per iteration (s)		Speedup ratio
			Smart-Spice	VinC LIM	
20×12	5,867	5,040	0.032	0.015	$2.13\times$
25×20	12,159	10,500	0.080	0.030	$2.67\times$
80×36	69,479	60,480	0.803	0.182	$4.41\times$
100×100	240,851	210,000	6.362	0.677	$9.40\times$
320×180	1,383,915	1,209,600	256.51	4.118	$62.29\times$
640×360	5,532,627	4,838,400	4393.41	18.83	$233.32\times$
960×540	12,446,147	10,886,400	dnc.	43.78	-
1920×1080	49,775,555	43,545,600	dnc.	193.30	-

*Wei Chun Chin, Andrei Pashkovich, José E. Schutt-Ainé, Nur Syazreen Ahmad, Patrick Goh,, "Thin-Film Transistor Simulations With the Voltage-In-Current Latency Insertion Method", *IEEE Access, Volume 9, 2021.*

Large Circuit - SRAM*



The schematic of the SRAM arrays example.



Simulation results of the SRAM array example.

*Yi Zhou, Bobi Shi, Qingyi Wang, Thong Nguyen, Patrick Goh, José E. Schutt-Ainé, "Latency Insertion Method for Fast FinFET Simulation Based on the BSIM-CMG Model", IEEE Transactions on Circuits and Systems I: Regular Papers, 2025, Early Access Article.

Large Circuit Results*

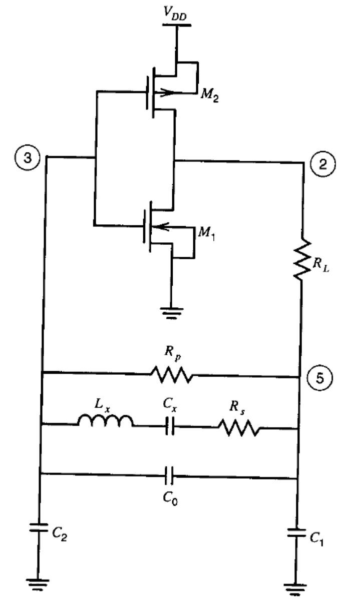
SIMULATION RESULTS OF LARGE-SCALE SRAM ARRAY EXAMPLES

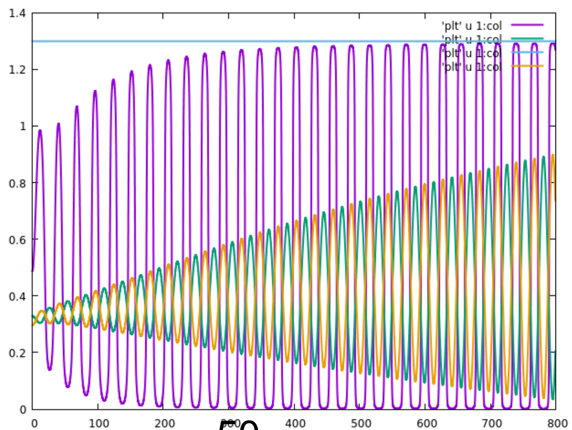
	RMSE	Spectre time	LIM time	Speedup
20×20 (3,200T)	0.049	2.5s	2.0s	× 1.3
100×100 (80,000T)	0.050	13m 10s	1m 32.3s	× 8.6
200×200 (320,000T)	0.051	6h 48m 51s	6m 6.8s	× 66.9
300×300 (720,000T)	0.049	1d 23h 25m	14m 11.0s	× 200.6
400×400 (1,280,000T)	0.050	6d 23h 43m	24m 52.6s	× 404.5

*Yi Zhou, Bobi Shi, Qingyi Wang, Thong Nguyen, Patrick Goh, José E. Schutt-Ainé, "Latency Insertion Method for Fast FinFET Simulation Based on the BSIM-CMG Model", IEEE Transactions on Circuits and Systems I: Regular Papers, 2025, Early Access Article.

Pierce Oscillator – BSIM4

```
*PIERCE XTAL OSCILLATOR WITH CMOS
M1 2 3 0 0 NMOS W=40U L=10U
M2 2 3 1 1 PMOS W=80U L=10U
RL 2 5 10000
C1 5 0 22.0e-12
C2 3 0 22.0e -12
RP 3 5 22.0e+06
LEFF 3 5 0.18e -03
VDD 1 0 5
.MODEL NMOS NMOS LEVEL=1 VTO=1 KP=20U
LAMBDA=0.02
.MODEL PMOS PMOS LEVEL=1 VTO= -1 KP=10U
LAMBDA=0.02
.tran 0.001e-09   6793.0e-09e-08
.LIM C=0.015e-12 L=0.1e-09 G=1.0e-20
.PRINT TRAN V(2) V(3) V(1) V(5)
.PLOT TRAN V(2) V(3) V(1) V(5)
.END
```





50

Commercial Simulators - Comparison

	NGSPICE	HSPICE	ADS	SPECTRE	AFS	NEXXIM	LIM
Frequency Dependence	NO	YES	YES	NO	NO	YES	YES
Uses MNA	YES	YES	YES	YES	YES	YES	NO
BSIM-CMG	NO	YES	NO	YES	YES	NO	YES

References

1. Jose Schutt-Ainé, Patrick Goh, "LIM Algorithms for Diodes and Branch Capacitors", 2018 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), Chandigarh, India, December 2018.
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