ECE 546
Lecture - 19
Noise and Signaling

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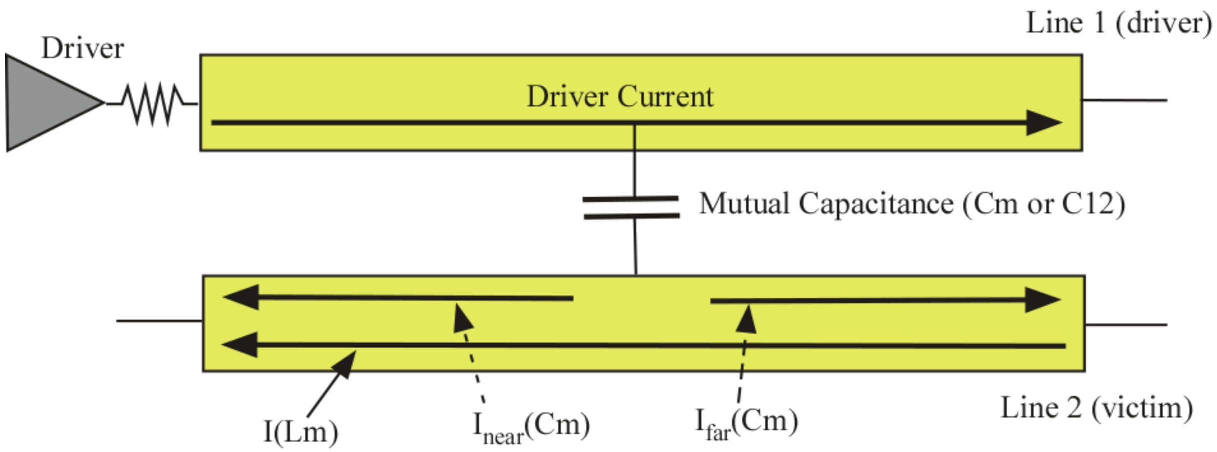
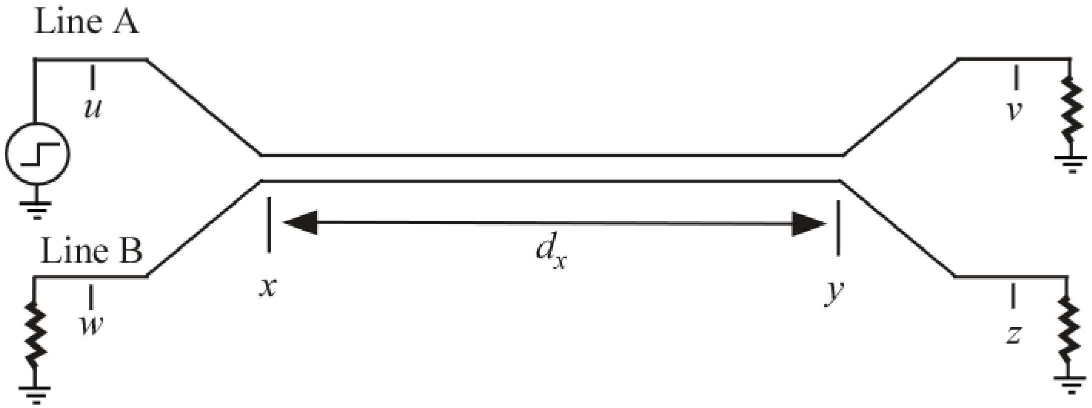
Near- and Far-End Crosstalks

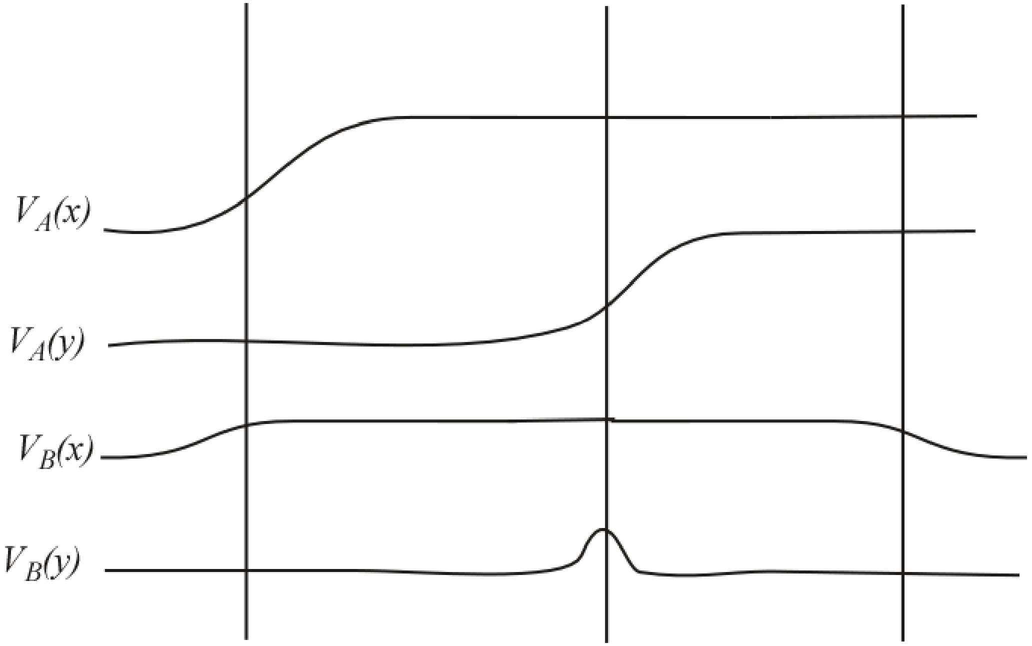


- Crosstalk current due to mutual capacitance will split into 2 parts and flow toward both ends of victim line

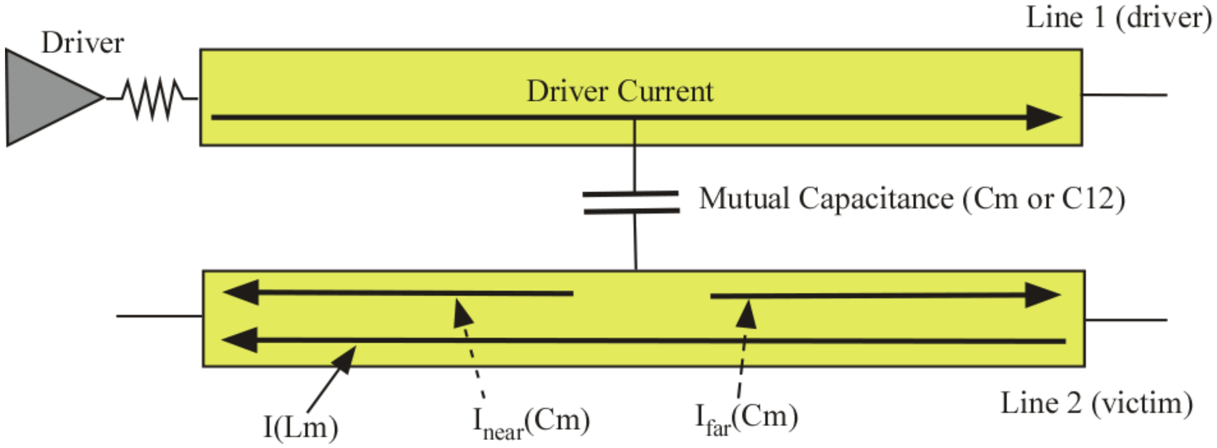
- Crosstalk current due to mutual inductance will flow from the far end toward the near end of victim line

Transmission-Line - Crosstalk





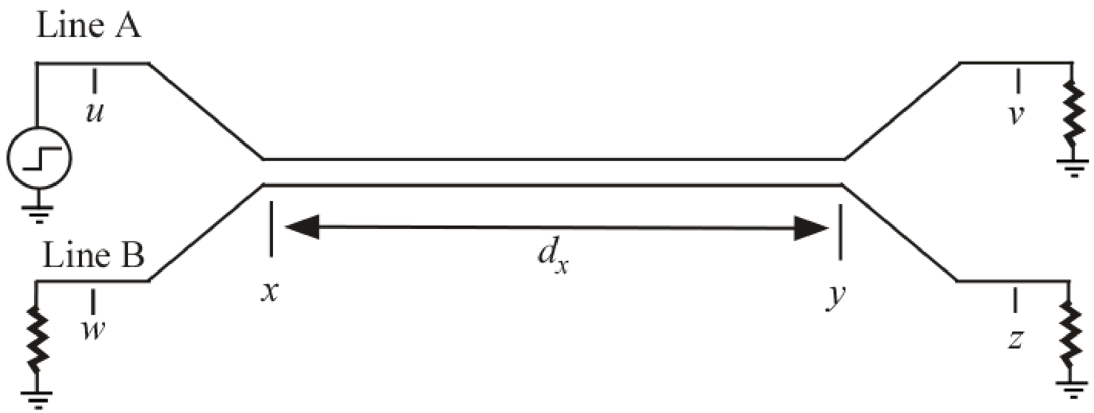
Near End Crosstalk



- Crosstalk seen on the victim line at the end closest to the driver
- Assumes that load is terminated with characteristic impedance of single isolated line
- Sum of contributions to reverse traveling wave that arrives at point x during period equal to time of flight

$$I_{near} = I(L_m) + I_{near}(C_m)$$

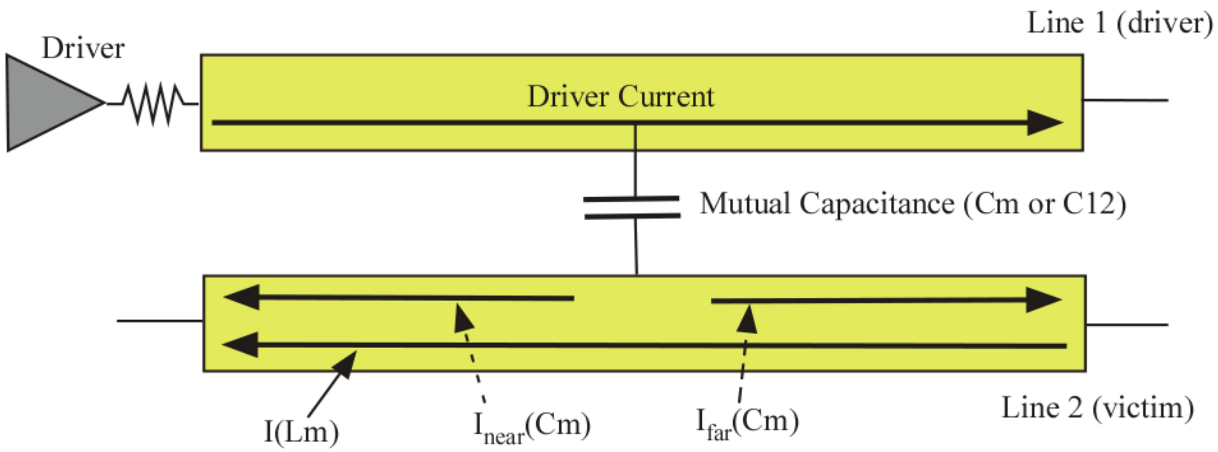
Near End Crosstalk



- Approximate quantity
- Assumes that load is terminated with characteristic impedance of single isolated line
- Sum of contributions to reverse traveling wave that arrives at point x during period equal to time of flight

$$k_{rx} = \frac{\left(k_{cx} + k_{lx}\right)}{4}$$

Far End Crosstalk

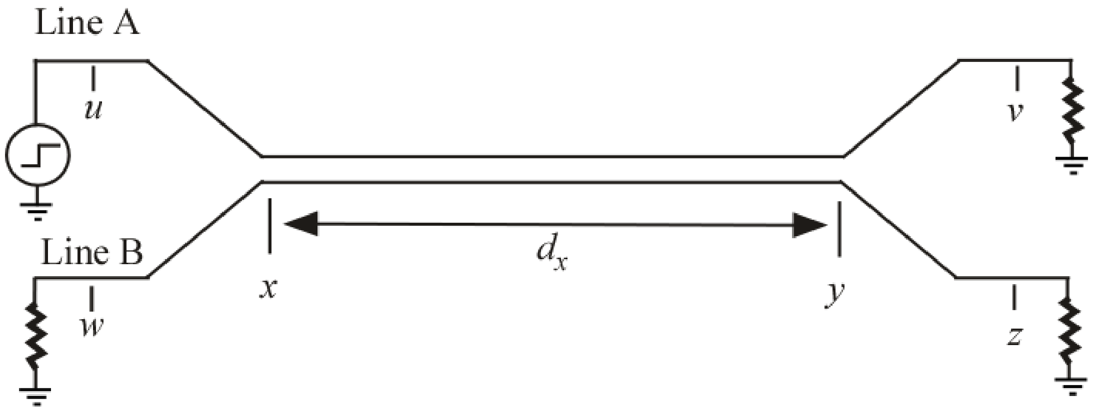


- **Crosstalk seen on the victim line at the end farthest away from the driver**

- **Assumes that load is terminated with characteristic impedance of single isolated line**

$$I_{far} = I_{far}(C_m) - I(L_m)$$

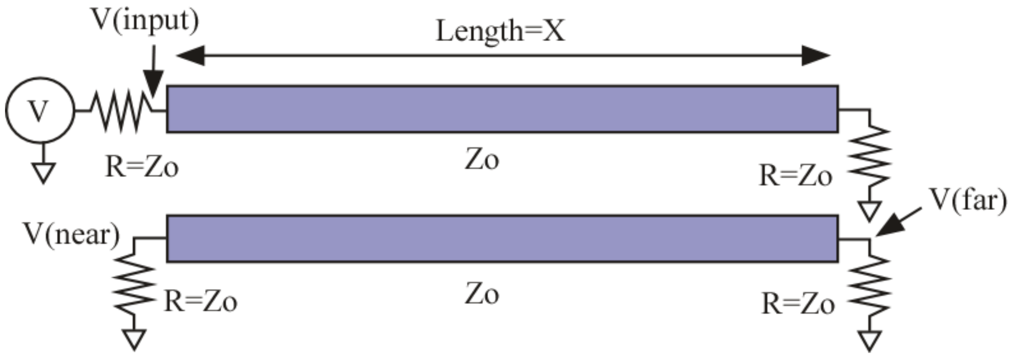
Far End Crosstalk

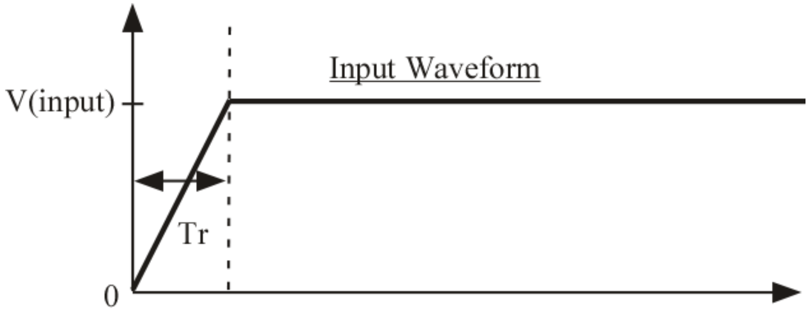


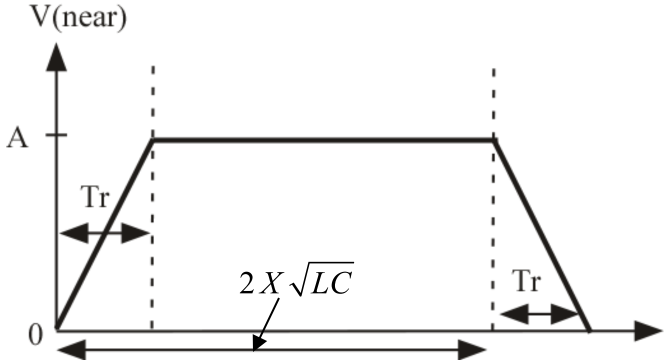
- **Approximate quantity**
- **Assumes that load is terminated with characteristic impedance of single isolated line**
- **Time derivative of signal on line A scaled by forward-coupling coefficient and coupling time**

$$k_{fx} = \frac{k_{cx} - k_{lx}}{4}$$

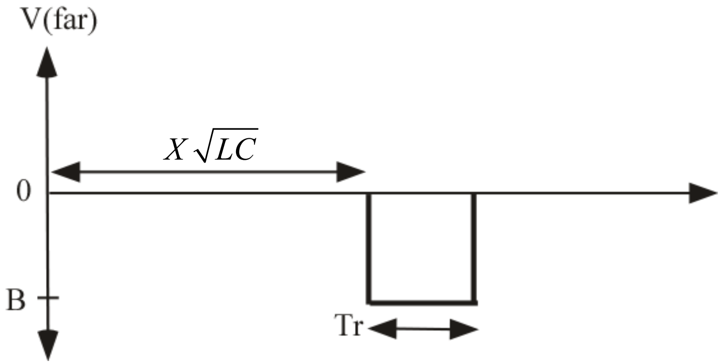
Digital Crosstalk - Case 1





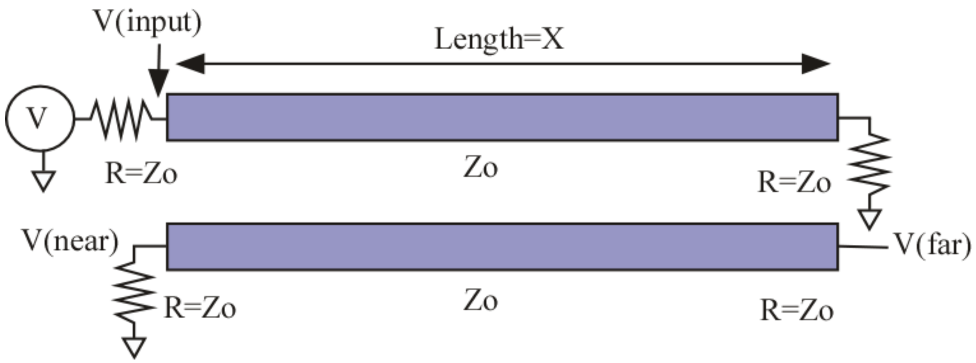


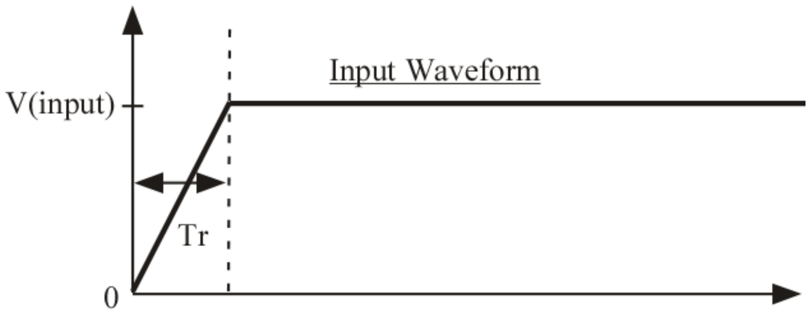
$$A = \frac{V(input)}{4}\left(\frac{L_M}{L} + \frac{C_M}{C}\right)$$

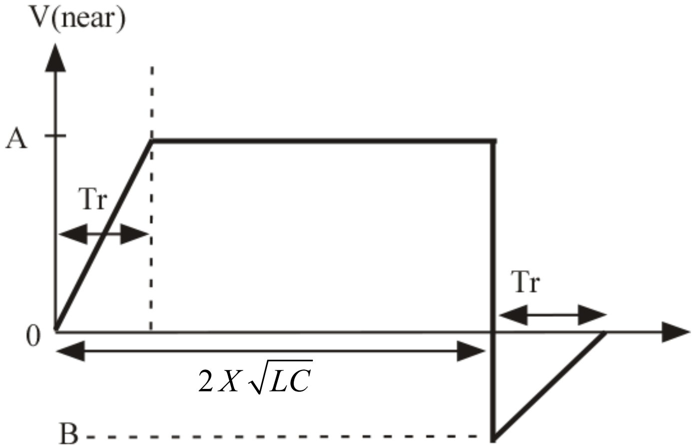


$$B = -\frac{V(input)\,X\sqrt{LC}}{2T_r}\left(\frac{L_M}{L} - \frac{C_M}{C}\right)$$

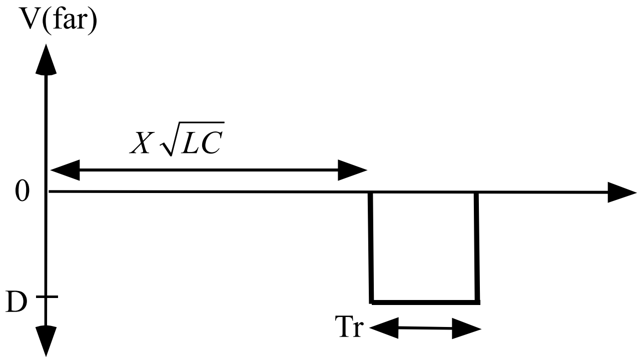
Digital Crosstalk - Case 2





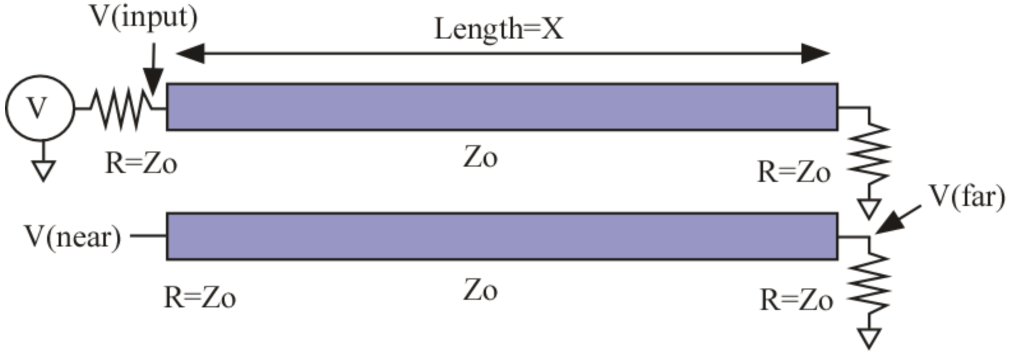


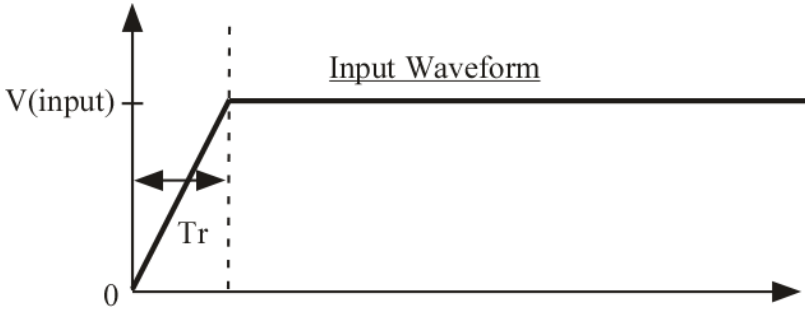
$$A=\frac{V(input)}{4}\left(\frac{L_M}{L}+\frac{C_M}{C}\right)$$

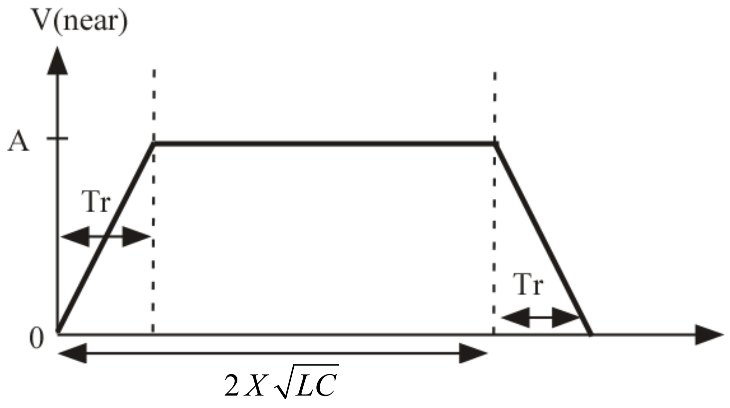


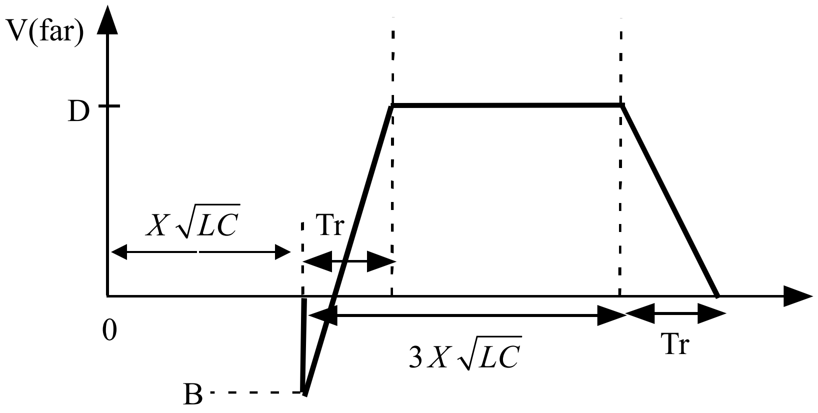
$$D=-\frac{V(input)X\sqrt{LC}}{T_r}\left(\frac{L_M}{L}-\frac{C_M}{C}\right)$$

Digital Crosstalk - Case 3









$$A = \frac{V(input)}{2}\left(\frac{L_M}{L} + \frac{C_M}{C}\right) \qquad B = -\frac{V(input)X\sqrt{LC}}{2T_r}\left(\frac{L_M}{L} - \frac{C_M}{C}\right) \qquad D = \frac{V}{4}\left(\frac{L_M}{L} - \frac{C_M}{C}\right)$$

Crosstalk Facts

- If the rise or fall time is short compared to the delay of the line, the near-end crosstalk noise is independent of the rise time.

- If the rise or fall time is long compared to the delay of the line, the near-end crosstalk noise is dependent on the rise time

- The far-end crosstalk is always dependent on the rise or fall time

Crosstalk Facts

- Assume that the transmission lines are terminated
- The near-end crosstalk will begin at $t=0$ and have a duration of $2\,t_D$.
- The far-end crosstalk will occur at time $t=t_D$ and have a duration approximately equal to the signal rise or fall time

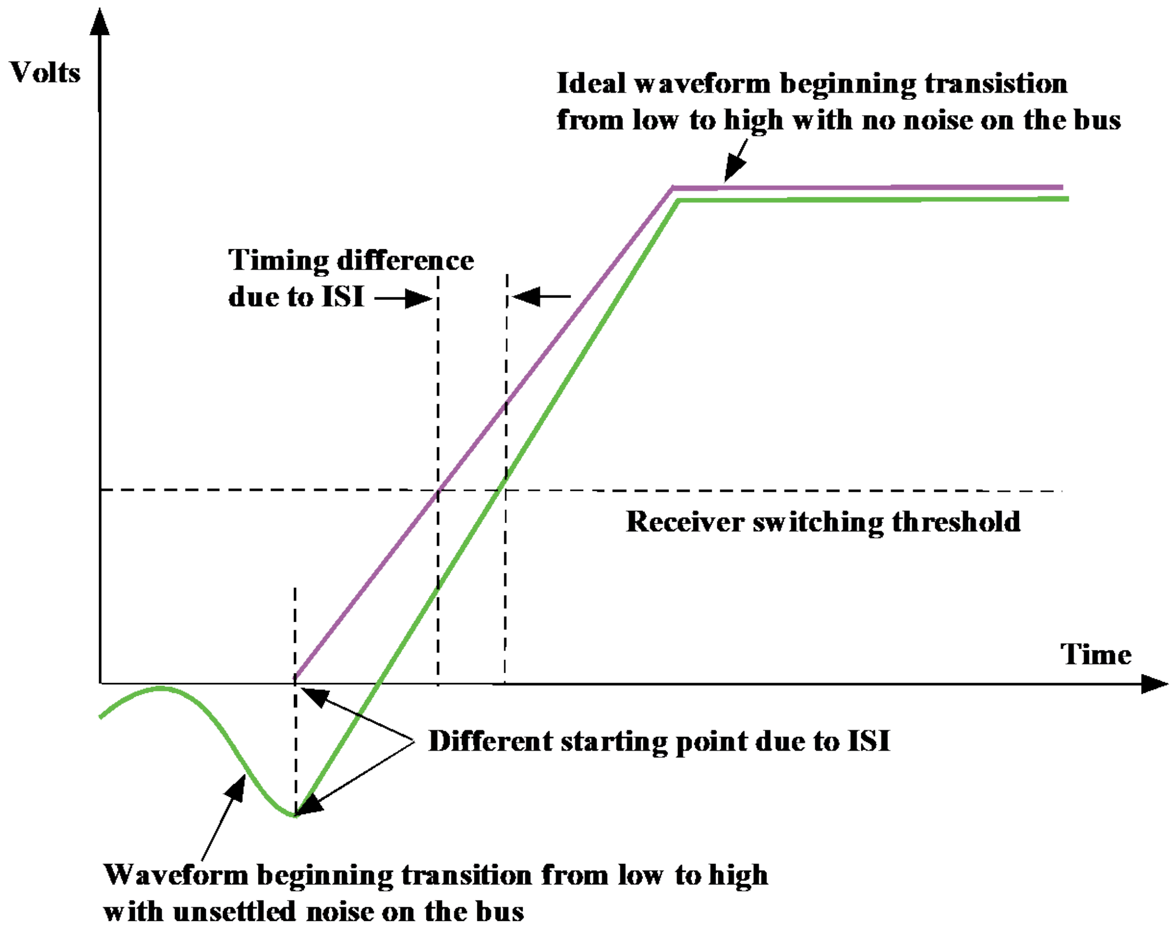
$$t_D = X\sqrt{LC}$$

X is the length of the lines

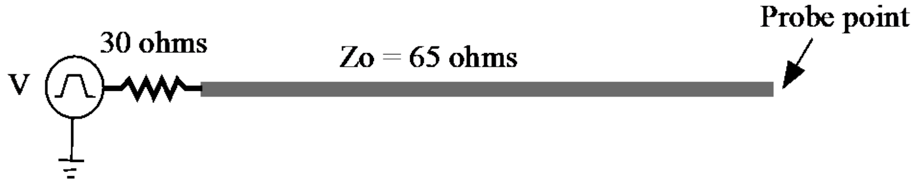
Intersymbol Interference (ISI)

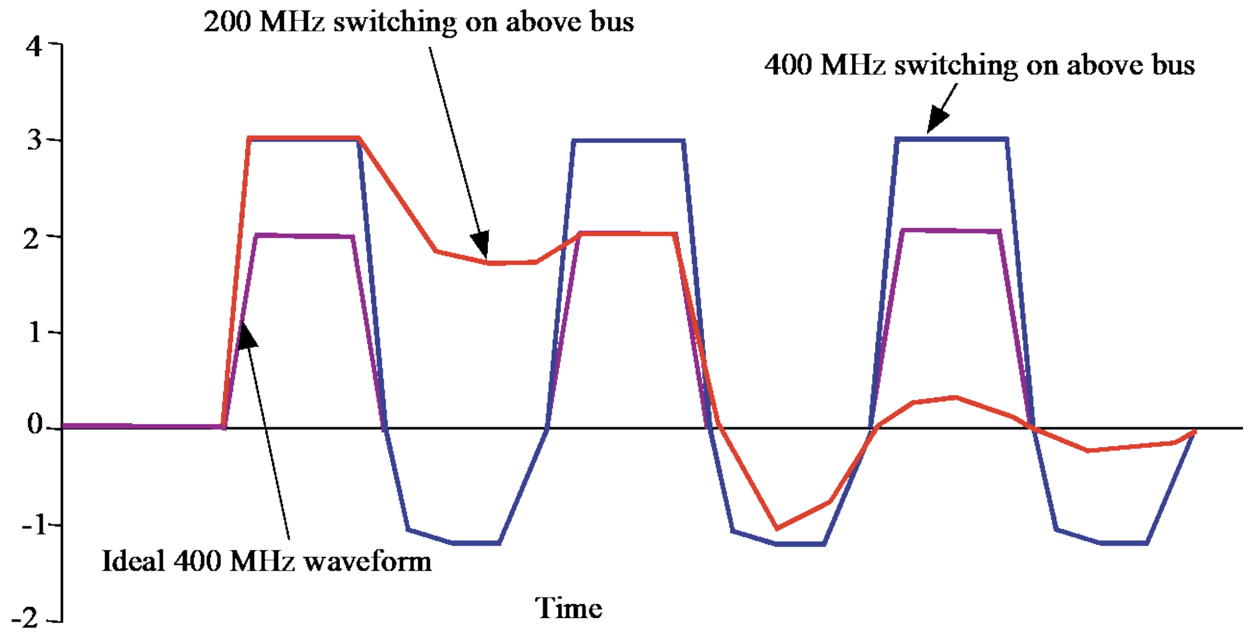
- Signal launched on a transmission line can be affected by previous signals as result of reflections
- ISI can be a major concern especially if the signal delay is smaller than twice the time of flight
- ISI can have devastating effects
- Noise must be allowed to settled before next signal is sent

Intersymbol Interference



Intersymbol Interference and Signal Integrity





Minimizing ISI

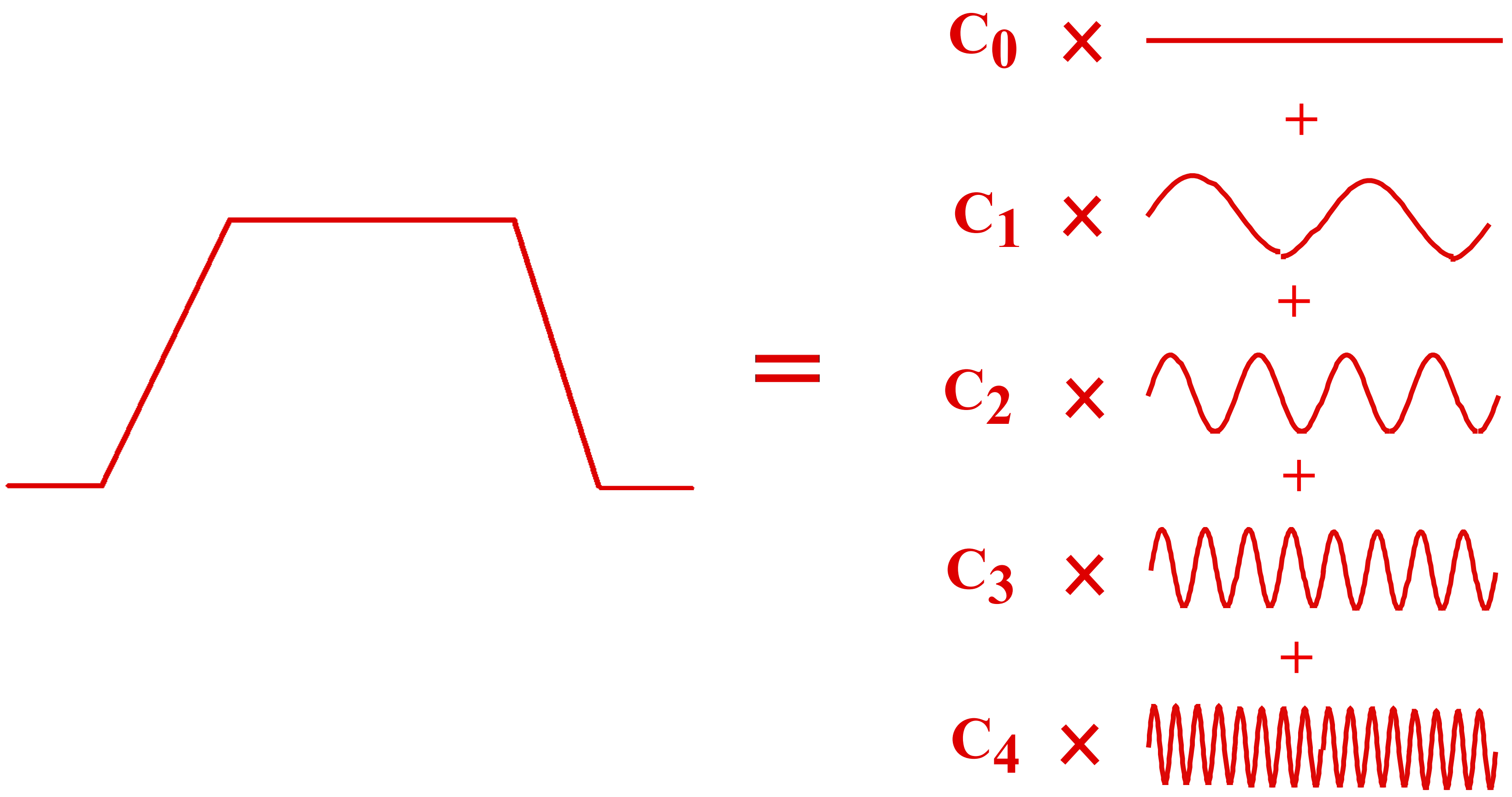
- Minimize reflections on the bus by avoiding impedance discontinuities

- Minimize stub lengths and large parasitics from package sockets or connectors

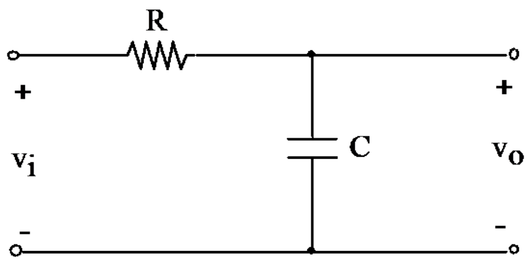
- Keep interconnects as short as possible (minimize delay)

- Minimize crosstalk effects

Frequency Components of Digital Signal



RC Network

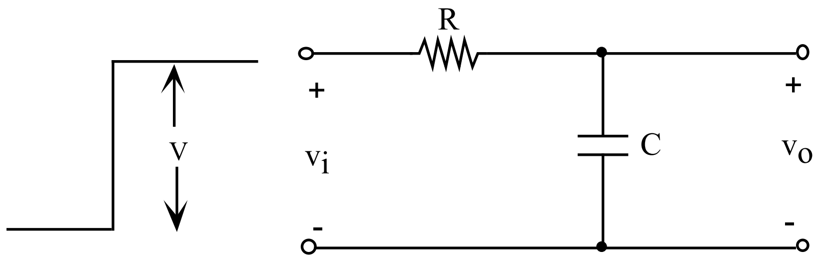


A is the steady-state gain of the network; $A = \frac{v_o(f)}{v_i(f)}$

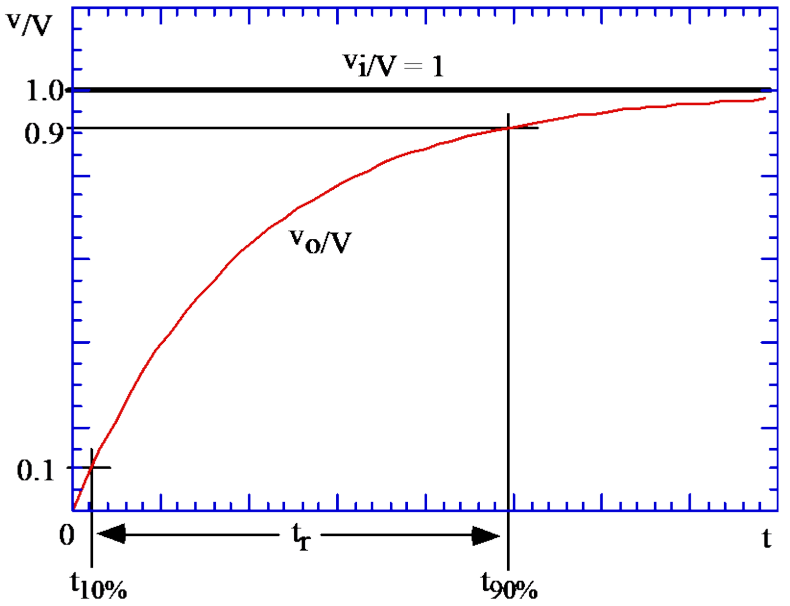
$$|A| = \frac{1}{\sqrt{1+\left(f/f_2\right)^2}} \qquad f_2 = \frac{1}{2\pi RC}$$

The gain falls to 0.707 of its low-frequency value at the frequency f_2. f_2 is the *upper 3-dB frequency* or the 3-dB bandwidth of the RC network.

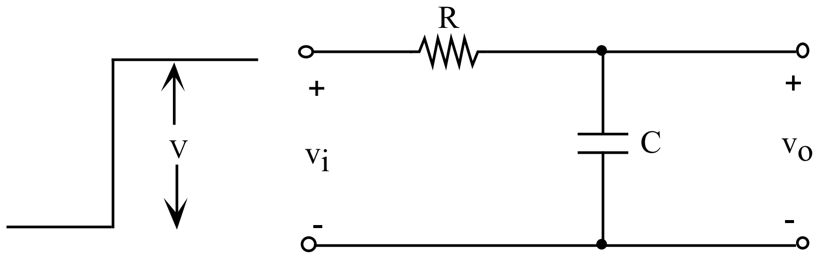
RC Network



$$v_o = V\left(1 - e^{-t/RC}\right)$$



RC Network



Rise time : $t_r = t_{90\%} - t_{10\%}$

$$t_r = 2.2RC = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2}$$

<u>Observation</u>: Simulating a 1-ns rise-time step requires a 3-dB bandwidth in the order of 350 MHz.

<u>Rule of thumb</u>: A 1-ns pulse requires a circuit with a 3-dB bandwidth of the order of 2 GHz.

Frequency Dependence of Lumped Circuit Models

At higher frequencies, a lumped circuit model is no longer accurate for interconnects and one must use a distributed model. Transition frequency depends on the dimensions and relative magnitude of the interconnect parameters.

$$f \approx \frac{0.3 \times 10^9}{10d\sqrt{\varepsilon_r}} \qquad t_r \approx \frac{0.35}{f}$$

Connector Design

- Minimize physical length of connector pins.
- Maximize the ratio of power and ground pins to the signal pins. If possible these ratios should be < 1.
- Place each signal pin as close as possible to a current return pin.
- Place power pins adjacent to ground pins.

8-Bit Connector Pin-Out Options

G	S	S	S	S	S	S	S	S	P

inferior

G	S	S	P	S	S	G	S	S	P	S	S	G

improved

G	S	P	S	G	S	P	S	G	S	P	S	G	S	P	S	G

More improved

G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P

Optimal

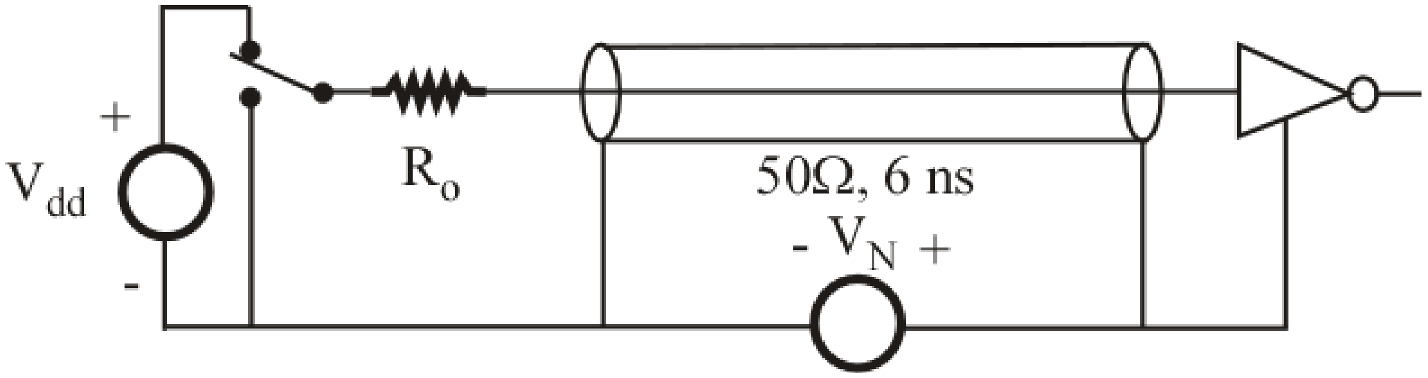
Signaling Conventions

- A good signaling convention isolates a signal from noise to provide noise immunity.

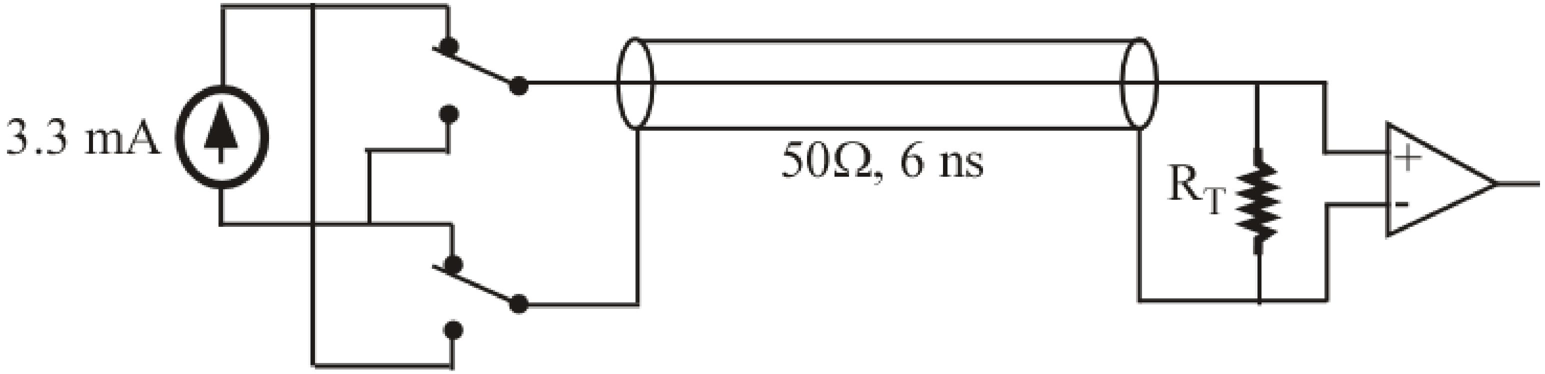
- Most signaling conventions in common use are based on standards and are actually quite poor.

- Many modern systems define their own signaling conventions rather than employ the standards

Transmission Systems



Full-swing CMOS transmission system



Low-swing current-mode transmission system

Transmission Systems

	CMOS	LSC
Signaling	Voltage mode: 0=GND, 1=V_{dd}	Current mode: 0=-3.3 mA 1=+3.3 mA
Reference	Power supply: V_r~V_{dd}/2	Self-centered: I_r=0 mA
Termination	Series terminated in output impedance of driver	Parallel-terminated at receiver with R_T within 10% of Z_o
Signal energy	1.3 nJ	22 pJ
Power dissipation	130 mW	11mW
Noise immunity	1.2:1 actual:required signal swing (with LSC receiver)	3.6:1
Delay	18 ns	6 ns

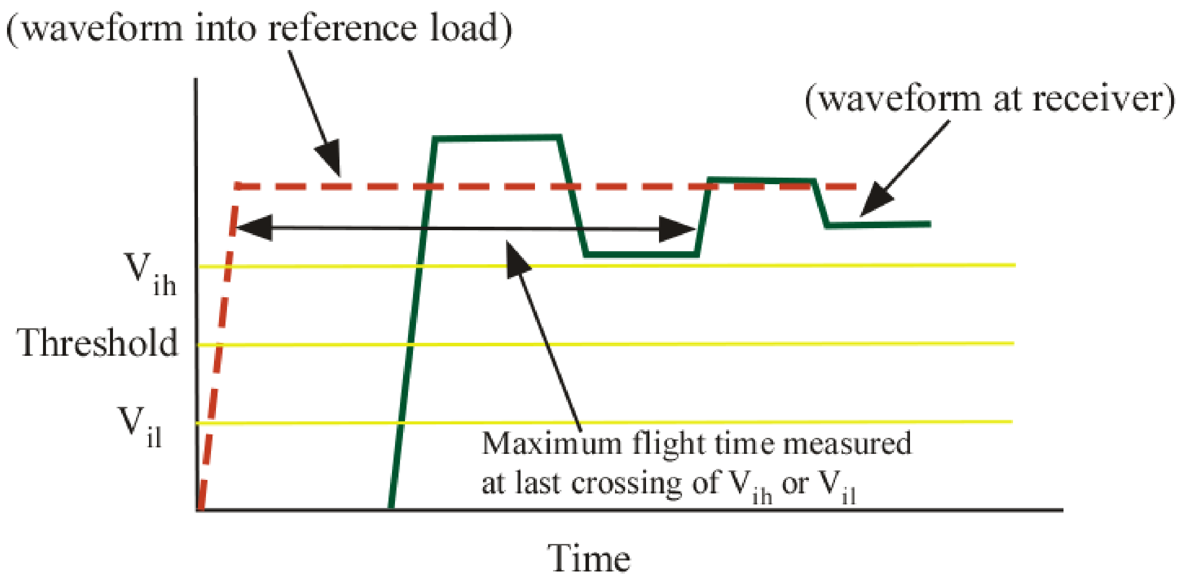
CMOS vs LSC

- With the worst-case combinations of noise sources the CMOS signaling system will fail
- The LSC system has 3.6 times the signal swing required.
- The transmission delay of the LSC system is the one-way delay of the transmission line.
- The CMOS driver must wait for the line to ring up to the full voltage.

CMOS vs LSC

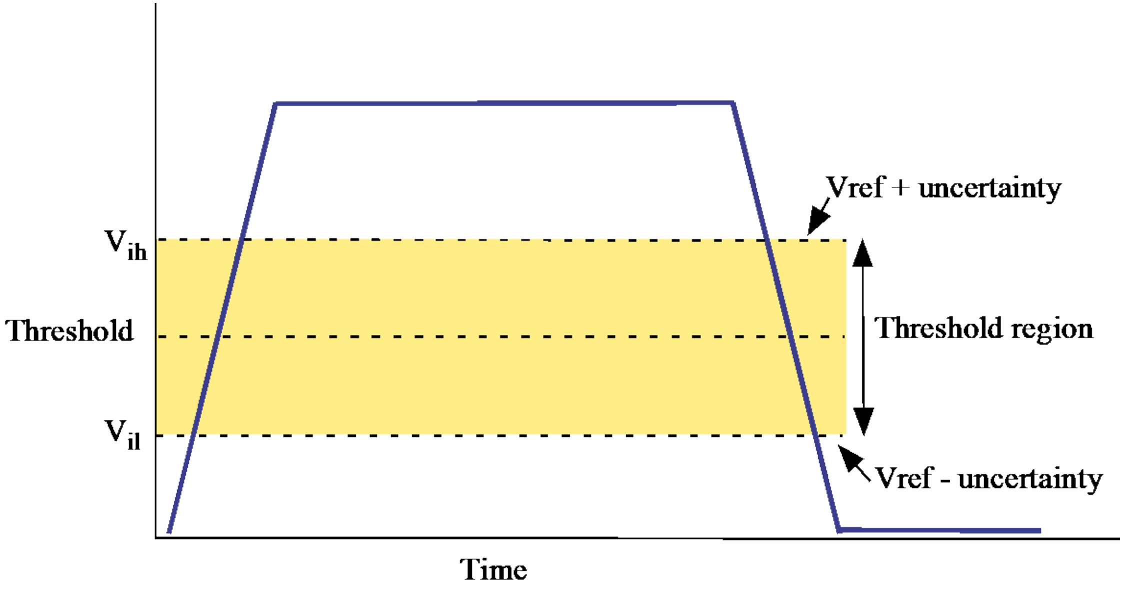
- Basic CMOS system is most commonly used and yet is far from optimal
- Large energy signal is used where it is not needed
- Transmitted signal not isolated from supply noise
- Receiver uses reference that changes significantly with process variations

Ringback and Rise Time Control



- Violation into threshold region
- Detrimental even if threshold is not crossed
- Can exacerbate ISI
- Can be aggravated by nonlinear (time varying) terminations
- Can increase skew between signals

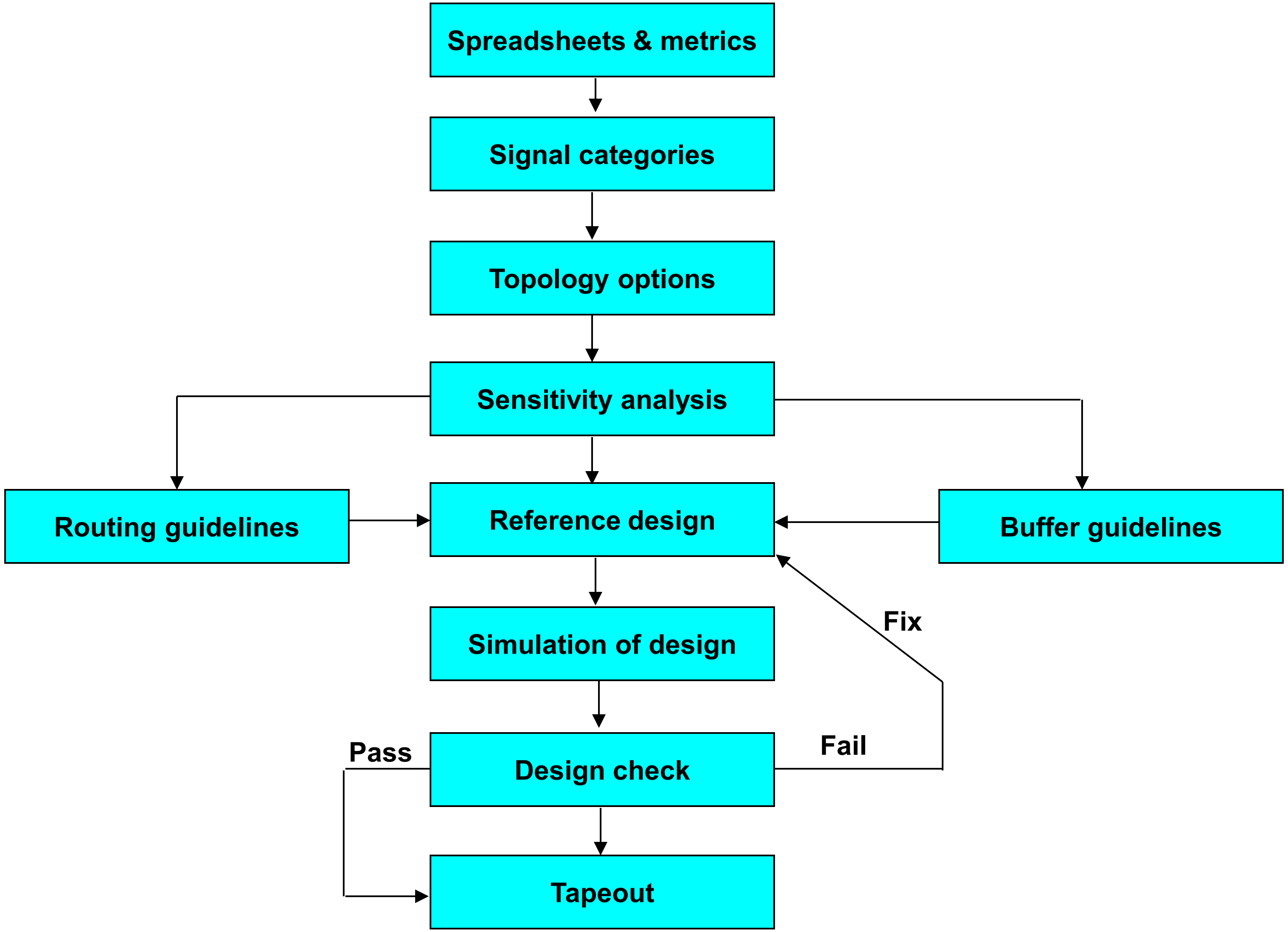
Voltage Reference Uncertainty



Major Contributors

- Power supply effects (SSN, ground bounce, rail collapse)
- Noise from IC
- Receiver transistor mismatches
- Return path discontinuities
- Coupling to reference voltage circuitry

Efficient Bus Design Methodology



Bus System Variables

- I/O capacitance
- Trace length, velocity, and impedance
- Interlayer impedance variations
- Buffer strengths and edge rates
- Termination values
- Receiver setup and hold times
- Interconnect skew specifications
- Package, daughtercard, and parameters

Differential vs Single-Ended

Line impedance: $Z_o = 50\ \Omega$
Source Resistance: $R_o = 50\ \Omega$
Lead Inductance: L = 5 nH
Pin count: P = 32
Data rate: TBR = 8GB/s

B: Bit rate per signal pin
TBR: Total bit rate
S: Number of signal pins
N: Number of return pins

$$S+N=P$$

$$S*B=TBR$$

$$K_{XRT} \le \frac{(N-1)Z_{RT}}{R_O+Z_O}$$

Z_{RT} is due to the lead inductance
Z_{RT} ➔ Z_{RT}/N since there are N ground pins
Need to determine S and N

Even and Odd Modes

$$v_d = \frac{1}{\sqrt{(L_s - L_m)(C_s + 2C_m)}} \qquad Z_d = \sqrt{\frac{L_s - L_m}{C_s + 2C_m}}$$

$$v_e = \frac{1}{\sqrt{(L_s + L_m)C_s}} \qquad Z_e = \sqrt{\frac{L_s + L_m}{C_s}}$$

In general, odd-mode impedance is smaller than even-mode impedance.

In general, odd-mode velocity is larger than even-mode velocity.

Coupled Lines

Line Space

$$V_1 = Z_{11} I_1 + Z_{12} I_2$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Modal Space

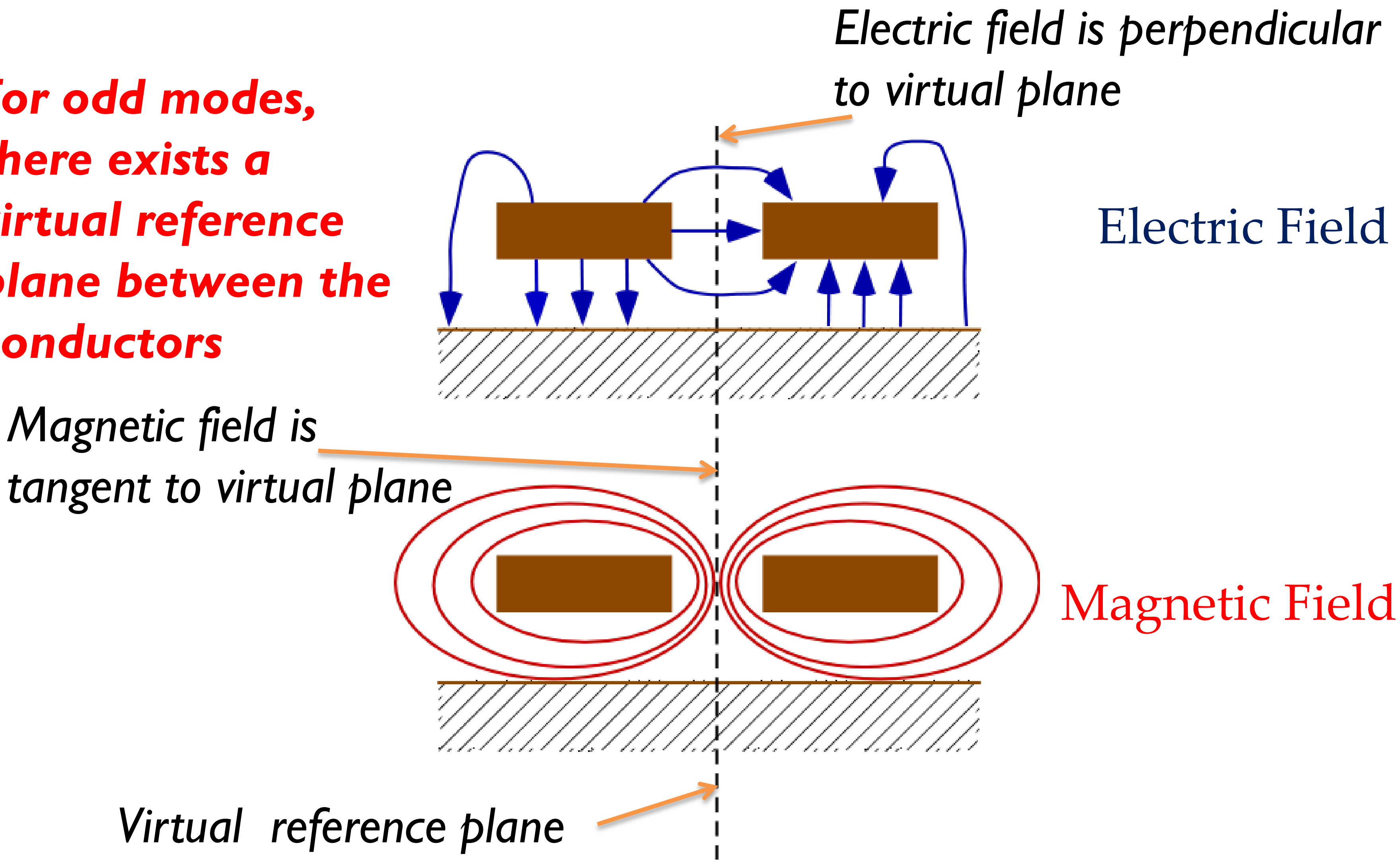
$$V_e = Z_e I_e$$

$$V_d = Z_d I_d$$

$$\begin{bmatrix} V_e \\ V_d \end{bmatrix} = \begin{bmatrix} Z_e & 0 \\ 0 & Z_d \end{bmatrix} \begin{bmatrix} I_e \\ I_d \end{bmatrix}$$

Virtual Reference Plane

For odd modes, there exists a virtual reference plane between the conductors



Low-Voltage Differential Signaling (LVDS)

Definition: Method to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces or a balanced cable

Criteria for high-performance communication

- Bandwidth
- Low Power
- Low Noise

Solution exists for very short and very long distances; however for board-to-board or box-to-box, this is a challenge

Why LVDS?

1. Differential transmission is less susceptible to common mode noise

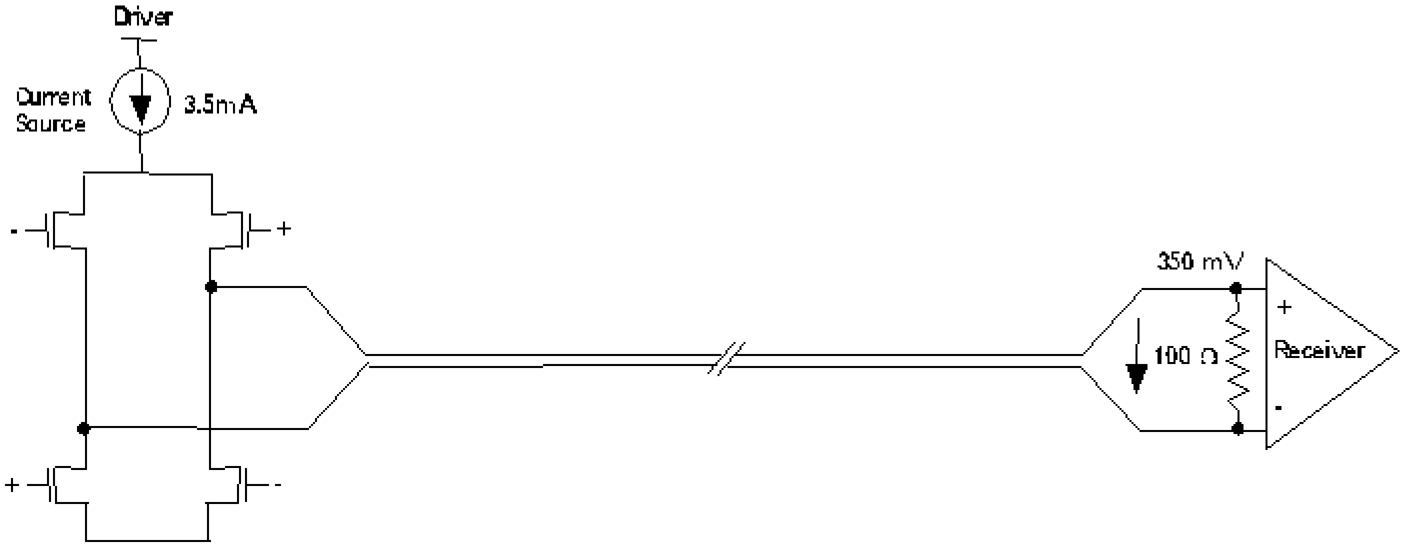
2. Consequently they can use lower voltage swings

3. In PC board (microstrip) odd-mode propagation is faster

LVDS Attributes for EMI

1. Low output voltage swing
2. Slow edge rates
3. Odd-mode operation (magnetic fields cancel)
4. Soft output corner transitions

LVDS Driver and Receiver



- Majority of current flows across 100-ohm resistor
- Switching changes the direction of current
- Logic state determined by current direction

LVDS Standard

- **Maximum Switching Speed**
  - Depends on line driver
  - Depends on selected media (type and length)

- **LVDS Saves Power**
  - Power dissipated in load is small
  - LVDS devices are in CMOS=>low static power
  - Lowers system power through current-mode

- **Design Practices**
  - Matching is critical
  - Preserve balance

Differential Signaling Technologies

	RS-422	PECL	LVDS
Differential Driver Output Voltage	±2 to ±5V	±600-1000 mV	±250-450 mV
Receiver Input Threshold	±200 mV	±200-300mV	±100 mV
Data Rate	<30Mbps	>400Mbps	>400Mbps
Supply Current Quad Driver (no load, static)	60 mA (max)	32-65mA (max)	8.0mA
Supply Current Quad Receiver (no load, static)	23mA (max)	40mA (max)	15mA (max)
Propagation Delay of Driver	11ns (max)	4.5ns (max)	1.7ns (max)
Propagation Delay of Receiver	30ns (max)	7.0ns (max)	2.7ns (max)
Pulse Skew (Driver or Receiver)	N/A	500ps (max)	400ps (max)