

Modeling of Multilayered Power Distribution Planes Using Transmission Matrix Method

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Abstract—This paper presents a method for analyzing multilayered rectangular and irregular shaped power distribution planes in the frequency and time domain. The analysis includes the effect of vias on the power distribution network. The planes are modeled using a two dimensional array of distributed RLCG circuit elements. Planes are connected in parallel using vias, which are modeled as self and mutual inductors. For the computation of the power distribution impedances at specific points in the network, a multiinput and multioutput transmission matrix method has been used. This is much faster than Spice and requires smaller memory. Using the transmission matrix method, via effects and the effects of multiple rectangular power/ground plane pairs without and with decoupling capacitors have been analyzed for realistic structures.

Index Terms—Loop inductance, power distribution system, simultaneous switching noise, transmission matrix method.

I. INTRODUCTION

AN IMPORTANT area in high-speed digital systems is the design of the power and ground planes arising in power distribution networks. This network supplies voltage and current to the drivers and receivers that generate and receive the signals. A major challenge in the design of planes, which forms an integral part of the power distribution system (PDS) for gigahertz (GHz) packages and boards, is the supply of clean power to the switching circuits. A major problem arising in power distribution networks is simultaneous switching noise (SSN) which is induced by the power and ground inductance. It has been recognized that power supply noise induced by a large number of simultaneously switching circuits in a printed wiring board (PWB) or multichip module (MCM) can limit the performance of the system [1]. As clock speeds increase, and signal rise time and supply voltages decrease, the power supply noise, commonly known as delta-I noise or switching noise, appears as an undesired voltage fluctuation on the power/ground planes. This is caused by the fast transient currents which excite cavity modes between the planes during the switching activity of the digital circuits [2]. This leads to unwanted effects on the PDS such as ground bounce, power supply compression, and electromagnetic interference. Hence, for an ideal power distribution network, the desired characteristics are zero self impedance and zero trans-impedance between ports at all frequencies [2], [3]. Therefore, the power distribution network should be designed to provide a low impedance power/ground connection to the devices, to minimize coupling between devices, and to minimize

the resonant frequencies over the entire bandwidth of the signal. However, the design of the PDS to meet this goal is difficult for modern CMOS microprocessors or application specific integrated circuits (ASICs) which contain thousands of drivers that can switch simultaneously within one clock cycle. As a result, for the analysis and design of the PDS to suppress SSN, efficient noise prediction methods are necessary.

In [3]–[5], Spice models have been used to analyze power/ground planes. However, as the size and frequency of the power distribution network increases, the use of Spice is limited due to larger memory requirements and computational time. In a realistic package/board, since the PDS consists of numerous vias, decoupling capacitors, signal lines, irregular geometries, and multiple plane layers, the number of transmission line segments required may become very large. As a result, large memory requirements and a considerable CPU run time are required for analysis. The transmission matrix method discussed in this paper offers a more efficient technique for solving these kinds of problems.

In [6], [7], for the analysis of an arbitrary shaped power/ground plane pair, it was demonstrated that the transmission matrix method required a smaller memory, smaller CPU time and could be applied to arbitrary geometries as compared to Spice. This is because the transmission matrix method is based on a multiinput, multioutput transfer function which enables the matrix for the entire power distribution network (with $N \times M$ unit cells) to be computed as the product of individual square matrices formed by $2N$ -port networks having N input ports and N output ports [6]. Once the unit cell parameters are computed, the transmission matrix method can be efficiently applied to any arbitrary shaped plane geometry.

In this paper, the transmission matrix method has been extended to a third dimension to analyze multilayered power distribution networks. In addition, vias have been included in the method. Using the via inductance extraction program FastHenry, which was developed at MIT, self and mutual inductances for power/ground via pairs have been extracted and added to the transmission matrix method. This paper, which is an extension of [6], [7], discusses the use of the transmission matrix method with Π model unit cells for computing impedances between 2 or more ports. However, unlike [6], [7] which was based on a column of unit cells confined to a single plane pair, each individual square matrix represents a plane pair in this paper. Where applicable, the results have been compared with Spice, where the cavity resonator model was used for simulation [8]. Multilayered power/ground planes have also been modeled with via inductances represented as short circuits, with vias as self inductances which are defined as loop inductances for each power/ground via pair, and with

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vias coupled to each other to demonstrate the differences in the computed results. Using the three types of via connections, the frequency response of multilayered power/ground plane structures made up of five, ten, and 15 plane pairs has been compared.

This paper, which is an expanded version of [9] and [10], is organized as follows.

- 1) In Section II, the extraction of equivalent circuit parameters for a Π unit cell has been discussed.
- 2) The mathematical details of the transmission matrix method for the analysis of multilayered power/ground planes are discussed in Section III. They are divided into four major parts; namely, power/ground planes, vias and via coupling, decoupling capacitors, and impedance computation at specific ports.
- 3) In Section IV, using inverse discrete Fourier transform (IDFT) and convolution, the transient response in the time domain has been generated from the frequency domain data.
- 4) In Section V, the accuracy of the transmission matrix method has been verified by comparing it with the cavity resonator model for a multilayered structure.
- 5) In Section VI, the transmission matrix method has been used to examine the effects of multilayered power/ground planes without and with decoupling capacitors, where vias are represented as short circuits, self inductances, and self and mutual inductances. Two test structures have been analyzed namely, uniformly distributed via connections and randomly distributed via connections to demonstrate the difference between symmetric and asymmetric structures.
- 6) The transmission matrix method has been applied to multilayered irregular shaped power/ground plane pairs having different geometries and dielectric thickness in Section VII followed by the conclusion in Section VIII.

II. MODELING OF PLANE LAYERS USING UNIT CELLS

Fig. 1 shows multilayered power distribution planes, which are commonly used in computer applications. In Fig. 1, vias are used to connect planes with the same potential. For example, all the ground planes (G1, G2, G3) could be shorted together through vias. From quasistatic approximations where the dielectric separation (d) is much less than the metal dimensions and the wavelength (λ) [11], which is true for power/ground plane pairs, each power/ground plane pair can be divided into unit cells with a lumped element model for each cell, as described in [3]. Each cell consists of an equivalent circuit with R, L, C, and G components, as shown in Fig. 2.

Using the equations for a parallel plate [11], from the lateral dimension of a unit cell (w), separation between planes (d), dielectric constant (ϵ), loss tangent of dielectric [$\tan(\delta)$], metal thickness (t), and metal conductivity (σ_c), the equivalent circuit parameters of a unit cell can be computed as

$$C = \epsilon_o \epsilon_r \frac{w^2}{d} \quad L = \mu_o d \quad R_{dc} = \frac{2}{\sigma_c t}$$

$$R_{ac} = 2 \sqrt{\frac{\pi f \mu_o}{\sigma_c}} (1 + j) \quad G_d = \omega C \tan(\delta). \quad (1)$$

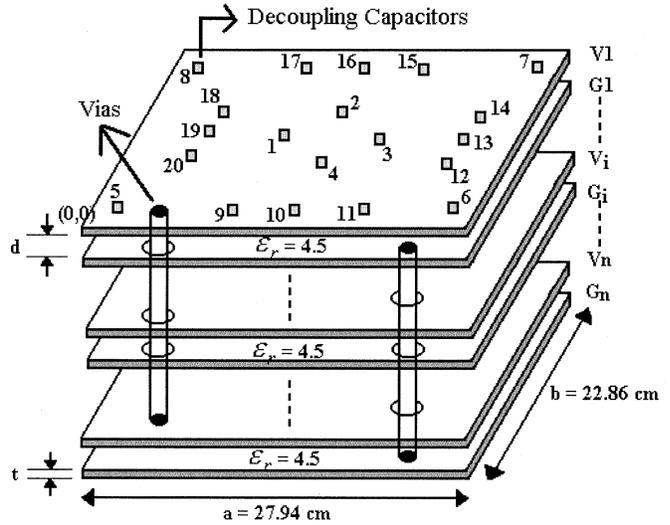


Fig. 1. Multilayered power/ground plane structure.

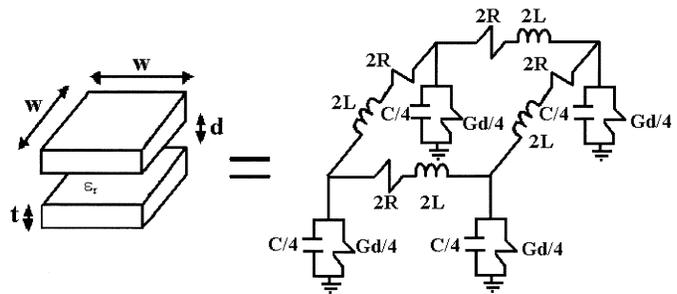


Fig. 2. Unit cell and equivalent circuit.

In the previous equation, ϵ_o is the permittivity of free space, μ_o is the permeability of free space, and ϵ_r is the relative permittivity of the dielectric. The parameter R_{dc} is the resistance of both the power and ground planes for a steady dc current where the planes are assumed to be of uniform cross section. The ac resistance R_{ac} accounts for the skin effect on both conductors. The shunt conductance G_d represents the dielectric loss in the material between the planes.

Using the unit cell, a distributed network of RLCG elements can be generated for the multilayered planes. Since this is a circuit model, it can be simulated in Spice by generating the modified nodal analysis (MNA) equations or using the transmission matrix method described in this paper. For good accuracy, a unit cell size that is ten times less than the wavelength at the highest frequency of interest is required.

III. TRANSMISSION MATRIX METHOD

A. Power/Ground Planes

As shown in Fig. 3, using a distributed network of RLCG elements, each rectangular plane pair can be divided into $(M - 1) \times (N - 1)$ unit cells. The $(M - 1) \times (N - 1)$ unit cells can be represented as a $2(M \times N) \times 2(M \times N)$ matrix formed by $(M \times N)$ input ports and $(M \times N)$ output ports.

From Fig. 3, the input ports are indexed as 1 to $(M \times N)$, and the output ports are indexed as $(M \times N) + 1$ to $2(M \times N)$. The transmission matrix for the $2(M \times N)$ port network can be

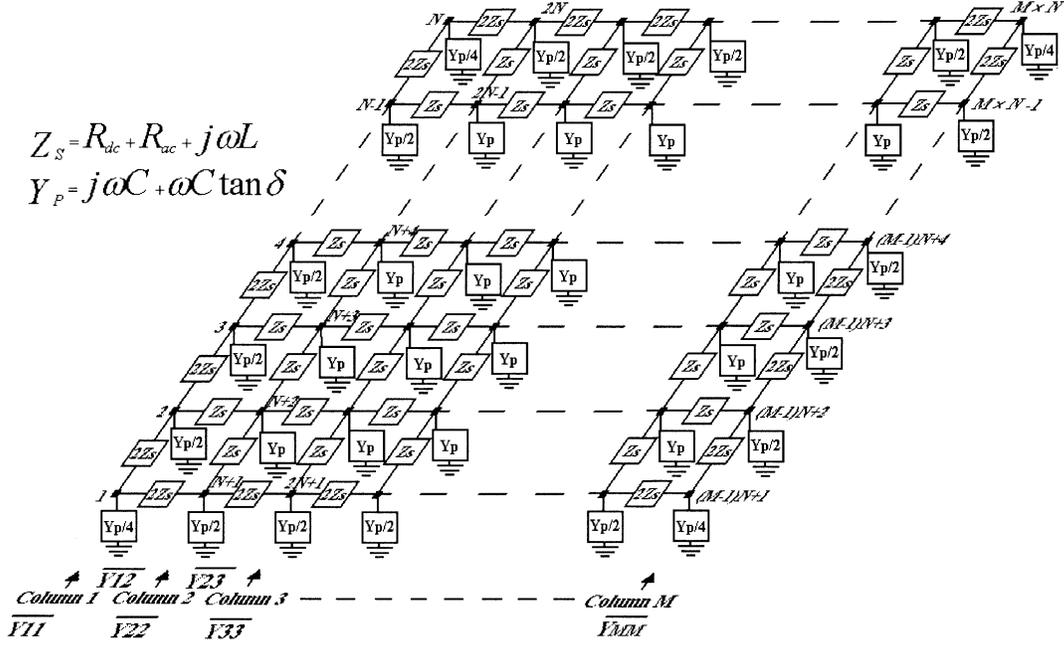


Fig. 3. Equivalent circuit for a pair of power/ground planes.

derived in terms of the node voltages and port currents. Using the 2×2 block matrix representation, the transmission matrix can be represented to relate the voltages and currents as

$$\begin{aligned} \overline{V}_{in} &= [A_p] \overline{V}_{out} + [B_p] \overline{I}_{out} \\ \overline{I}_{in} &= [C_p] \overline{V}_{out} + [D_p] \overline{I}_{out} \end{aligned}$$

where

$$\begin{aligned} \overline{V}_{in} &= \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{M \times N} \end{bmatrix} & \overline{I}_{in} &= \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{M \times N} \end{bmatrix} \\ \overline{V}_{out} &= \begin{bmatrix} V_{M \times N + 1} \\ V_{M \times N + 2} \\ \vdots \\ V_{2(M \times N)} \end{bmatrix} & \overline{I}_{out} &= \begin{bmatrix} I_{M \times N + 1} \\ I_{M \times N + 2} \\ \vdots \\ I_{2(M \times N)} \end{bmatrix}. \end{aligned} \quad (2)$$

The above transmission matrix for a power/ground plane pair can be rewritten in the simpler form

$$T_p = \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} = \begin{bmatrix} I & 0 \\ C_p & I \end{bmatrix} \quad (3)$$

where $[I]$ is the identity matrix, $[0]$ is the null matrix, and $[C_p]$ represents $(M \times N) \times (M \times N)$ matrices. In (3), the matrix $[C_p]$ is (3a), shown at the bottom of the next page. As can be seen in (3), the transmission matrix for a power/ground plane pair is tridiagonal and sparse, which enables reduction in memory usage and CPU run time when applied to realistic structures. The use of repeated unit cells enables the propagation of electromagnetic (EM) wave between the planes [3].

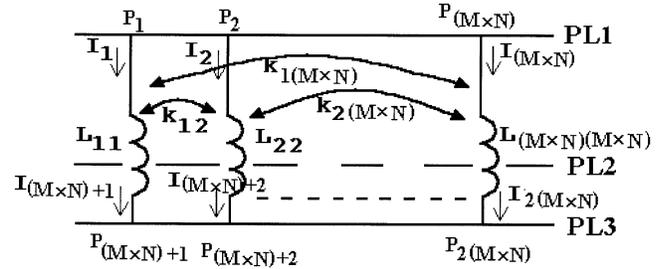


Fig. 4. Side view of power/ground planes with vias.

B. Vias and Via Coupling

Multilayered power distribution structures can be represented as power/ground plane pairs connected by vias. In a realistic structure, there are thousands of via connections for reducing the via inductances and for thermal dissipation. For high clock rates, these effects have to be included for computing the response in the high frequency range. Fig. 4 shows the side view of three conductor planes, which can be separated into two pairs of power/ground planes. The voltage planes PL1 and PL3 are connected together through vias for maintaining the same potential. It is assumed here that there are $(M \times N)$ power/ground via pairs, which can be decomposed into self and mutual inductances as shown in Fig. 4.

In terms of PL1 and PL3 conductor planes, the voltage and current between point P_1 and $P_{(M \times N) + 1}$, shown in Fig. 4, can be represented as follows:

$$\begin{aligned} V_{P_1 P_{(M \times N) + 1}} &= j\omega L_{11} I_1 + j\omega M_{12} I_2 + \dots \\ &\quad + j\omega M_{1(M \times N)} I_{(M \times N)} \\ I_1 &= I_{(M \times N) + 1} \end{aligned} \quad (4)$$

where mutual inductance $M_{ij} = k_{ij}\sqrt{L_{ii}L_{jj}}$. Other node voltages and port currents follow (4). In (4), the inductances of the vias represent loop inductances for each power/ground via pair.

Since mutual inductance can couple energy instantaneously between spatially separated points, the use of (4) can violate causality in the time domain. Hence, (4) is in direct contradiction to the modeling technique used for power/ground planes where an electromagnetic wave takes finite time to travel between spatially separated points. To ensure causality, the currents for mutual inductances ($I_2, I_3, \dots, I_{(M \times N)}$) shown in (4) are not excited until the EM wave reaches the via location. Hence, since the currents are causal, (4) preserves causality. This method has been used in Section VI to generate a causal solution.

From (4), the self and mutual inductances can be included into the transmission matrices of the vias based on the current direction in (3). The FastHenry extraction program from MIT provides losses, inductances, and polarity. The extracted real (loss) and imaginary (inductance) impedance values are frequency-dependant. As an approximation, frequency independent values have been used in this paper. These have been derived using

two frequency data samples; namely, low-frequency sample and high-frequency sample. Since inductance values are dominant in the high frequency range, the high frequency inductances are used over the entire frequency band. The loss (real) term for the via has been approximated as $(R_{dc} + R_{ac}\sqrt{f})$ which represents a skin effect approximation. From the two real parts of the data, the two unknown variables can be found and represented using

$$\begin{aligned} R_{dc} &= \frac{D_1\sqrt{f_2} - D_2\sqrt{f_1}}{\sqrt{f_2} - \sqrt{f_1}} \\ R_{ac} &= \frac{D_2 - D_1}{\sqrt{f_2} - \sqrt{f_1}} \end{aligned} \quad (5)$$

where D_1 and D_2 are the real values of data at frequencies f_1 and f_2 , respectively. From these values, the transmission matrix for vias in terms of input ports on PL1 and PL2, and output ports on PL3 and PL2 planes can be represented as (6), shown at the bottom of the next page. In (6), $Z_{via,ij} = R_{dc,ij} + R_{ac,ij}\sqrt{f} + j\omega L_{ij}$. As seen in (6), the transmission matrix loses the sparsity as the number of via pairs increases. To maintain sparsity, the negligible coupling coefficients (k_{ij}) in (6) can be neglected during matrix computation.

$$[C_p] = \begin{bmatrix} \bar{Y}_{11} & -\bar{Y}_{12} & 0 & 0 & \dots & \\ -\bar{Y}_{12} & \bar{Y}_{22} & -\bar{Y}_{23} & 0 & \dots & \\ 0 & -\bar{Y}_{23} & \bar{Y}_{33} & -\bar{Y}_{34} & \dots & \\ \vdots & \vdots & \vdots & \vdots & \dots & \\ 0 & 0 & 0 & 0 & \dots & \bar{Y}_{MM} \end{bmatrix}$$

where

$$\begin{aligned} \bar{Y}_{11} = \bar{Y}_{MM} = 0.5\bar{Y}_{22} = 0.5\bar{Y}_{33} = \dots = 0.5\bar{Y}_{(M-1)(M-1)} \\ = \begin{bmatrix} \frac{Y_p}{4} + \frac{1}{Z_s} & -\frac{1}{2Z_s} & 0 & \dots & 0 & 0 \\ -\frac{1}{2Z_s} & \frac{Y_p}{2} + \frac{2}{Z_s} & -\frac{1}{2Z_s} & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \dots & \ddots & \frac{Y_p}{2} + \frac{2}{Z_s} & -\frac{1}{2Z_s} \\ 0 & 0 & \dots & -\frac{1}{2Z_s} & \frac{Y_p}{4} + \frac{1}{Z_s} & \end{bmatrix} \\ \bar{Y}_{12} = \bar{Y}_{23} = \dots = \bar{Y}_{(M-1)M} = \begin{bmatrix} \frac{1}{2Z_s} & & & & & 0 \\ & \frac{1}{Z_s} & & & & \\ & & \ddots & & & \\ & & & \frac{1}{Z_s} & & \\ 0 & & & & & \frac{1}{2Z_s} \end{bmatrix} \end{aligned} \quad (3a)$$

C. Decoupling Capacitors

In the transmission matrix method, decoupling capacitors can readily be included into the matrices as demonstrated in [6], [7]. The impedance of a decoupling capacitor is represented using

$$Z_{cap} = R + j\omega L + \frac{1}{j\omega C} \quad (7)$$

where “ R ” is the Equivalent Series Resistance (ESR), “ L ” is the Equivalent Series Inductance (ESL), and “ C ” is the capacitance. The transmission matrix for decoupling capacitors can be represented as follows:

$$[T_{cap}] = \begin{bmatrix} I & 0 \\ C_{cap} & I \end{bmatrix}$$

where

$$[C_{cap}] = \begin{bmatrix} Y_{cap,1} & & & & \\ & \ddots & & & \\ & & Y_{cap,i} & & \\ & & & \ddots & \\ & 0 & & & Y_{cap,M \times N} \end{bmatrix} \quad (8)$$

where $Y_{cap,i} = 1/Z_{cap,i}$ and if there is no decoupling capacitor in the i th row, then $Y_{cap,i} = 0$.

D. Impedance Computation

The $2(M \times N) \times 2(M \times N)$ transmission matrix for the overall power distribution network which consists of a cascade of two or more networks can now be obtained by multiplying the individual matrices [6], [7]. For the rectangular multilayered planes in Fig. 1, since all the matrices for planes, vias, and decoupling capacitors have the same size, the response of the entire geometry can be obtained as a single $2(M \times N) \times 2(M \times N)$ matrix. The block representation of the cascade connection of $2(M \times N)$ port networks is shown in Fig. 5 using the $[T]$ matrix representation. As seen in Fig. 5, the entire system can be simplified into three blocks in terms of input and output ports, which have input voltage and current variables; and output voltage and

current variables, respectively. The transmission matrix for the block diagrams in Fig. 5 can be represented as follows:

$$\begin{aligned} [T_l] &= \begin{bmatrix} A_l & B_l \\ C_l & D_l \end{bmatrix} \\ &= \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_1 \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{1,2} \\ &\quad \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_2 \times \cdots \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_l \\ &\quad \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l,l+1} \\ [T_m] &= \begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix} \\ &= \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+1} \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l+1,l+2} \\ &\quad \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+2} \times \cdots \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+m} \\ [T_n] &= \begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} \\ &= \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l+m,l+m+1} \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+m+1} \\ &\quad \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l+m+1,l+m+2} \times \cdots \\ &\quad \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+m+n} \end{aligned} \quad (9)$$

where l , m , and n represent the number of power/ground plane pairs. From Fig. 5, two inversions of a $2(M \times N) \times 2(M \times N)$ matrix are needed to obtain the overall transmission matrix, and one inversion of a matrix is needed to convert to the $2(M \times N) \times 2(M \times N)$ impedance matrix $[Z]$ of the network [6], [7]. However, since most of the computational time is taken to invert a matrix, the number of matrix inversions needs to be minimized. Using one inversion of a matrix, which is the overall “ C ”

$$[T_{via}] = \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}$$

where

$$[B_{via}] = \begin{bmatrix} Z_{via,11} & Z_{via,12} & Z_{via,13} & \cdots & Z_{via,1(M \times N)} \\ Z_{via,12} & Z_{via,22} & Z_{via,23} & \cdots & Z_{via,2(M \times N)} \\ Z_{via,13} & Z_{via,23} & Z_{via,33} & \cdots & Z_{via,3(M \times N)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ Z_{via,1(M \times N)} & Z_{via,2(M \times N)} & Z_{via,3(M \times N)} & \cdots & Z_{via,(M \times N)(M \times N)} \end{bmatrix} \quad (6)$$

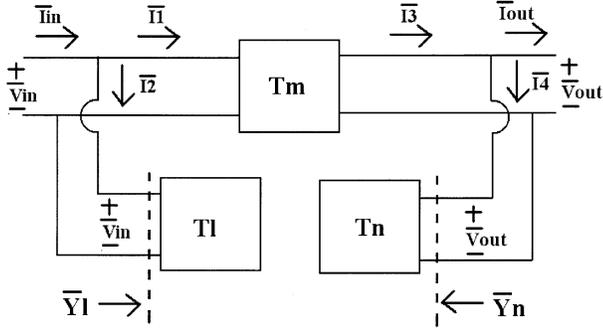


Fig. 5. Block diagram of entire system.

matrix computed by multiplications of the transmission matrix from Plane 1 to Plane $(l+m+n)$, it is possible to convert to the impedance matrix in (9). The overall $2(M \times N) \times 2(M \times N)$ impedance matrix for the multiple input and output ports can be computed as follows:

$$[Z_A] = R_n \times C_{inv} \times D_l \quad [Z_D] = A_n \times C_{inv} \times R_l$$

$$[Z_B] = [Z_C] = A_n \times C_{inv} \times D_l$$

where

$$C_{inv} = \left([C_l \quad D_l] \times \begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix} \times \begin{bmatrix} A_n \\ C_n \end{bmatrix} \right)^{-1}$$

$$R_n = A_m \times A_n + B_m \times C_n$$

$$R_l = C_l \times B_m + D_l \times D_m. \quad (10)$$

During the design of the power delivery system, the impedance at specific points on the network is often desired. This can either be the self impedance at a port or the transfer impedance between ports. This can reduce about half the computations during the matrix multiplications, requiring only the “ C ” full matrix, the rows of R_n and A_n , and the columns of R_l and D_l at the specific points.

IV. TRANSIENT RESPONSE

Using inverse discrete Fourier transform (IDFT) and convolution, the transient response of the power distribution network can be generated from the frequency domain data. Once the impedances in the frequency domain were computed using the transmission matrix method, a spline interpolation technique was applied to the complex data to obtain enough samples for IDFT. A transfer function ($H(\omega)$) was then constructed depending on the excitation source and converted to its impulse response ($h(t)$) using IDFT. Using the property that the output response in the time domain is real, the IDFT equation for computing the impulse response can be represented as [12]

$$h(t) = T_s F_s \operatorname{Re} \left\{ H(0) + 2 \sum_{n=1}^k H(2\pi F_s n) \times e^{j2\pi F_s n t} \right\}_{t=T_s m; m=0, 1, 2, \dots} \quad (11)$$

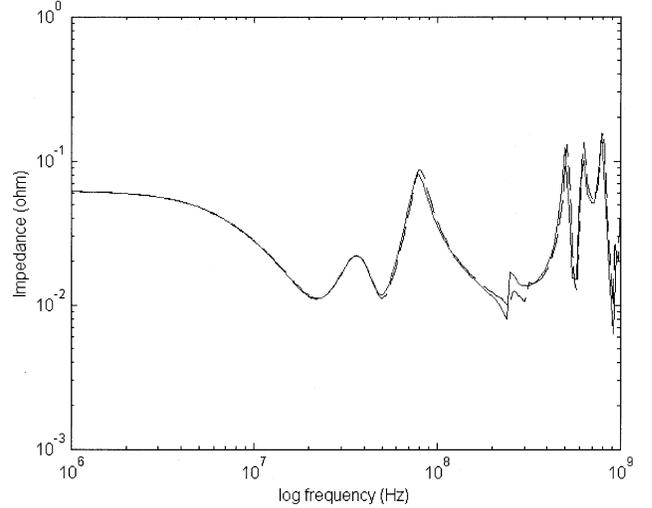


Fig. 6. Impedance without via effects: solid line: transmission matrix method, and dashed line: cavity resonator method.

where T_s is the sampling time and F_s is the sampling frequency. Finally, from the convolution of the two sequences $h(t)$ and $x(t)$ (input source), the output transfer voltage ($v(t)$) can be computed. In this paper, a triangular excitation current source was used with a short termination to mimic a transient current generated from the switching circuit.

V. COMPARISON OF TRANSMISSION MATRIX METHOD AND CAVITY RESONATOR METHOD FOR MULTILAYERED PLANES

The test structure consists of five 27.94 cm by 22.86 cm rectangular pairs of power/ground planes with FR4 dielectric with relative permittivity $\epsilon_r = 4.5$. While V1/G1, V2/G2, and V3/G2 plane pairs have a 109.22 μm dielectric thickness, V2/G1 and V3/G3 plane pairs have a 337.82 μm dielectric thickness. Fig. 1 shows the details of the plane layers. The conductor planes are made of copper ($\sigma_c = 5.8 \times 10^7 \text{ S/m}$) with a thickness of 30 μm and dielectric loss tangent $\tan(\delta) = 0.02$ at 1 GHz. An excitation point (Port 1) was located at $(x = 13.8 \text{ cm}, y = 11.25 \text{ cm})$ and an observation point (Port 2) at $(x = 2 \text{ cm}, y = 2 \text{ cm})$ between V1 and G1 planes. Three kinds of 32 decoupling capacitors ($C = 47 \text{ nF}$, ESL = 1 nH, ESR = 0.1 Ω ; $C = 10 \text{ nF}$, ESL = 1 nH, ESR = 0.1 Ω ; and $C = 20 \mu\text{F}$, ESL = 10 nH, ESR = 0.1 Ω), with locations as shown by the rectangular dots in Fig. 1, were incorporated between V1 and G1 planes. Twenty vias, which have the same locations as the decoupling capacitors, were vertically connected from power plane to power plane and from ground plane to ground plane. This ensures that the voltage planes and ground planes are at the same potential.

To check the accuracy of the transmission matrix method, the results have been compared with the cavity resonator model [8] for the structure shown in Fig. 1. Fig. 6 shows the transfer impedance between Port 1 and Port 2. In this section, via inductances were not included. Each plane pair was connected by a small value of resistors (1 $\mu\Omega$), so that the resistors can mimic a short circuit. For comparison, the propagating modes were set to $m = 6$, and $n = 5$ in the cavity resonator model described in [8]. As shown in Fig. 6, both the methods show good agreement over a frequency range of 1 GHz.

VI. EFFECT OF MULTILAYERED POWER/GROUND PLANES WITH VIAS

Vias are a common type of discontinuity in multilayered power distribution networks which can contain thousands of via connections. To accurately model such multilayered structures, it is necessary to consider via effects as the frequency bandwidth of the PDS increases. Since vias can be represented as inductances, the impedance of the PDS is affected in the high frequency range and the null resonant frequencies of the PDS are shifted to lower frequencies. To quantify the effect of multilayered power distribution planes with vias, three cases were compared for the multilayered network made up of five, ten, and 15 pairs of planes. The three test cases are

- 1) vias represented as short circuits;
- 2) vias represented as self inductances;
- 3) vias represented as self and mutual inductances.

Fig. 1 shows the cross section of “n” multilayered power distribution planes. Each two-dimensional plane pair is connected through vertical vias. The test structure consists of five, ten, and 15 rectangular pairs of power/ground planes with a $223.56 \mu\text{m}$ thick FR4 dielectric with relative permittivity $\epsilon_r = 4.5$. The conductor planes were made of copper ($\sigma_c = 5.8 \times 10^7 \text{ S/m}$) with a thickness of $30 \mu\text{m}$ and dielectric loss tangent $\tan(\delta) = 0.02$ at 1 GHz. Using a unit cell size of 7.62 mm by 7.62 mm , the PDS was divided into 37×30 unit cells, which resulted in a matrix size of 2356×2356 for each individual square transmission matrix. An excitation point (Port 1) was located at $(x = 0 \text{ cm}, y = 0 \text{ cm})$ and an observation point (Port 2) at $(x = 13.94 \text{ cm}, y = 11.43 \text{ cm})$ between V1 and G1 planes (top plane pair) for 5, 10, and 15 plane pairs. Decoupling capacitors with values described in Section V with locations as shown by the rectangular dots in Fig. 1 were incorporated between the V1 and G1 planes. For analysis, the test structure was simulated using two different scenarios for via connections; namely uniformly distributed via connections and randomly distributed via connections. While vias were connected to each plane at every unit cell (7.62 mm) position for uniformly distributed via connections (1178 vias), vias were only connected to each plane at the decoupling capacitor locations shown for randomly distributed via connections (20 vias). Using the via inductance extraction program FastHenry, self ($\sim 0.11 \text{ nH}$) and mutual inductances between vias were extracted and incorporated into the transmission matrix. Since coupling coefficients between the vertical layers were small, they were neglected in the computation.

Fig. 7 shows the simulated impedances without decoupling capacitors for five, ten, and 15 pairs, in which the vias were modeled as short circuits and as self inductances at every unit cell position (1178 vias). In the case of the via connections modeled as short circuits, when all the plane pairs have the same dimensions (a and b) with no decoupling capacitors, all the plane resonant frequencies (peak and null) remained unchanged, but the impedance magnitudes changed according to the number of plane pairs. This is due to the additional capacitance of the plane layers. However, the frequency response of the self impedance changed with the via self inductances, as shown in Fig. 7(b). As the number of plane pairs increased, the null resonant frequencies shifted to lower frequencies while

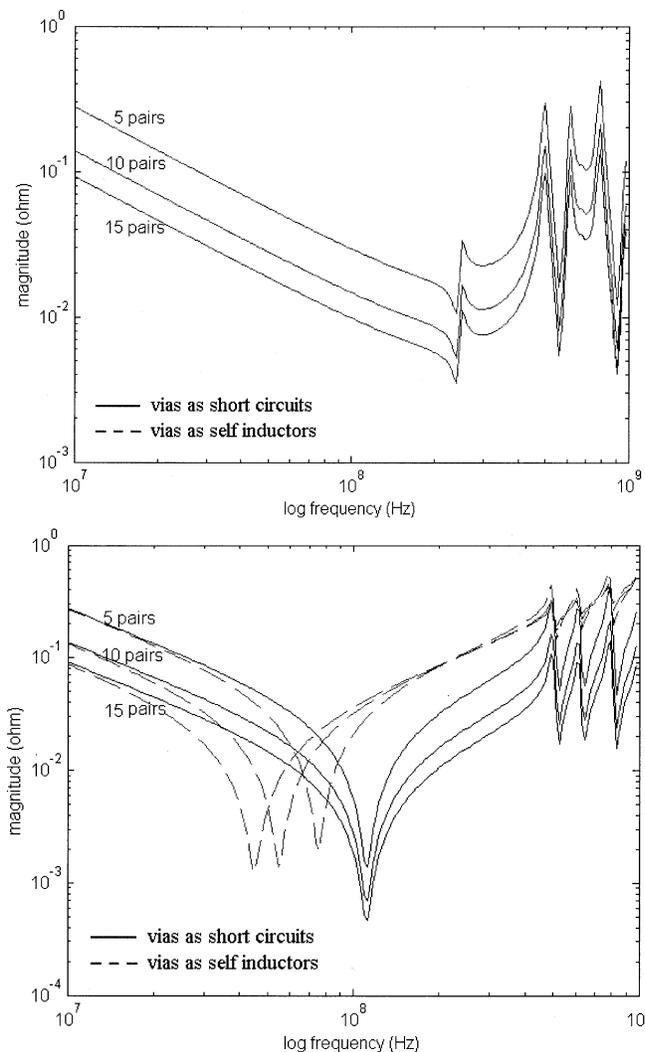


Fig. 7. Impedance magnitude without decoupling capacitors with vias connected at every unit cell position: (a) transfer impedance and (b) self impedance at port 2.

the peak resonant frequencies remained the same. In addition, the impedance magnitudes were closer to each other after the first null resonant frequency. This change is caused by the increased capacitance between the planes, which is proportional to the number of plane pairs. Hence, the low-frequency impedances were reduced, but the high-frequency impedances were not changed significantly as the number of plane pairs was increased. The effect of via inductance becomes prominent at high frequencies. For the transfer impedance, the resonant frequencies and magnitudes with via inductance connections were similar to those with short circuit connections, as shown in Fig. 7(a). This means that the transfer impedances on the same layer are not changed due to the presence of via inductances.

Fig. 8 shows the simulated impedances without and with decoupling capacitors for each structure, in which vias were modeled as short circuits, self inductances, and self and mutual inductances for ten pairs of planes. In this simulation, the vias were randomly distributed (20 vias). As shown in Fig. 8, the null resonant frequencies and magnitudes of all self and transfer impedances are affected in all three cases (even in the case of

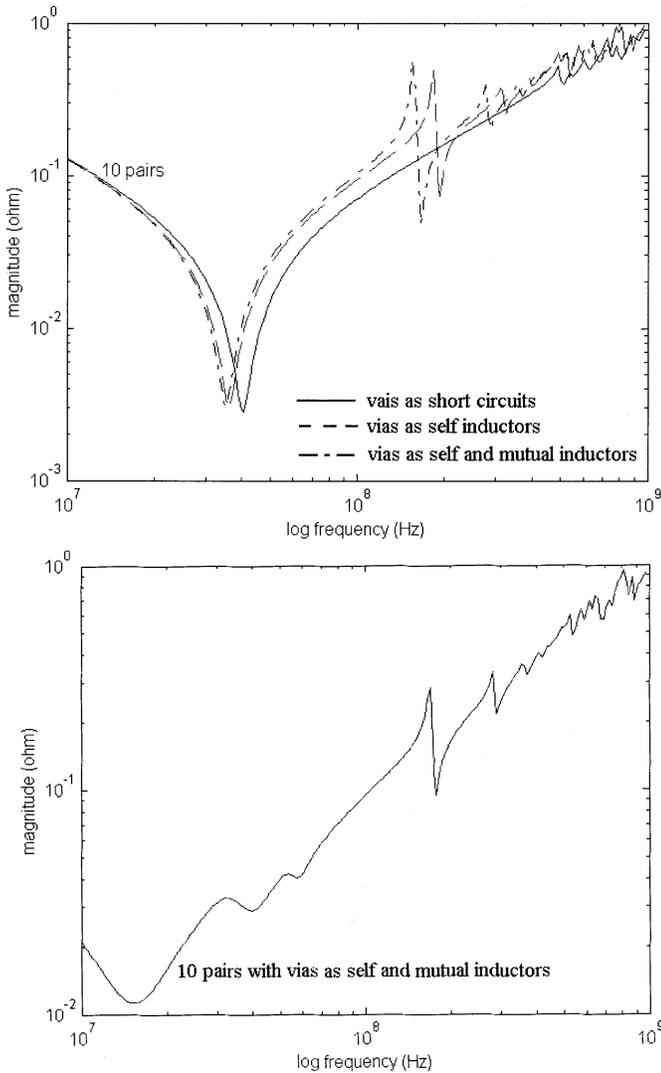


Fig. 8. Impedance magnitude without and with decoupling capacitors with vias randomly connected: (a) self impedance without decoupling capacitors at port 2 and (b) self impedance with decoupling capacitors at port 2.

short circuit connections which have the same null resonant frequencies for five, ten, and 15 planes, as shown in Fig. 7) as the frequency increases. While multilayered power/ground planes with via inductances have the same peak resonant frequencies of the planes without via inductances, they have additional resonant frequencies since the via inductances are coupled with the capacitances of the planes. However, if vias are modeled as short circuits, the additional resonant frequencies cannot be seen. As the number of planes with the via connections is increased, the frequency response can be affected by the vias at high frequencies even though the low-frequency impedances are reduced. The impedance magnitude with self and mutual inductances is close to the magnitude with stand-alone self inductances, but the additional resonant frequencies shift to lower frequencies due to the additional mutual inductances. Depending on the separation and number of vias, the coupling coefficients between power/ground via pairs can be secondary effects to the PDS. As the decoupling capacitors mentioned above are incorporated, the low-frequency impedances and the magnitude of the peak resonant frequencies are reduced, as shown Fig. 8(b).

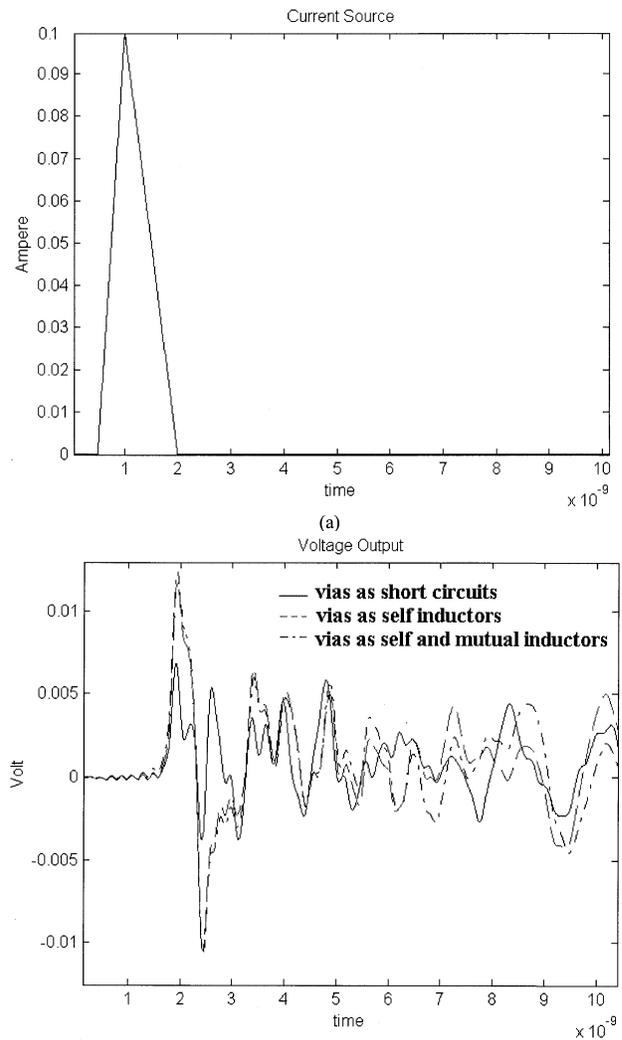


Fig. 9. Transient response of five plane pairs with the randomly populate via connections (20 vias): (a) current source at port 1 and (b) voltage output at port 2.

However, the inductances in the high frequency range are close to those without decoupling capacitors.

Based on the results in Figs. 7 and 8, for the analysis of multilayered plane pairs with vias, several issues have to be considered such as

- 1) the inductance and number of the vias in parallel connecting the planes;
- 2) the separation between the vias and port locations at which the impedance is desired;
- 3) the interaction between vias and plane capacitances.

Based on the comparison between the self impedances at Port 2 in Figs. 7 and 8, the inductance of the plane pairs is reduced as the number of vias is increased. Since vias are connected in parallel, the via inductance is reduced as the number of vias increases. This results in a reduction in the plane impedance with the additional resonant frequencies, which are caused by the coupling between the via inductances and the plane capacitances, that occur at higher frequencies.

To evaluate the noise due to the via inductances, the transient response for the five plane pairs with the randomly distributed via connections (20 vias) were compared for the three cases

TABLE I
MATRIX SIZE AND CPU RUN TIME COMPARISON

Number of Unit Cells	Parameter	Spice (MNA)	Transmission Matrix Method	Matrix Size comparison CPU: (without, with decaps)
37 X 30 X 5	Elements	57,520	57,520	0.1380% (483 s, 538 s)
	Nodes	40,195	5,890	
	Matrix size	63,410 X 63,410	2,356 X 2,356	
37 X 30 X 10	Elements	115,040	115,040	0.0345% (967 s, 1069 s)
	Nodes	80,390	11,780	
	Matrix Size	126,820 X 126,820	2,356 X 2,356	
37 X 30 X 15	Elements	172,560	172,560	0.0153% (1417 s, 1622 s)
	Nodes	120,585	23,560	
	Matrix Size	190,230 X 190,230	2,356 X 2,356	

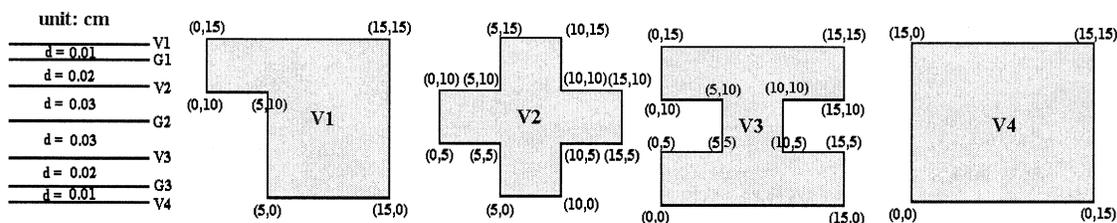


Fig. 10. Multilayered irregular shaped power/ground planes.

described earlier in the time domain. The transient output voltages were generated from the frequency impedance data from 0 Hz to 5 GHz. With a short termination at ($x = 27.94$ cm, $y = 22.86$ cm) between V3 and G3 planes (bottom plane pair), a 0.1 amp triangular current source with open source resistance was used to mimic a transient current generated from a switching circuit. The current source had a rise time of 500 ps and fall time of 1 ns, and sampled up to 100 ns using a sampling interval of 10 ps, as shown in Fig. 9(a). The transient output voltage for the three cases is shown in Fig. 9(b), where the voltage fluctuations continue even after the source is switched off, indicating the high quality factor of the plane cavity. As a comparison, vias modeled as inductances generate $\sim 2\times$ peak noise as compared to vias modeled as short circuits. However, the responses for the two cases *viz.*, vias modeled as self inductors and vias modeled as self and mutual inductors, are close to each other. In addition, the transient output voltage begins after a delay which is caused by the physical separation between the ports. The delay time of ~ 1.1 ns for the three cases is the same, indicating that causality of the system is preserved for all three cases, as described in Section III.

As mentioned in the Section I, the transmission matrix method enables memory saving and reduction in computation time. The memory required and computational time between Spice and the transmission matrix method have been compared in Table I for the five, ten, 15 plane pairs with the randomly distributed via connections, where vias were modeled as self and mutual inductances. On an average, the transmission matrix method requires less than 1% memory as compared to Spice. All the impedances between the two ports (Z_{11} , Z_{12} , and Z_{22}) were simulated with 200 frequency-sampling points

in MATLAB, and the CPU run time is shown in Table I. Since the transmission matrix method retains the same matrix size, the CPU time is almost linear for each additional plane pair. Most of the computational time is required to invert a matrix, as mentioned in Section III. Hence, the smaller the matrix, the smaller is the computation time. As shown in Table I, the small size of the transmission matrix leads to savings in CPU time.

VII. APPLICATION OF TRANSMISSION MATRIX METHOD FOR MULTILAYERED IRREGULAR SHAPED PLANES

The transmission matrix method was next applied to a multilayered irregular shaped plane structure shown in Fig. 10. The aim of this analysis was to demonstrate that the transmission matrix method can be applied to multilayered arbitrary shaped power/ground planes that are typical in a number of applications. The structure consisted of seven layers which were modeled as six power/ground plane pairs using a unit cell size of 5 mm \times 5 mm. Each power/ground plane was connected in parallel using a $1 \mu\Omega$ resistor to mimic vias modeled as short circuits. The positions of the vias were at every 5 mm interval from $x = 5$ cm to $x = 10$ cm and from $y = 5$ cm to $y = 10$ cm using a coordinate system with the origin as defined in Fig. 10. All ground planes were assumed to have the same rectangular shape as the V4 plane. Each plane pair had a different dielectric thickness, as shown in Fig. 10, with relative permittivity $\epsilon_r = 4$ and dielectric loss tangent $\tan(\delta) = 0.02$ at 1 GHz. The conductor planes were made of copper with a thickness of 30 μm . An excitation point (Port 1) was defined at ($x = 5$ cm, $y = 5$ cm) on V4–G3 plane pair and an observation point (Port 2) at ($x =$

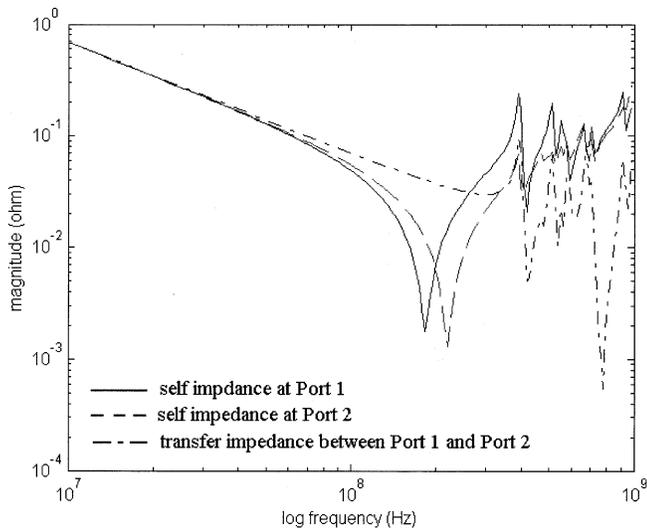
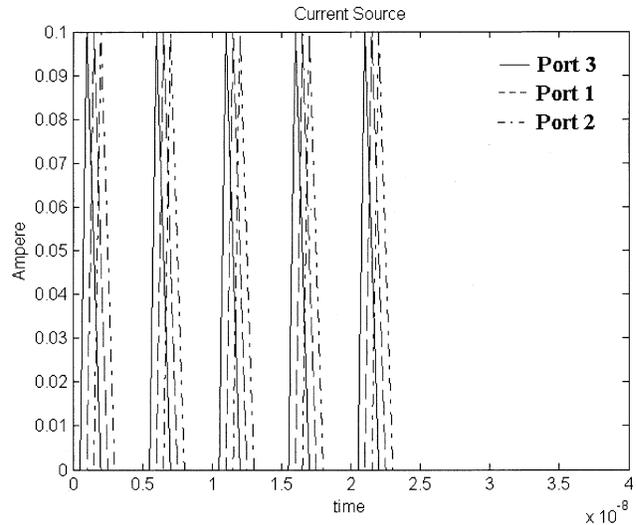


Fig. 11. Impedance of multilayered irregular shaped planes.

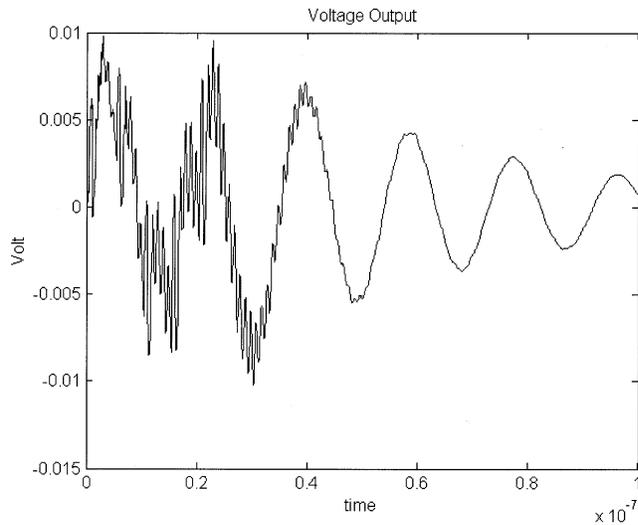
9 cm, $y = 9$ cm) on V1–G1 plane pair. The impedance magnitudes between the two ports are shown Fig. 11. Due to many boundaries in the structure, the resonant frequencies in a multilayered irregular shaped plane structure occur at more frequencies than in a multilayered rectangular plane structure. To understand the resonant behavior of the structure in the time domain, multiple triangular current sources with a period of 5 ns having a rise time of 500 ps and fall time of 1 ns, which are caused by a switching circuit generating 200 MHz voltage clock waveforms, were injected at Port 1, Port 2, and Port 3 defined at ($x = 7.5$ cm, $y = 7.5$ cm) on V4–G3 plane, as shown in Fig. 12(a). The structure was terminated using $1 \text{ m}\Omega$ at ($x = 15$ cm, $y = 0$ cm) between V4–G3 plane. Fig. 12(b) shows the transient response of the multilayered irregular shaped cavity at Port 1. As is typical of a resonant cavity, the multilayered plane structure initially builds up energy generated by each current source until the energy gained equals the energy lost on each cycle, then reaches the steady state, and finally decays to zero due to the losses in the planes after the switch is turned off. In addition to the oscillating waveform, high frequency glitches can be seen in the initial time period due to the switching circuits. The transmission matrix method is ideally suited for analyzing irregular shaped plane geometries, as demonstrated by the results in Fig. 12.

VIII. CONCLUSION

The transmission matrix method has been discussed in this paper for analyzing multilayered rectangular and irregular shaped power/ground planes in the presence of vias. This paper described the physical principle, formulation and implementation of the transmission matrix method for multilayered planes. In addition, via effects and the effects of multilayered power/ground planes both in the frequency and time domain have been studied using the transmission matrix method. This method is computationally more efficient than Spice, which is commonly used for most power delivery system analysis. With linear CPU time and small memory requirements, the transmission matrix method provides the flexibility to analyze a large network containing up to 20 power/ground plane pairs.



(a)



(b)

Fig. 12. Transient response of multilayered irregular shaped planes: (a) current source at ports 1–3 and (b) voltage output at port 1.

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