Failure Mechanisms and Optimum Design for Electroplated Copper Through-Silicon Vias (TSV)

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Abstract

Through-Silicon Vias (TSVs) have garnered a lot of interest in recent years because TSV is a key enabling technology for three dimensional (3D) Integrated Circuit (IC) stacking, silicon interposer technology, and advanced wafer level packaging (WLP). There has been significant effort in TSV fabrication and electrical design. However, considerably less work has been done on thermo-mechanical analysis and mechanical design of these structures. Due to the high coefficient of thermal expansion (CTE) mismatch between Si and the conducting material in the vias, thermo-mechanical reliability is a major concern. This paper uses Finite-Element (FE) models and X-ray diffraction (XRD) experiments for the thermo-mechanical analysis of TSVs. Two-dimensional thermo-mechanical Finite-element models have been built to analyze the stress/strain distribution in the TSV structures, and the models show that large stress gradients and plastic deformation exist near the corner of electroplated Cu pads. The stress results from the finite-element models have been compared against XRD experimental data. A fracture mechanics analysis has also been performed, and the fracture analysis shows that Cu/SiO_2 interfacial cracks and SiO_2 cohesive cracks are more likely to initiate and propagate at those corner locations.

Key words: Through Silicon Via, Finite-Element Modeling, Thermo-mechanical Reliability, XRD measurements

1. Introduction

In recent years, through-silicon vias (TSVs) are being used to fabricate three dimensional vertically stacked devices, where specific components such as logic, memory, sensors, and actuators are fabricated on separate wafers and then interconnected by either wafer-to-wafer or chip-to-wafer methods. Since these devices are vertically interconnected, the effective electrical interconnect path becomes shorter, resulting in reduced signal latency between strata and greater signal bandwidth. In addition to faster electrical signal propagation, reduced power consumption, higher I/Os density, and lower cost can be realized, along with the possible interconnection of hybrid/heterogeneous functional devices.

Tremendous research effort [1-7] has been devoted to the development and improvement of various TSV fabrication process steps. However, relatively less work has addressed the TSV reliability issues. Limited studies have focused on the analysis of thermo-mechanical failure mechanism, and most of these studies have approached this problem empirically. Due to the unique feature of TSV structure and the high mismatch in the coefficient of thermal expansion (CTE) between silicon substrate, dielectric layer material and metal core, large stress may develop, and these stresses may lead to various reliability issues, such as cohesive cracking and/or interfacial delamination. Therefore, there is a compelling need to study TSV reliability through both experiments and numerical models, and thus to develop geometry, material, and processing guidelines that will result in reliable TSV structures. In addition, there is a need for developing computer-based tools that help designers to perform a number of "what-if" simulations to be able to design current and future TSVs with optimum thermo-mechanical performance

In this paper, we present simulation and experimental results from thermal loading of high aspect ratio copper electroplated through-silicon vias (TSVs). Details on TSV fabrication are provided in [1-2]. Due to the significant thermal mismatch between silicon and copper, large thermo-mechanical stresses were generated at the copper-silicon interface. 2-D Finite Element (FE) fracture models of the copper filled TSVs were built and simulations were performed to predict the distribution of thermo-mechanical stress and deformation. X-ray diffraction (XRD) was used to measure stresses. Also, numerical fracture analysis was also carried out in the critical locations where interfacial/cohesive fracture could occur. The effect of different designs, blind-via and through-via, aspect ratios were studied based on the fracture models.

2. Experimental Stress Measurements using XRD

A large array of filled TSVs were subjected to XRD analysis using Cu-Kα as the characteristic XRD source, at different temperatures ranging from 25 ℃ to 425 ℃ in steps of 25 ℃. The analysis was also done in the reverse direction with the temperature going from 425 ℃ to 25 ℃ in steps of -25 ℃. The temperature change leads to strain and stress in the TSV structure. In the X-Ray stress measurement, the strain is detected by a shift in the 2θ peak at the different temperatures of measurement. A monotonic peak shift downwards with increasing temperature was detected for each Cu peak of the XRD spectra. An example of this is shown as Figure 1 for the 2θ=89.933°, which corresponds to the Cu (311) texture.

From the measured 2θ change at different temperatures, we can use the following equation to determine the stress in the TSV.

$$\sigma = \frac{E \cot\theta \Delta 2\theta}{2\nu} \times \frac{\pi}{180}$$

where,

σ : Stress

E : Young's modulus

ν : Poisson ratio

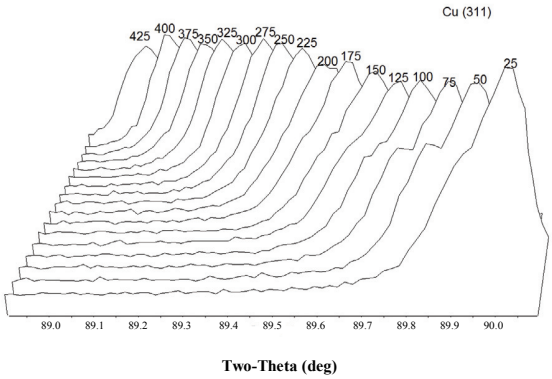


Figure **1:** XRD pattern (near 2θ=89.933°) for Cu at different temperatures

Fig. 2 shows the stress calculated in the TSVs at different temperatures, where the 2θ peak shift is determined relative to the Powder Diffraction File (PDF) for Cu. The 2θ angle for the sample tested in 50 ℃ is nearly the same as the angle of the powder diffraction file and is therefore assumed to be the zero-stress condition. It can be seen that plastic deformation of Cu is occurring at temperatures as low as 100 ℃.

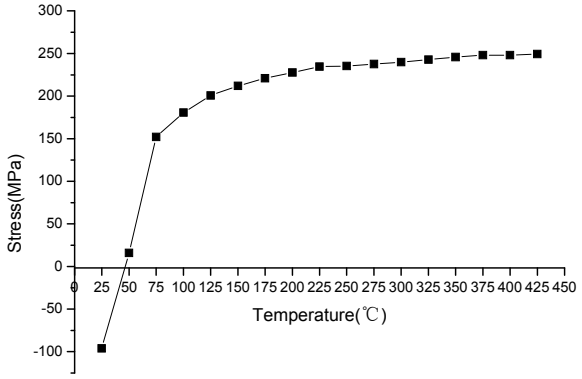


Figure **2:** Stress in TSVs at different temperatures.

XRD measurements were collected as the temperature was increased in steps and also as the temperature was decreased at the same step. No significant hysteresis was observed from these measurements. The spectra at each temperature were mostly indistinguishable in both increasing and decreasing temperature measurements.

This XRD method does not provide a spatial distribution of the stresses on the wafer. It is instead an average measurement of the stresses near the top of the TSV structure. The stresses as determined by this method are preliminary and more measurements will be made to better develop this method and to correlate the numerical predictions with the XRD data.

3. Finite Element Analysis of electroplated copper TSV

Two-dimensional axisymmetric models were adopted for computational efficiency. The geometry of the through-vias and blind-vias in this study are depicted in Fig.3. In both cases, silicon holes were completely filled with copper. The height of Cu via in both cases is 200 μm, and there is a 1 μm thick SiO_2 dielectric layer between the metal core and the Si substrate. The assumptions made in these models are as follows:

1. All vias were modeled as a cylinder with right angle on the top and bottom corners.
2. The stress-free temperature for the TSV structure is taken to be 50℃to mimic XRD measurements.
3. All materials can be assumed to be isotropic for the current study.

The material properties used in the models are listed below in Table 1 and Table 2.

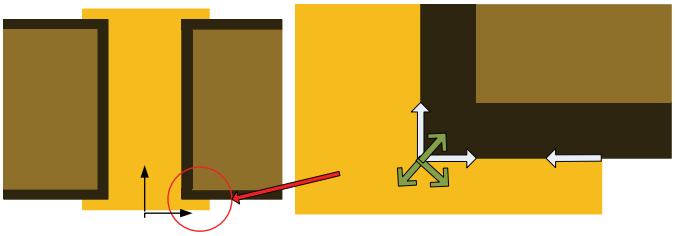


Figure **3:** (a) Through-via

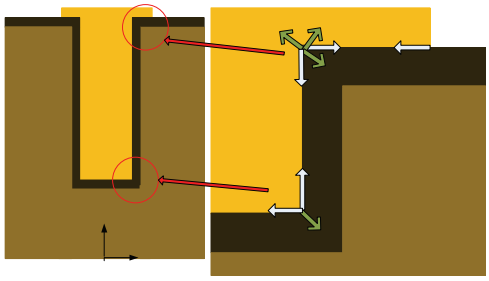


Figure **3:** (b) Blind-via

Table 1: Material properties

	Cu	SiO_2	Si
Young's Modulus (GPa)	Table 2	71.4	130.91
Poison ratio	0.3	0.16	0.28
CTE (ppm/℃)	17.3	0.5	2.6

Table 2: Material properties of Cu

Temperature (℃)	27	38	95
Young's Modulus (GPa)	121.00	120.48	117.88
Temperature (℃)	149	204	260
Young's Modulus (GPa)	115.24	112.64	110.00
Temperature (℃)	27		
Plastic Curve - stress (MPa) vs. strain	121@ 0.001ε 186@ 0.004ε 217@ 0.01ε 234@ 0.02ε 248@ 0.04ε		

As shown in Figure 3, the radial axis is the *x* axis and the vertical axis along the center of the via is the *y* axis. Axisymmetric boundary conditions were applied along the

center of the via, and one node at the bottom was additionally constrained in the vertical direction to prevent rigid body motion. Also, in this study, the right edge of the model was constrained in the radial direction to mimic constraints in actual microsystems. In our ongoing work, we are comparing these results with 3D as well as 2D models with coupled periodic boundary conditions.

3.1. Critical locations in through-vias and blind-vias

To identify critical locations of fracture, a thermo-mechanical analysis was carried out assuming perfect bonding between materials. Starting with a stress-free temperature of 50 ℃, the structure was then heated to 300 ℃.

For the through-via, the distribution of the various stresses components as well as von Mises stress are shown in Figure 4, which indicate that Cu tends to expand more than the surrounding Si. Therefore, the axial stress σ_{yy} for most of the the via is compressive. Similarly, the radial stress σ_{xx} for Cu is mostly compressive. The shear stresses dominate near the corners of Cu/SiO_2 interface.

The via layout is periodic in nature, and one can determine an average magnitude of stress in Cu over a given planar area of the structure. Thus, when the simulated stress results averaged over a given area for a given depth of the sample, it is seen that the simulated stress magnitude is of the same order as measured by the XRD. Such a comparison provides a preliminary experimental validation of the models.

The plot of equivalent plastic strain (Fig.5) indicates that Cu yielding occurs along the Cu/SiO_2 interface near the Cu pad corner.

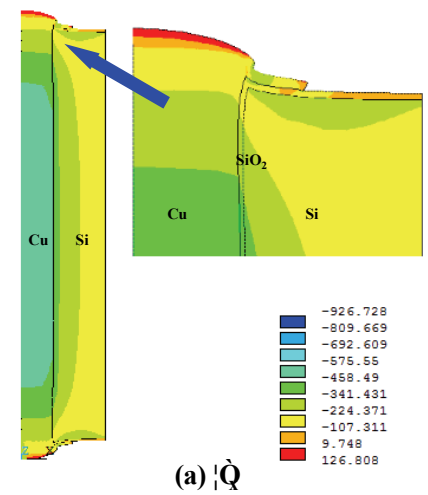
The blind-via has similar stress distribution near the top Cu pad corner as the through-via. In addition, it has another critical location at the bottom corner of the via, as illustrated in Fig. 6 and Fig. 7.

Furthermore, when the blind-vias and through-vias are cooled to -50 ℃, the results also show that those corner locations are highly stressed.

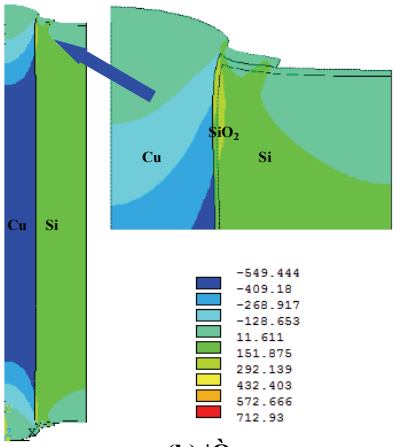
3.2. Fracture Analysis

The stress and strain analysis gives us a general view of possible critical locations. However, a more detail analysis is needed to decide the failure mechanisms and exact failure locations. Because most of the failures in the TSV result from either cohesive or interfacial cracks, fracture analysis is carried out in the locations indicated in Fig. 3. When referring to Fig. 3, the notation *T* represents through-via, while *B* represents blind-via. Also, *C* represents cohesive crack, while *I* represents interfacial crack. Thus, TC-1 represents a cohesive crack number 1 in a through-via.

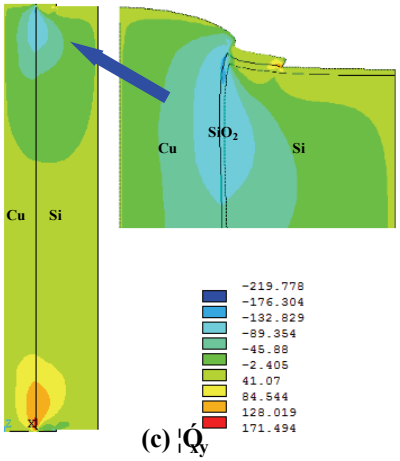
To simplify the analysis, predefined cohesive/interfacial cracks were built in the models, and for each case there was only one crack built into the TSV structure. For the cohesive fracture, cracks were assumed to grow along 45° direction as depicted in Fig.3.



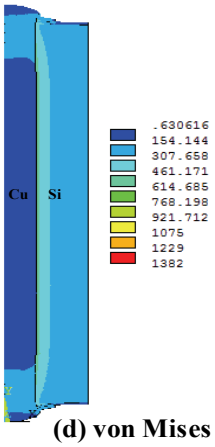
(a) σ_{xx}



(b) σ_{yy}



(c) σ_{xy}



(d) von Mises

Figure **4:** Stresses in through-via at 300℃(deformation scale factor ×50)

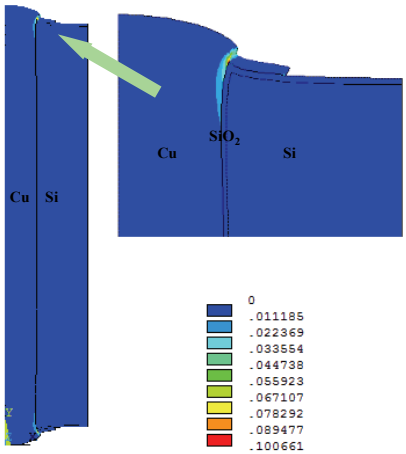


Figure **5:** Equivalent plastic strain in through-via at 300℃ (deformation scale factor ×50)

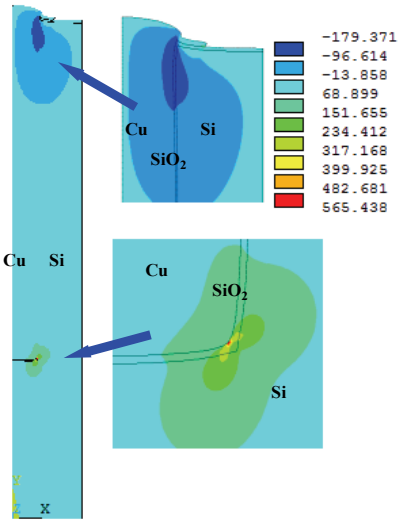


Figure **6:** τ_{xy} in blind-via at 300℃(deformation scale factor ×50)

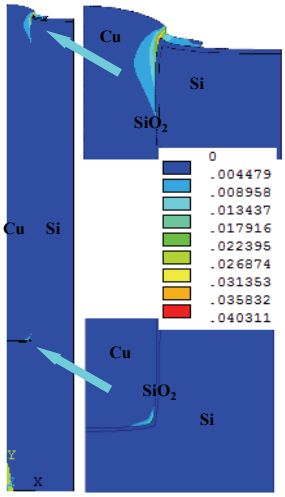


Figure **7:** Equivalent plastic strain near the bottom corner in blind-via at 300℃ (deformation scale factor ×50)

As seen, the models studied cohesive fracture in the Cu pad as well as the dielectric layer. On the other hand, the interfacial cracks were assumed to exist only between Cu and dielectric layer, because of the large CTE mismatch between Cu and the dielectric layer, not at the interface between the dielectric layer and Si. In order to prevent the crack surfaces from penetrating into each other, surface-to-surface contact elements were applied on those crack surfaces.

The energy release rate G was used to compare and decide failure locations and mechanisms. Since loading in the models is due only to thermal expansion with no work performed by external loads, the energy release rate can be determined as the rate of change in strain energy with crack extension. Based on this, two FE models were built for each analysis, one with a crack length of a, and another with a crack length $a+da$. Using a forward finite difference approach, the change in the total strain energy between the two models can be divided by the increase in crack length to approximate G.

For interfacial cracks in both blind-via and through-via, the crack length of 3 μm was used for each case. Limited by the thickness of dielectric layer and Cu pad, which are only 1 μm thick, 0.5 μm cracks were used for cohesive crack models. For these, the models were heated to a temperature of 125℃ and also cooled to a temperature of -50℃. In both cases, the models were assumed to be stress free at 50℃. The G values in all cases are shown in Table 3, which indicates, at the same location, when the neighboring stress field tends to open the crack, the corresponding G is much higher than that of closed ones.

Although the G values for the cohesive cracks in the Cu may be higher than those in dielectric layers, it is unlikely that cohesive failures will occur in the Cu pad first. Because Cu is a ductile material, its critical strain energy release rate (G_c) value is of the order of 10^3 J/m^2 [8] if we assume J_c equals G_c for linear elastic condition, and the G values derived from the FE analysis are far below this critical value. However, for SiO_2, G_c is only about 8.5 J/m^2 [9]. Therefore, cohesive failure for both through-via and blind-via may first initiate

from those dielectric layers. As for blind-via, when temperature is higher than stress-free temperature, dielectric cracking may first initiate from bottom corner (BC-3), however, if temperature is below stress-free temperature, the dielectric layer (BC-4) near the upper Cu pad corner is more likely to break first, because the neighboring stress field tends to open the crack.

The lower bound of the debonding energy of Cu/SiO_2 interface is around 0.7 J/m^2; as mode mixity increases, the value may increase up to 10 J/m^2 [10]. Based on the results presented in Table 3, it is seen that the computed G values at some of the locations are of comparable magnitude to interfacial fracture toughness, and interfacial crack propagation is a probable mode of failure in these locations. As shown in Table 3, for through-vias, the Cu/SiO_2 interface near the Cu pad corner (TI-3) is more critical than that of Cu pad edge. The Cu/SiO_2 interface near the top and bottom corners (BI-2 and BI-5) of blind-vias are also prone to debond as well as the interface below Cu (BI-1) at -50℃.

Table 3: G value of cohesive/interfacial crack in through-via and blind-via

			125℃		-50℃	
			G (J/m2)	**Open/Close crack**	**G (J/m2)**	**Open/Close crack**
Through-via	**Cohesive**	Cu Pad Left (TC-1)	0.00822	Close	0.25760	Open
		Cu Pad Right (TC-2)	0.05077	Close	0.10011	Open
		Dielectric (TC-3)	0.02699	Close	0.19531	Open
	Interfacial	Cu Pad Corner (TI-1)	0.00876	Open	0.00052	Close
		Cu Pad Edge (TI-2)	0.14578	Close	0.18786	Open
		Side Crack (TI-3)	0.31721	Close	3.00131	Open
Blind-via	**Cohesive**	Cu Pad Left (BC-1)	0.00824	Close	0.28185	Open
		Cu Pad Right (BC-2)	0.06599	Close	0.09785	Open
		Dielectric Bottom (BC-3)	0.14696	Open	0.01684	Close
		Dielectric Top (BC-4)	0.02639	Close	0.19428	Open
	Interfacial	Bottom Horizontal (BI-1)	0.42331	Close	1.64372	Open
		Bottom Side(BI-2)	0.69741	Close	2.30492	Open
		Cu Pad Edge(BI-3)	0.14172	Close	0.18462	Open
		Top Horizontal(BI-4)	0.02225	Open	0.00090	Close
		Top Side(BI-5)	0.41762	Close	1.55588	Open

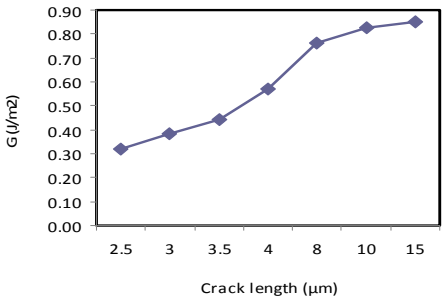


Figure 8: Crack length vs. G value for TI-3 in through-via

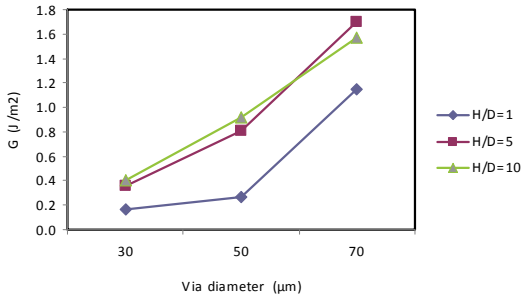


Figure 9: Effect of aspect ratio on G value for TI-3 in through-via

3.3. Factors that affect *G*

Those critical locations found in the above fracture analyses correlate well with the results from previous stress/strain analysis. It is necessary to examine whether those cracks are under slow stable crack growth or unstable fracture process. Let us consider Cu/SiO_2 interface near the Cu pad corner (TI-3) of the through-vias. As seen in Fig.8, at 125℃ G increases with longer crack. This means that for a given crack length, if G is initially smaller than G_c, then crack would arrest, once G reaches G_c, unstable crack growth will occur. Other critical interfaces also present a similar trend.

The effect of via aspect ratio (height to diameter ratio; H/D) on G was also studied by considering the Cu/SiO_2 interface near the Cu pad corner (TI-3) with a crack length 3 μm in the through-via. As Fig.9 shows, G increases with larger via-diameters when aspect ratio is fixed. And as aspect ratio increases, G generally increases. However, for higher aspect ratios and under perfect processing conditions with no voids or defects, G may be leveling off with the increase in the aspect ratio.

4. Summary

Stress/strain analysis shows that high stress concentration exists at Cu pad corners of through-vias and blind-vias, resulting in plastic deformation of Cu. For blind-via, the Cu

via bottom corner has high stress that can result in plastic deformation of Cu. The stress results from the models are of the same order as seen in preliminary XRD experimental data. Additional experiments are planned to further enhance the models and findings. The fracture analysis not only confirms those critical locations, but also shows that the failure mechanisms will be the interfacial delamination at the Cu/SiO_2 interface as well as the cohesive cracking of dielectric layers. Furthermore, FE analysis shows that as the interfacial crack grows, the energy release rate will increase resulting in unstable crack growth at the critical corner locations. Generally, the energy release rate increases with larger diameter and higher aspect ratio.

Acknowledgments

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