INVITED PAPER

3-D Hyperintegration and Packaging Technologies for Micro-Nano Systems

These technologies stack and interconnect materials and components to achieve high density, small size, low weight, reduced power, and very low cost.

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ABSTRACT | Three-dimensional (3-D) hyperintegration is an emerging technology, which vertically stacks and interconnects multiple materials, technologies, and functional components to form highly integrated micro-nano systems. This 3-D hyperintegration is expected to lead to an industry paradigm shift due to its tremendous benefits. Worldwide academic and industrial research activities currently focus on technology innovations, simulation and design, and product prototypes. Anticipated applications start with memory, handheld devices, and high-performance computers and extend to high-density multifunctional heterogeneous integration of InfoTech-NanoTech-BioTech systems. This paper overviews the 3-D hyperintegration and packaging technologies, including motivations, key technology platforms, status, and perspectives towards commercialization. The challenges associated with the 3-D technologies are addressed, including integration architectures and design tools, yield and cost, thermal and mechanical constraints, and manufacturing infrastructure.

KEYWORDS | Hyperintegration; InfoTech-NanoTech-BioTech systems; three-dimensional (3-D) integration; through silicon via; wafer alignment; wafer bonding; 3-D packaging

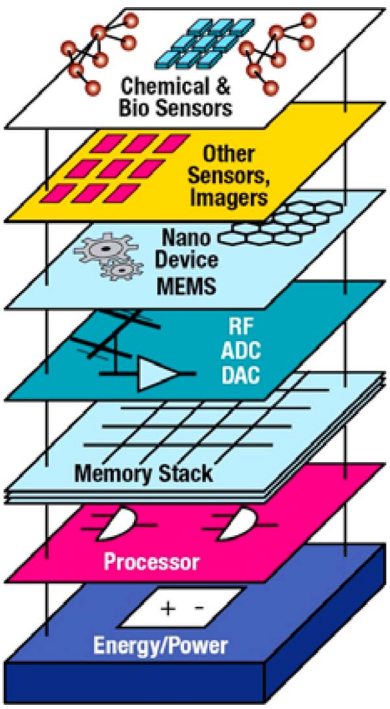

Fig. 1. *A vision of future 3-D hyperintegration of InfoTech, NanoTech, and BioTech systems—a new paradigm for future technologies.*

I. INTRODUCTION

Three-dimensional (3-D) hyperintegration is an emerging technology that can form highly integrated systems by vertically stacking and connecting various materials, technologies, and functional components together, as shown in Fig. 1 [1]. The potential benefits of 3-D integration can vary depending on approach; they include multifunctionality, increased performance, increased data bandwidth, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration, and reduced overall costs. For example, a small form factor is achieved by stacking active component layers on top of one another in any 3-D approach. Since simple complementary

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metal–oxide–semiconductor (CMOS) device scaling has stalled, this third dimension allows extending Moore's law to ever higher density, higher functionality, higher performance, and more diversified materials and devices to be integrated with lower cost. Speaking at the 2006 IEEE International Electron Devices Meeting (IEDM), Dr. C.-G. Hwang, president and CEO of Samsung Electronics, stated that "rapid adoption of 3-D integration technology seems to be essential and, thankfully, unavoidable." [2] It is expected that the industry paradigm will shift to a new industry-fusing technology era that will offer tremendous global opportunities for expanded use of 3-D silicon-based technologies in highly integrated systems. Indeed, 3-D integration is recognized as an enabling technology for future ICs and low-cost micro/nano/electroopto/bio heterogeneous systems.

This paper attempts to provide an overview of the 3-D hyperintegration and packaging technologies, to discuss their benefits and applications, and to address key challenges associated with the 3-D technologies. The author believes that many unique system architectures will be realized with 3-D integration and hopes that this paper motivates IC system architect designers to extend their horizons to 3-D hyperintegration.

II. 3-D INTEGRATION APPROACHES

Various 3-D technologies are currently pursued, as illustrated in Fig. 2. They can be divided into three categories based on their similarity to other technologies:

1) 3-D packaging technology [Fig. 2(a)–(c)];
2) transistor build-up 3-D technology [Fig. 2(d)–(f)];
3) monolithic, wafer-level, back end of the line (BEOL)-compatible 3-D technology [Fig. 2(g)–(k)].

Each 3-D technology is briefly described below, with possible application examples showing the worldwide research and development activities.

A. Packaging-Based 3-D Integration

Packaging-based 3-D integration, i.e., the stacked chip-scale package (CSP) as called historically, is enabled by wire bonding and flip-chip bonding as depicted in Fig. 2(a). These include system-in-package (SiP), which is formed by stacking thinned chips with wire bonding to connect them, and package-on-package (PoP), which is formed by stacking packages such as SiPs with flip-chip bonding. These SiPs or PoPs are already commercially available products, particularly widely used in cell phones [3], [4], [91]. Today's new cell phones have at least one SiP or PoP, while more than a billion cell phones were delivered in 2006.

B. Die-to-Die 3-D Integration

Die-to-die 3-D integration is enabled by thinned die-to-die bonding and through silicon via (TSV) interconnections, as depicted in Fig. 2(b). The TSVs are typically formed by laser drilling, such as a prototype eight-die memory stack by Samsung [5] or deep reactive ion etching (DRIE), such as a Bosch process [6], [7], followed by liner deposition and copper fill.

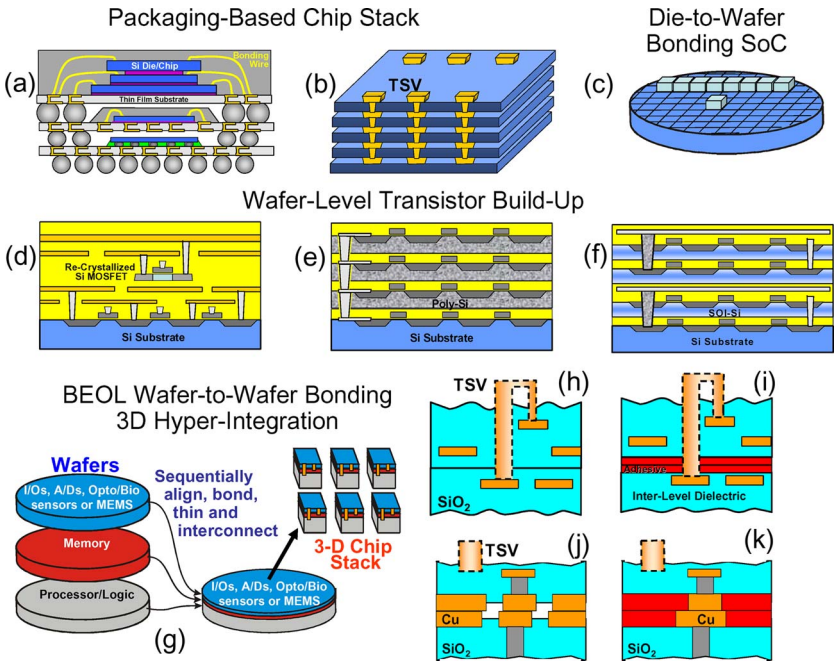


Fig. 2. *Schematic representations of major 3-D integration approaches: (a)–(c) 3-D packaging technology, (d)–(f) wafer-level transistor buildup 3-D technology, and (g)–(k) wafer-level BEOL-compatible 3-D technology.*

C. Die-to-Wafer 3-D Integration

Die-to-wafer 3-D integration as depicted in Fig. 2(c) is enabled by die-to-wafer bonding, with interchip electrical interconnections formed by postbond via formation [8] or solder (or eutectic) bonding during the die bonding process [9]. This approach uses techniques from both packaging and wafer fabrication, such as die pick-and-place and TSV formation, respectively. A system-on-chip (SoC), which is difficult to be fabricated with two-dimensional (2-D) integration, may be realized with several smaller chips stacking on a large chip [8].

D. Transistors Formed Inside On-Chip Interconnect

The approach to form transistors inside on-chip interconnect layers on a piece of recrystallized silicon film is depicted in Fig. 2(d). A small piece of amorphous silicon film is deposited with a catalyst followed by either laser heating or rapid thermal anneal to recrystallize the silicon [10], [92]. The transistors are then formed by BEOL compatible processing. These transistors may be used to form repeaters for on-chip interconnects or signal amplifiers for optical interconnects.

E. Transistors Formed on Polysilicon Films

The approach to form transistors on polysilicon films layer by layer with tungsten interlayer vias is depicted in Fig. 2(e). After the first layer of transistors is completed, an amorphous silicon film is deposited and converted to polysilicon by laser heating or rapid thermal anneal [11]. The tungsten via can tolerate the relatively high temperatures ($\sim$600 °C) needed for polysilicon conversion and transistor formation. These transistors may be used to fabricate low-performance nonvolatile memory [11].

F. Transistors Formed on Single-Crystal Silicon Films

The approach to form transistors on single-crystal silicon films layer by layer is depicted in Fig. 2(f). The silicon layer can be bonded onto the oxide surface of a previously fabricated transistor layer by transferring the crystal silicon film from a silicon-on-insulator (SoI) wafer. The interstrata via is filled with polysilicon and/or tungsten, enabling device fabrication at relatively high temperature. Very high-density SRAMs and NANDs are demonstrated with this approach [2], [12], [13].

G. Wafer-Level BEOL-Compatible 3-D Hyperintegration

Monolithic wafer-level BEOL-compatible 3-D hyperintegration is enabled by wafer alignment, bonding, thinning, and interwafer interconnections, as depicted in Fig. 2(g)–(k). All approaches shown use TSVs to form the interwafer interconnects (i.e., interstrata interconnects, interwafer vias, or interstrata vias). They differ as to when the via is formed, before/during bonding (via first) or after bonding (via last). In addition, a variety of bond layer types can be chosen. Four major bonding and interstrata interconnection approaches are highlighted in Fig. 2(h)–(k):

- via last, oxide-to-oxide bonding [Fig. 2(h)];
- via last, adhesive (polymer) bonding [Fig. 2(i)];
- via first, copper-to-copper bonding [Fig. 2(j)];
- via first, bonding of damascene-patterned metal/adhesive redistribution layer [Fig. 2(k)].

Academic and industrial organizations are actively developing a variety of wafer-level 3-D technologies [14]–[39]. Many organizations are currently evaluating competing wafer-level 3-D technologies [2], [14], [23], [24], [26], [31], [36], [37].

There are also other approaches not shown in Fig. 2, such as forming the TSVs during the front end of the line (FEOL) processing [29], stacking chips with metallization on the stack lateral side [40], stacking chips on silicon carrier with TSVs [41], or combining various approaches.

Wafer-level BEOL-compatible 3-D hyperintegration is perhaps the most promising 3-D integration for high-volume production of highly integrated micro-nano systems. More details of these wafer-level 3-D platforms and their key enabling unit processes are discussed in the next section.

III. WAFER-LEVEL BEOL-COMPATIBLE 3-D HYPERINTEGRATION

Wafer-level BEOL-compatible 3-D hyperintegration can be categorized into two platforms, i.e., via-last and via-first 3-D platforms, as illustrated in Figs. 3 and 4, respectively.

For the via-last 3-D platform as shown in Fig. 3, the interstrata vias are formed after the wafers are aligned and bonded, and the top wafer backside is thinned. Since these vias are usually formed through a silicon layer, they are also called through silicon vias. The TSV usually consists of an electrical isolation layer (e.g., SiO_2 or other dielectrics), liner or barrier layer (e.g., titanium, tantalum, TiN, or TaN), and a via metal (e.g., copper, tungsten, or highly doped polysilicon). The wafers can be attached by either adhesive-to-adhesive bonding [15], [18] or oxide-to-oxide bonding [24], [26].

For the via-first 3-D platform as shown in Fig. 4, the majority of interstrata vias can be formed during the wafer bonding process (right after wafer alignment) but before the top wafer backside is thinned. To differentiate TSVs, thus bonded interstrata vias can be called "bond vias." For some cases, wafers are bonded only by these bond vias. Similar to the TSV, the bond via also consists of an electrical isolation layer, a liner or barrier layer, and a via metal, while the candidates for the via metal can be elemental metals (e.g., copper, gold), eutectic conductors, or solders (e.g., InAu, CuSn). Besides the metal bonding that forms the interstrata interconnects (bond vias), the bonding interface can include adhesive-to-adhesive bonding (such a platform is called a metal/adhesive via-first 3-D platform [16], [17]), oxide-to-oxide bonding (such a

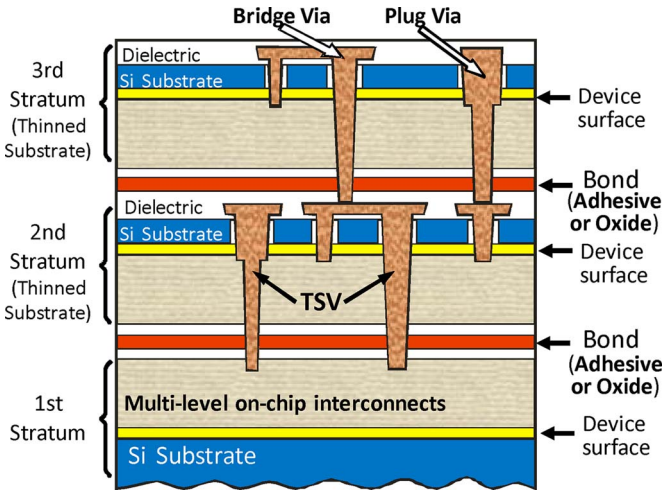


Fig. 3. *Schematic cross-section of three-stratum stack of via-last 3-D platform, showing bonding interface and vertical interstrata vias (TSVs). The bonding interface can be either adhesive-to-adhesive bonding [15], [18] or oxide-to-oxide bonding [24], [26].*

platform is called a direct bonded interconnect [42]), or leaving an air gap by recessing the dielectrics surrounding the metal bonding posts [23], [29].

For wafer-level BEOL-compatible 3-D platforms, only four key enabling unit processes are required, as discussed below.

1) Wafer-to-Wafer Alignment: A wafer-level alignment accuracy of one micrometer or smaller has been achieved, which is sufficient for most applications. Wafer alignment tools were developed for microelectromechanical systems (MEMS). New wafer alignment tools have been further developed for wafer-level 3-D integration [21], including infrared (IR) aligner (limited to IR transparent wafers) [26] and SmartView aligner for aligning wafers face-to-face or face-to-back [22], [43]–[45]. Mechanical interlock structures have also been demonstrated for fine alignment [46].

2) Wafer-to-Wafer Bonding: A bonding temperature compatible with BEOL processing (e.g., $\leq 400\,^{\circ}\mathrm{C}$) and a bonding interface thickness of one micrometer or smaller have been achieved. Wafer bonding was also developed initially for MEMS. It has been greatly researched for BEOL-compatibility and wafer-scale void-free bonding, which limit the wafer bonding to low temperature and use of nonoutgassing materials as the bonding intermediate

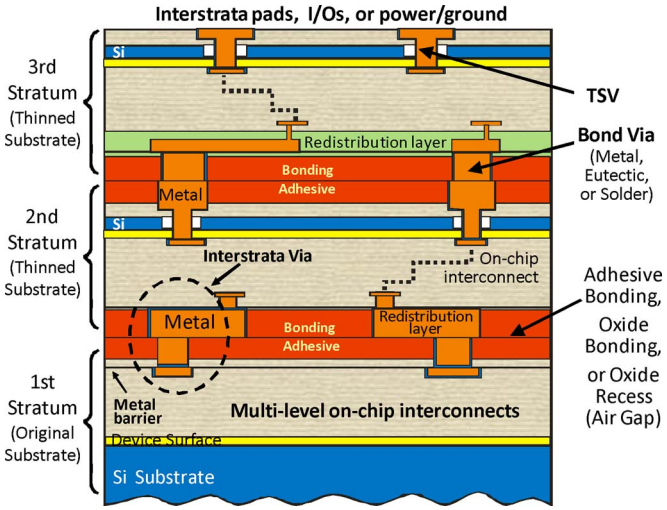


Fig. 4. *Schematic cross-section of three-stratum stack of via-first 3-D platform, showing bonding interface and vertical interstrata vias (bond vias and TSVs). Besides the metal bonding that forms the interstrata interconnects, the bonding interface can include an adhesive-to-adhesive bonding [16], [17] or oxide-to-oxide bonding [42], or leave an air gap by recessing the dielectrics surrounding the metal bonding posts [23], [29].*

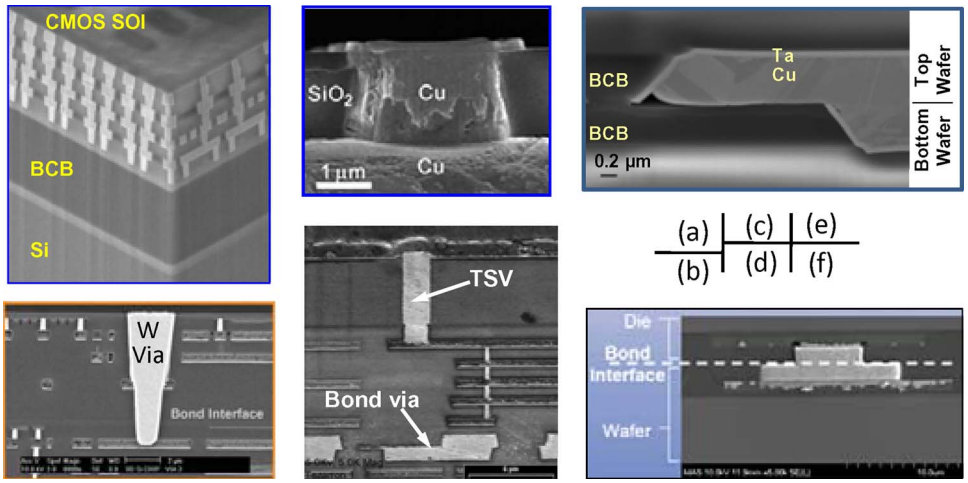


Fig. 5. *Representative bonding interfaces with images adapted from the literature: (a) adhesive (BCB) bonding of an SoI CMOS wafer on an Si wafer with the electrical characteristics of CMOS devices and circuits unaffected [15], [19]; (b) PECVD oxide bonding with tungsten (W) via shown for advanced focal planes [26]; (c) Cu interconnect bonded to Cu pad showing a high-quality bonding interface [23]; (d) Cu bonding for bond vias with "supercontact" TSV shown [29]; (e) bonding of damascene patterned Cu/BCB redistribution layers for metal/adhesive via-first 3-D platform [16]; and (f) bonding of metal/oxide layers using direct oxide bond for a direct bonded interconnect (DBI) 3-D approach (the information about the metal material was not released) [42].*

materials, such as nonoutgassing adhesives [21], [25], [32], [43], [45], [47]–[49], plasma-enhanced chemical vapor deposition (PECVD) oxide [24], [26], and few metals (e.g., copper [23], [27]–[31], titanium [50], [51], InAu [33], and CuSn [52]). Fig. 5 shows cross-sectional images of representative wafer bonding interfaces. Table 1 lists four key wafer bonding approaches demonstrated so far and key parameters differentiating their advantages and challenges for high-volume manufacturing.

3) Wafer Thinning: A range of submicrometer to 100 μm with adequate uniformity has been achieved. One wafer thinning approach is to use an etch-stop, i.e., the top wafer backside is thinned by backside grinding, optional chemical-mechanical polishing (CMP), and selective wet-etching to an etch stop, e.g., an ion implanted layer, a graded SiGe epitaxial layer, or a buried oxide (BOX) layer with SoI wafers. An excellent control of the thinning uniformity and thickness (down to a few tens of nanometers) can be achieved [15], [18]–[20], [26]. Another approach is a thickness-control removal of silicon, which is used for bulk wafers without an etch-stop. It is therefore expected that the thinned wafer is relatively thick (e.g., in a range of a few tens or hundreds of micrometers) with limited thickness uniformity (in a range of a few to few tens of micrometers) [36], [43], [45], [53]. Other approaches are also demonstrated with TSVs as a thinning stopper, where the TSVs are formed either during the FEOL process [29] or after the BEOL process but right before wafer alignment and bonding [36], [53]. If the wafers are bonded back-to-face (i.e., back of the top wafer is bonded onto the face of the bottom wafer or wafer

Table 1 Key Bonding Approaches for Wafer-Level 3-D Technologies*

Key Parameters \ Bonding Approach	Oxide Via-Last	Adhesive Via-Last	Copper Via-First	Copper/ Adhesive
Bonding Temperature	Fair	Low	High	High
Surface Planarity	Strict	Loose	Strict	Strict
Bond Strength	Good	High	Good	Good
Bond Integrity	Fair	High	Good	High
Via Density	Low	Low	High	High
Thermal Management	Fair	Fair	Good	Best
Complexity	High	Fair	Fair	High

**Color codes*: green (light dark) for most desirable to manufacturing; yellow (light) for adequate; and red (dark) for concerns.

stack), a handling wafer (or temporary carrier wafer) is needed to provide the mechanical support during thinning and handling of the thinned wafer [36], [53].

4) Interwafer Interconnection: A via diameter in a range of a few micrometers with high via height-to-diameter aspect ratio has been achieved. Both TSVs and bond vias can be formed by via etching and clean, liner deposition, metal fill, and CMP—similar to a BEOL damascene patterning process developed for on-chip copper interconnects. Actually, the bond vias have been formed using the BEOL damascene patterning process as shown in Fig. 5(c) to (e) [16], [23], [29]. The TSVs have been formed 1) before or during the FEOL process using polysilicon [33] or tungsten [29] as the via filling material; 2) after the FEOL or BEOL process using copper as the via filling material with/without a carrier wafer for wafer thinning [29], [36], [53]; or 3) after wafer bonding and thinning [15], [26], as shown in Fig. 5(b). Since the TSVs usually pass through the thinned silicon wafer and/or on-chip interconnects, their diameter and height-to-diameter aspect ratio are usually much larger than the bond vias. Hence the TSV density is relatively lower than that of bond vias because of the limitations associated with the current TSV processing technologies, TSV resistance, and silicon real estate consumption of the TSVs.

Feasibility for all these four key processes has been demonstrated. No technology show-stoppers are expected. Technology variations are being investigated for prototyping and commercialization, including:

- face-to-face or face-to-back alignment and bonding;
- with or without handling wafers (carrier wafers);
- with or without etch-stop for wafer thinning;
- when and how to form the interstrata vias.

Based on the 3-D technology developments so far, it is clear that the key advantage of the via-last 3-D approach is that the wafer bonding process is separated from interstrata via formation. Therefore, a robust mechanical/chemical wafer bond, for instance, using benzocyclobutene (BCB) as shown in Fig. 5(a) [15], [18]–[20], can be easily achieved compared to the via-first 3-D approach. The key concern for the via-last 3-D approach is that the TSV density could be low because of the large via diameter required for long TSVs to pass through the thinned silicon substrate, particularly if a bulk silicon wafer is used. If an SoI wafer is used for the top wafer, a high density of short TSVs can also be achieved using BEOL damascene patterning process through the BOX/SoI layer because the bulk silicon substrate of the SOI wafer can be completely removed, leaving only the BOX/SoI layer with a thickness of a few ten to a few hundred nanometers [19], [20], [26]. In fact, these TSVs are formed through the SiO_2 layer surrounding the SoI CMOS device islands; there is no silicon layer for TSVs to go through. Therefore, the term "TSVs" could be used more generically for "through strata vias."

The key advantages of the via-first 3-D approach are that 1) a high density of bond vias can be formed at the bonding interface and 2) the formation of bond vias and wafer bonding are done in one unit process. Particularly, as shown in Fig. 4, the metal/adhesive via-first 3-D platform offers combined process integration advantages of metal-to-metal electrical bonding (e.g., Cu-to-Cu) with the increased adhesion strength and robustness of dielectric adhesive bonding (e.g., using partially cured BCB) [16], [17], [54]. A redistribution layer formed by damascene-patterned metal/adhesive structure provides additional interstrata signal/power routing as well as alleviation of the wafer alignment tolerance [54]. Planarity requirements are stringent but appear to be reasonable [17]. However, if the top wafers are bulk silicon wafers, the density of TSVs, which interconnect the bonded wafers (i.e., the top strata) and bring the I/Os out of the stack, is as limited as that with the via-last 3-D platform. Similar to the via-last 3-D platform, SoI wafer is a better choice as the top wafer in the 3-D stack because its bulk silicon substrate can be removed with BOX as the etch stop; short TSVs can be formed using BEOL damascene patterning process as for bond vias.

Though the use of SoI wafers obviously makes the wafer thinning and TSV formation much easier, and hence low cost, the choice to use SoI or bulk silicon wafer depends on overall processing protocols, components [Si CMOS logic, SRAM, DRAM, NAND, SiGe, radio frequency (RF), etc.] in the system, and the IC manufacturer's preferences. Further research and development is necessary to fully evaluate these promising platforms.

IV. TECHNOLOGY COMPARISON AND APPLICATIONS

With the significant research progress in 3-D technologies thus far, it is still too early to do a full comparison among various 3-D technologies. We attempt to briefly discuss the key advantages and limitations of different 3-D technologies and their potential applications, as summarized in Table 2. In general, all 3-D technologies would offer *high density* component integration with:

- small form factor (small size and light weight);
- reduced packaging;
- reduced power (fewer I/Os to be driven).

For 3-D packaging technologies [Fig. 2(a)–(c)], using known good die (KGD) can provide a yield advantage. Time-to-market for a new product is short because the flexibility in the assembly process requires less design effort for a new system. However, the cost for high-volume production can be very high because of the testing required for KGDs and the low throughput of pick-and-place assembly. The SiP and PoP approaches [Fig. 2(a)] are already used in portable devices (e.g., cell phones) [3], [4]. The die-stack approach with TSVs [Fig. 2(b)] has been demonstrated for memory stacks [5]. The die-wafer approach [Fig. 2(c)] has the potential for building 3-D SoCs [8].

Table 2 3-D Technologies and Potential Applications

Technology	Key Advantages / Key Concerns	Key Applications
3D Packaging	KGDs; Heterogeneous integration / Low throughput for high volume production	Memory stack; memory stack to microprocessor; discrete device integrated with ICs
Transistor Build-Up 3D Technology	Wafer-level lithography and processing / Thermal and material constraints	Highest density memory; low performance CMOSs
Wafer-Level BEOL-Compatible 3D Technology	Massive, short interstrata via; Heterogeneous integration; Low cost for high volume production / Design and technology complexity	Any highly integrated systems requiring high performance, high data bandwidth and low power, e.g., memory, memory-intensive processors, imagers, mixed signal and wireless communication

Transistor buildup 3-D technology [Fig. 2(d)–(f)] can achieve the highest density of silicon transistors with wafer-level fabrication using advanced photolithography. Wafer-level processing can also reduce costs for high-volume production. However, the processing constraints (particularly the thermal budget) affect the properties of the transistors and limit the material choices mostly to silicon and tungsten. The silicon recrystallization approach [Fig. 2(d)] could be used for fabrication of repeaters within on-chip interconnect to alleviate interconnect delay [10], [92]. The poly-Si layer approach [Fig. 2(e)] is used for low-performance memory [11]. The bonded crystalline silicon approach [Fig. 2(f)] can be used for a NAND flash memory stack [2], [13]. Companies, such as Samsung, that manufacture cell phones and handhelds see great potential for a high-density memory stack [2].

For wafer-level BEOL-compatible 3-D technology [Fig. 2(g)–(k)], the electrical, RF, optical, thermal, and mechanical behavior can be considered for each component separately. For example, the starting yield can be improved by fabricating logic and memory on separate wafers with optimized materials and process technologies. The separate wafers are then stacked using a monolithic wafer-level BEOL-compatible process for all components, potentially improving the cost and overall system yield at high-volume production. Typically the bottom wafer retains its full thickness and serves as a mechanical support for the stack. Each subsequent wafer is then thinned to micrometer scale after stacking (bonding); thus the overall stack thickness is close to that of a single wafer and can be processed and packaged with current wafer technologies. Massive (millions), short (micrometer-scale) interstrata interconnects (vias) provide extremely high data bandwidth and dramatically decrease interconnect delay and power consumption.

Wafer-level BEOL-compatible 3-D hyperintegration is perhaps the most attractive 3-D technology due to its flexibility for monolithic heterogeneous integration of different materials, processing technologies, and functional components with additional benefits in cost and performance. Many research groups are exploring its potential applications, such as improving interconnect delay [55]–[60], [93], memory stacks [29], [59], [61], memory-processor or logic–logic stacks [29], [62]–[65], signal-processing circuits [66], [67], field-programmable gate arrays (FPGAs) [68], [69], imagers [26], [70], mixed-signal and RF [70]–[72], and 3-D power delivery [73], [74]. Design and simulation tools have been demonstrated, such as for electronic computer-aided design (ECAD) tools [55]–[69], [93], [75]–[80], switching energy, and thermal and mechanical simulations [59], [60], [65], [79]–[81].

V. KEY CHALLENGES ASSOCIATED WITH 3-D INTEGRATION

Present FEOL device technologies, such as strained layers, high-k gate dielectrics, metallic gates, and wrap-around gate structures, are resulting in enhanced digital CMOS devices at the 45 and 32 nm technology nodes. By the 22 nm node, these FEOL enhancements will result in another interconnect bottleneck with Cu damascene patterning and low-k interlevel dielectrics. Wafer-level 3-D is perhaps the only viable near-term alternative to planar ICs with Cu/lowest-k interconnects, as well as enabling heterogeneous integration of different planar technologies for innovative SoCs. The technology and infrastructure challenges that must be overcome before or soon after a decision to move to large-volume manufacturing are discussed in this section, which are split into technological challenges, yield, test and cost challenges, thermal and power challenges, and infrastructure challenges.

A. Technological Challenges

The three major 3-D technologies (i.e., chip-stack, transistor buildup, and wafer-level stack) will perhaps coexist for a long time, while the chip-stack technology is

relatively mature (though its limitation is also clear). Technological challenges include development of cost-effective manufacturable 3-D processes and evaluation/selection of various 3-D platforms for a given application or system. Recent processing developments focus on TSVs because they can be used for both wafer-level 3-D integration and packaging-based 3-D integration [38]. Table 3 lists the need for all the processing technologies and the need for equipment, which is discussed in the infrastructure section.

For wafer-level 3-D integration, there are a number of technological choices, as discussed in Section III. The feasibility of the wafer-level 3-D unit processes, i.e., alignment, bonding, thinning, and interstrata interconnection, have been demonstrated, as summarized below [22]–[39], [42]–[54]:

- wafer-to-wafer alignment accuracy: ~1 μm;
- wafer bonding interfaces: adhesive (e.g., BCB), oxide, metal (e.g., Cu), and combinations (Cu/BCB);
- wafer bonding thickness: ~1 μm at $T \leq 400\,^{\circ}C$;
- wafer thinning (remaining silicon thickness): ~0.1 μm for SoI wafer, ~15 μm for bulk Si wafer;
- interstrata interconnects (vias): 2–10 μm in diameter.

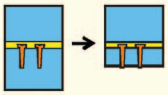
Wafer bonding determines the 3-D integration integrity, while the alignment accuracy, wafer thinning, and interstrata interconnect formation determine the interstrata interconnect length and density, and hence the interconnect delay reduction (system performance) and data bandwidth. All these unit processes require further research and development before 3-D technology is mature enough for high-volume manufacturing.

B. Yield, Test, and Cost Challenges

Yield is related to test; yield, test, and throughput drive the cost. 3-D yield and test are certainly a concern; that is why 3-D packaging by wire-bonding KGDs first found its applications in the handheld devices (e.g., memory stacks for cell phones). However, planar (2-D) memories already use redundancies and error-correcting codes (ECCs) to minimize the effects of yield loss [82], [83]; the question of KGD has already been answered for existing memory chips. Moreover, redundant processor cores are also implemented to increase 2-D system yield; for instance, the Sony Playstation 3 requires only seven of eight cores to work in its IBM CELL multiprocessor [84], [85]. Furthermore, current 2-D SoCs, such as Intel's dual-core multithreaded Xeon processor [82], use not only redundancies and ECC for memory but also design-for-testability (DFT), built-in self-test (BIST), and scan and observability registers to accelerate the yield learning processes and to produce KGDs from imperfect chips. Three-dimensional integration will benefit from redundancy, ECC, DFT, BIST, and defect/fault tolerant designs in overcoming the challenges in its yield, test, and cost while providing a more flexible platform for novel implementation of the yield enhancements; for instance, a stratum of phase-change nonvolatile memory (PCNVM, or PCM) could be used to effectively repair faulty chips.

While die yield and test issues need to be considered further, smaller die and wafer-specific processing indicate that yield may not be a limiting factor with a robust monolithic wafer-level 3-D process. Actually, 3-D integration inherently improves the yield since heterogeneous structures (analog circuits, processors, and various types of memory) can be fabricated on separate wafers with differing fabrication procedures and materials optimized for that technology. This would be impossible in 2-D for the same system. Moreover, monolithic wafer-level approaches have many performance advantages, such as a very high density of low parasitic interstrata interconnects

Table 3 Key 3-D Technologies and Equipment Needs*

Alignment and Bonding		Via Etching	Via Filling	Wafer Thinning
				
C2C	W2W			
Unit Processing Technologies				
Adhesive, oxide or metal bonding Chip alignment	Adhesive, oxide or metal bonding Wafer alignment	Laser drilling or DRIE	ECD or CVD, and PVD	Mechanical grinding, CMP, Wet etching, Plasma etching
Equipment Needs				
Chip aligner and bonder	Wafer aligner Wafer bonder	Laser drill or DRIE Photolitho	Metal deposition, CMP Photolitho	Precise thinning Temporary bonding

Abbreviations: C2C for chip-to-chip (or die-to-wafer) stack; W2W for wafer-to-wafer stack; DRIE for deep reactive ion etching; ECD for electrochemical deposition (electroplating); CVD for chemical vapor deposition; PVD for physical vapor deposition; CMP for chemical-mechanical planarization (polishing); and Photolitho for photolithography.

for high bandwidth and increased noise immunity. Most important, lower cost for high-volume interconnects should be possible with monolithic wafer-level processes, compared to 3-D KGD packaging. The chip-on-wafer approach can be used to salvage particularly bad wafers.

In particular, effective 3-D implementation would benefit from the development of a mature BIST wafer-probe technology because 1) it provides at-speed testing, with a minimum number of probes per chip; 2) it allows all chips on a wafer to be tested simultaneously; and 3) it provides the thorough testing needed for rapid yield learning and/or imperfect chip repair. While wafer-level test and repair for each stratum are important similar to processing monitors in 2-D implementations, critical test and repair will be conducted after 3-D wafer processing, dicing, and packaging just as the critical test and repair in 2-D implementations are conducted after chip packaging.

C. Thermal and Power Challenges

Thermal issues arise from increasing electrical power density with the continuous scaling of the ICs, i.e., feature size shrinking of transistors and interconnects and performance and functionality increases of systems. Feature size shrinking leads to increased transistor leakage power loss and interconnect joule power loss; increasing performance and functionality leads to increased dynamic power loss in logic transistors, interconnects, and repeaters for the interconnects. These power losses in turn increase the temperature in the IC chip. The power for today's microprocessor is around 100 W, with a power density in a range of 100 to 300 W/cm^2 or higher at hot spots. Thermal and power issues are of huge concern for 2-D ICs [85], which is the reason that various FEOL technologies (e.g., high-k gate dielectrics and novel CMOS structures), BEOL technologies (e.g., Cu/low-k processes), circuit designs (e.g., multicore multithreaded processors), and various thermal management technologies are being aggressively pursued to alleviate power and thermal constraints.

Thermal and power constraints are of great concern with any 3-D microarchitecture because die stacking could dramatically increase power density if two highly active regions were stacked on top of each other; such a case should be avoided. Heat dissipation is also challenged by the fact that each additional die is stacked farther and farther from the heat sink. This physical distance results in higher thermal resistances and potentially creates thermal isolation leading to self-heating of additional die.

However, 3-D implementation does not necessarily produce extraordinary increases in chip temperatures, and the power consumption and chip temperature can be even reduced if circuits are properly partitioned and arranged horizontally across each die and vertically across different circuit strata. Thermal-aware 3-D floor-planning is the key [64], [65], [76], [79], [80]. In fact, studies, based on detailed analysis and simulation of state-of-the-art microprocessors implemented in a 3-D stack, showed that 1) the thermal impact of stacking memories on microprocessors is not significant [64], and power consumption of a large memory can be reduced with a proper 3-D floor-planning [59]; and 2) 3-D implementation can improve power, clock frequency, temperature, *and* performance for a given system. For example, in a 3-D logic-to-logic stack of two strata, scaling to neutral performance yields a 54% power reduction; or frequency and voltage scaling can produce a 34% power reduction with 8% performance improvement; or a simultaneous 15% performance gain and 15% power reduction can be achieved [65]. This 3-D benefit in temperature and power is mainly due to significant reduction in long interconnects and the number of associated repeaters (note: 2–3 million repeaters may be required for a 2-D processor designed at 45 nm [86]). Typically a power reduction results in a performance reduction, but in the 3-D design the energy consumed per instruction is reduced without reducing performance.

Three-dimensional platforms provide more design space, allowing a greater range of performance and power tradeoffs while making other thermal and power management possible, such as 3-D power delivery [73], [74] and integration of microfluidic channels for heat removal [87], [88].

D. Infrastructure Challenges

As with any disruptive technology introduced to high-volume manufacturing, 3-D hyperintegration requires:

- equipment for 24/7 operation;
- ECAD and simulation tools;
- standards.

Most processing equipment and tools needed for 3-D integration are listed in Table 3. These tools have been available for years and used in product manufacturing. However, the aligner, bonder and deep via (TSV) etcher do not meet the requirements of the IC industry for high-volume 24/7 manufacturing of 3-D systems. The TSV technology being developed for 3-D packaging can be readily modified for wafer-level 3-D integration. In addition, the wafer bonding processes developed to date can take an hour or more; shorter process times are certainly desirable, maybe with cluster tools. Other process requirements are technology platform dependent as described earlier.

Two-dimensional ECAD and simulation tools are currently used for 3-D integration with some modifications, while the research and development of 3-D design and simulations tools shows good progress [55]–[81], [93]. Significant developments in ECAD and simulation tools are required to: 1) allow use of mixed technology nodes and mixed processing technologies (such as for silicon or compound semiconductor, analog, digital, various types of memories) with abundant IP cores, 2) effectively utilize the 3-D advantages in smaller die size, massive short vertical interstrata interconnects, and huge data bandwidth, 3) provide the flexibility for novel circuit designs that are

impossible with 2-D circuits, 4) establish design rules, particularly for certain circuits that may not be complete in one circuit stratum, 5) include yield enhancements (e.g., redundancy, ECC, DFT, and BIST), and 6) accommodate thermal and power constraints. These will require simulation software to ensure signal and power integrity with semiconductor devices in multiple strata.

Besides equipment and ECAD tools, one very critical infrastructure development for 3-D integration is to establish a set of standards; little has been done so far. It is very critical because 1) various materials and processing technologies are involved and 2) die or wafers can come from different IC manufacturers in different sectors of industry; even the die or wafer sizes can be different. While SEMATECH has attempted to develop a roadmap within the International Technology Roadmap for Semiconductors (ITRS) [89], a new association or society perhaps should be formed in order to establish 3-D integration standards and roadmaps.

VI. 3-D INTEGRATION PERSPECTIVES

Jack Kilby invented the integrated circuit (IC) in 1958 at Texas Instruments. About ten years later, Intel introduced the world's first single-chip microprocessor, the Intel 4004, in 1971. We have since then experienced an exponential growth of ICs following Moore's law in terms of transistor numbers per chip. Both the bipolar transistor and MOS field-effect transistor were the workhorses for about two decades. Since 1990, CMOS has become the predominant technology in digital ICs because of benefits in the areas of circuit size, operating speed, energy efficiency, and manufacturing costs. The major issue that led to the switch from bipolar transistors to CMOS was that the thermal power density of bipolar ICs reached a level that was extremely difficult to cool. After enjoying CMOS technology for little more than ten years, we have encountered again the thermal power issue, as marked perhaps by Intel pulling the plug on a planned 4.0-GHz speed upgrade of its Pentium 4 processor in late 2004. We then entered into an era of single-chip multicore processors [82]–[84], [90]. Since the multicore processor requires huge cache capacity and memory bandwidth, 3-D integration is perhaps the only viable solution to provide the required cache and bandwidth. Considering the profound impact of the semiconductor industry on our business, economics, and society, the author believes that we will soon enter into a new era of 3-D hyperintegration of infotech, nanotech, and biotech systems—a new paradigm for future technologies, as depicted in Fig. 1.

Looking forward, the first killer 3-D applications would be extremely high-density heterogeneous memory stacks (e.g., NAND flash, SRAM, DRAM, FRAM, and PCNVM) and extremely high-resolution/low-cost imagers, followed perhaps by 3-D integration of mixed signal/RF circuits with digital CMOS. Advanced handheld devices will also continue to drive the mix and match of various 3-D approaches.

A variety of 3-D approaches may be combined to offer more flexible integration with even higher functionality, signal integrity, or added value. For example, stacking discrete die (or discrete devices, such as solid-state lasers or GaN transistors) onto a wafer stack provides a pathway for heterogeneous integration of compound semiconductor devices or analog circuits with digital circuits.

Once 3-D integration technology is mature and the design and manufacturing infrastructure (such as ECAD tools, fabrication equipment, and standards) is in place, it is likely that more ICs will be designed for general purposes because massive production of 3-D ICs would lower the manufacturing cost. For instance, a general-purpose 3-D multicore processor with extremely high-density memory, FPGA, and software in the nonvolatile memory in the same stack could be reprogrammed by FPGA or software for multiple purposes, or varying purposes, over a processor's lifetime. We might even have to change the term of "3-D hyperintegration" to "4-D hyperintegration" because the highly integrated system can be changed with the fourth dimension, i.e., *time*. An example would be using PCNVM to change an FPGA or to reroute different processor cores in the same stack if needed at certain times.

As shown in Fig. 1, ongoing research and development in 3-D integration could lead to a new paradigm of future technologies for hyperintegration of infotech-nanotech-biotech systems, enabling extremely high functionality, high performance, and small size and weight with very low cost. Different components optimized for energy/power can be integrated, such as processors, memories, imagers, wireless communications, special functions of nanodevices and MEMS, various micro/nanoscale chemical, bio, thermal, mechanical, electrical, and optical sensors, and even nuclear (radiation) sensors. Different industry sectors, universities, and government may have to reshape their business models to meet the required close collaborations in building more highly integrated systems. In the future, it will not be just a dream that a tiny device can fly, move, see, smell, hear, taste/analyze, feel, and "think"; it will be able to interact with other devices and with human beings and their surroundings; it could perform certain functions, such as for security (e.g., detection of dangerous materials, devices, or terrorists) and health care (e.g., medical devices and drug discovery). Our daily lifestyle and even our culture may be dramatically changed with a proliferation of this 3-D or 4-D hyperintegration technology. ■

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