ECE 546 SPRING 2016

Instructor
José Schutt-Ainé (jesa@illinois.edu) – Office Hours Wednesday 3-4 pm, 5042 ECEB

Class Time
12 -12:50 pm, MWF, 2013 ECEB

Textbooks - Required
W. J. Dally and J. W. Poulton, "Digital Systems Engineering", Cambridge University Press, 1998

Textbooks - Recommended
1. S. Hall and H. Heck, Advanced Signal Integrity for High-Speed Digital Designs. IEEE-J.Wiley, 2009
2. Kyung Suk (Dan) Oh and Xingchao (Chuck) Yuan, High-Speed Signaling: Jitter Modeling, Analysis, and Budgeting, Prentice Hall, 2012.
3. Madhavan Swaminathan and Ege Engin, Power Integrity Modeling and Design for Semiconductor and Systems, Prentice Hall, 2007.

Grading Policy

Homework	60% of total
Project	30% of total
Participation	10% of total

Homework Policy
Problems are assigned every week and are due the following week at the end of the class period. Homework is to be the student's own work, not a collaborative or plagiarized work. However, students are permitted and encouraged to help one another by engaging in discussion of course material and approaches to solving the homework problems. Homework solutions will be posted on the course web-page.

Teaching Assistant
Da Wei (dawei1@illinois.edu) - Office Hours Monday 1-2 pm, 5034 ECEB

WWW Home Page
The course internet home page can be found at *http://emlab.illinois.edu/ece546*

Office Hours
José Schutt-Ainé - Wednesday 3-4 pm - Room 5042 ECEB

ECE 546 SCHEDULE: SPRING 2016

Lect	Date		Topic	Book	
1	**JAN**	W-20	Packaging and Levels of integration	Ch 1 & 2	
2		F-22	Resistance, capacitance & inductance	3.1-3.2	
3		M-25	Ideal transmission line	3.3	
4		W-27	Losses in transmission lines	3.4	
5		F-29	Nonuniform transmission lines	3.4	
6	**FEB**	M-1	Coupled-line analysis	notes	
7		W-3	Multi-line analysis	notes	HW 1 due
8		F-5	MOS Transistors	4.1, 4.2	
9		M-8	CMOS Logic Circuits	4.3	
10		W-10	MOS Amplifiers	notes	HW 2 due
11		F-12	Integrated Circuits	notes	
12		M-15	Measurements of transmission lines	3.6	
13		W-17	Network Parameters	notes	HW 3 due
14		F-19	Scattering Parameters	notes	
15		M-22	S-Parameter Analysis of Transmission Lines	notes	
16		W-24	Conductor Nonidealities	notes	HW 4 due
17		F-26	Blackbox Macromodeling	notes	
18		M-29	Requirements for Physical Channels	notes	
19	**MAR**	W-2	Circuit Synthesis from Macromodels	notes	HW 5 due
20		F-4	I/O Circuits and Models	notes	
21		M-7	MNA, SPICE, Latency Insertion Method	notes	
22		W-9	IBIS Modeling	notes	HW 6 due
		F-11	**EOH – NO CLASS**		
23		M-14	X-Parameters	notes	
24		W-16	Package & parasitics	3.7	HW 7 due
25		F-18	On-chip interconnect issues	4.4	
		M-21	**SPRING BREAK**		
26		M-28	Power supply network	5.1	
27		W-30	On-chip distribution	5.3	HW 8 due
28	**APR**	F-1	Power supply distribution	5.3	
29		M-4	Bypass & decoupling capacitors	5.3	
30		W-6	TSV and Interposers		HW 9 due
31		F-8	Power supply noise	6.2	
32		M-11	Crosstalk noise in distributed systems	6.3	
33		W-13	Dispersion, loss in distributed circuits	6.3	HW 10 due
34		F-15	Measurement of noise	notes	
35		M-18	Jitter Basics	notes	
36		W-20	Eye Diagrams	notes	HW 11 due
37		F-22	Serial Communication Systems	notes	
38		M-25	Signaling convention	7.1	
39		W-27	Signaling over lumped media	7.2	HW 12 due
40		F-29	High-Speed I/O Links		
41	**MAY**	M-2	Advanced Signaling Techniques		
42		W-4	Equalization		
		F-13	**PROJECTS DUE**		