Development of High-speed and Large-capacity 2U MRDIMM: First-ever MRDIMM with Dual PMICs

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***Abstract*—Continuous increase in the demand for high-speed and large-capacity memory modules is being intensified by the development of numerous memory-intensive applications. In order to fulfill these demands, Multiplexed Rank Dual In-line Memory Module (MRDIMM) has been newly proposed in JEDEC, with its main objective being doubling of the data bandwidth without having to overcome the physical limitations in DRAM scaling. In this paper, we introduce the design concept of 2U MRDIMM that can fulfill both speed and capacity needs of various memory-intensive applications. The proposed concepts have been verified through a series of signal and power simulations, as well as Proof of Concept (PoC)-based measurements.**

Keywords—MRDIMM, DRAM, Memory Module, Multiplexer, Bandwidth, 2-PMIC

I. INTRODUCTION

Development of numerous memory-intensive applications such as Artificial Intelligence (AI) and Machine Learning (ML) has driven significant growth in demand for high-speed and large-capacity memory modules. While core counts of processors continue to rise, the increasing difficulties associated with DRAM speed scaling is limiting the system bandwidth and density [1]. In order to mitigate these limitations, use of a buffer with MUX feature to combine two memory ranks has been introduced. In JEDEC, a new DIMM type named Multiplexed Rank Dual In-line Memory Module (MRDIMM) has been proposed, with its main objective being doubling of the data bandwidth using Multiplex Data Buffer (MDB).

As shown in Fig. 1, MRDIMMs are composed of two time-interleaved Pseudo Channels (PS), where data from PS0 and PS1 are selected on even and odd cycles, respectively. As opposed to the conventional DIMMs that only allow access to a single rank, MRDIMM permits simultaneous access to both pseudo-channels through 2:1 multiplexing. As a results, the data rate at the host-side (b/w CPU and MDB) can be twice that of the DRAM-side (b/w MDB and DRAM) without having to overcome the physical limitations in DRAM scaling.

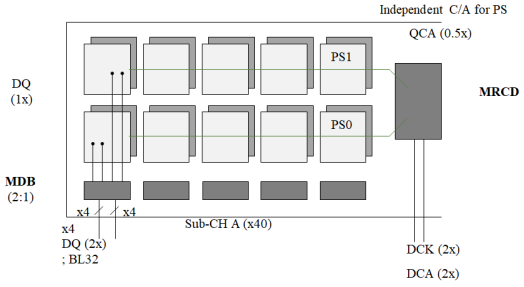

Fig. 1. Concept of MRDIMM with MDB that supports 2:1 MUX feature to enable doubling of the data bandwidth

The demand for high speed can be fulfilled with the use of MDB, and we are left with the challenge of large-capacity. Conventionally, stacking of multiple dies in a package with through-silicon vias or bond wires has been widely adopted; however, stacked-die solutions often suffer from low yield and high cost that make them less viable. Instead of increasing the number of dies in each package, we can also increase the number of packages to meet the capacity requirements. In 2U MRDIMM, we increased the number of DRAM packages from 40 to 80 to achieve large capacity of 128/256 GB. In order to accommodate twice as many DRAMs, 2U MRDIMM will adopt 2 Power Management Integrated Circuit (PMIC) for the first time and have a completely new form factor.

In this paper, we introduce the concept of 2U MRDIMM for the first time that can simultaneously achieve both high-speed and large-capacity. The increased DIMM height, along with the increase in the number of loadings and PMIC, is likely to cause a number of signal and power integrity (SI/PI) related issues. Through a series of SI/PI simulations, we verify that the proposed concepts can successfully hedge potential SI/PI risks. Lastly, measurement results based on Proof of Concept (PoC) samples further confirm the stable operation of the proposed 2U MRDIMM at the target speed.

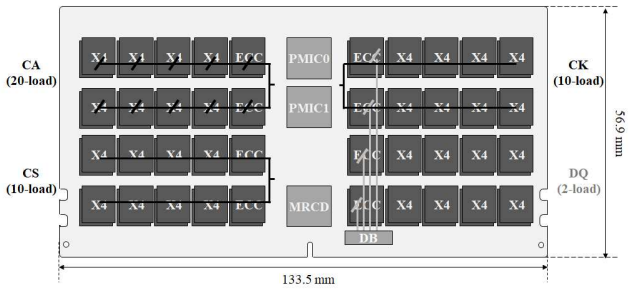

Fig. 2. Design of 2U MRDIMM with 4 rows of DRAMs and 2 PMICs

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II. Concept of 2U MRDIMM

A. SI Design Concept of 2U MRDIMM

As mentioned in the previous chapter, 2U MRDIMM has twice as many DRAMs as standard server DIMMs; 2U (4Rx4) MRDIMM consists of 80 DRAMs, while conventional RDIMMs have maximum of 40 DRAMs (2Rx4). In order to accommodate the increased number of packages, the DIMM height is increased from 31.25 to 56.9 mm, as shown in Fig. 2. This change in the DIMM dimension results in the increased routing length and loadings, which will deteriorate insertion loss and reflection. In order to mitigate these problems, careful design including signal topology is of high importance.

The signal topologies we have applied to 2U MRDIMM are shown in Fig. 3. Post-MDB DQ (MDQ) has two loadings separated at the end of the channel, and expected to have enough margin as the operating frequency of the DRAM-side is only half that of the host-side; for example, for 8800 Mbps operation at host-side, only 4400 Mbps is required for DRAM-side. However, for post-MRCD CA/CS/CK (QCA/QCS/QCK), the number of loadings is substantially increased to 20/10/10 DRAMs; exactly twice that of standard RDIMMs. Despite QCA having 20 loadings, its SI risk is relatively negligible as its operating frequency is only half that of QCK; in addition, QCA can also support 2N mode. Further, for post-MRCD signals, instead of using a fly-by topology, we have applied a Y-topology, where the signal is separated into two traces near the MRCD thereby decreasing the effective loadings at each trace by half, as shown in Fig. 3. By applying this topology, the speed limitation of QCK has been extended from 4.8 to beyond 6.0 Gbps (Host-side 12.0+ Gbps).

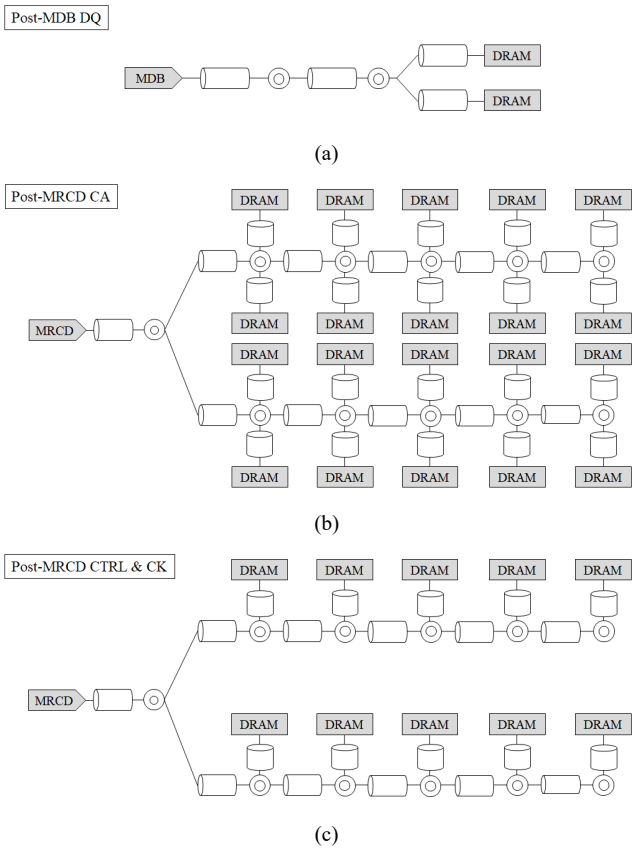

Fig. 3. Signal Topology for (a) Post-MDB DQ, (b) Post-MRCD CA, and (c) Post-MRCD CS/CK

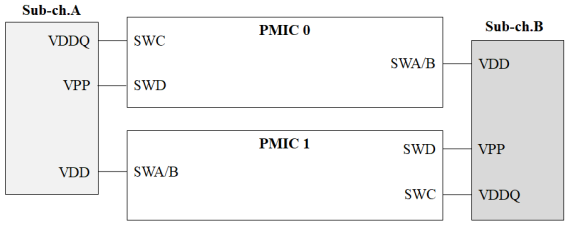

Fig. 4. Dual PMIC configuration in 2U MRDIMM

B. PI Design Concept of 2U MRDIMM

Continuous increase in the data rate and decrease in the supply voltage has led to the mounting of PMIC on DIMM in DDR5. While most 1U DIMMs can operate with a single PMIC, 2 PMICs are required on 2U MRDIMM in order to meet the power capacity and ensure reliable operation of 80 DRAMs. While there are multiple ways that dual PMICs can be configured in 2U MRDIMM, we have prioritized the power capability and connectivity of the planes in our design; to do so, we have decided to separate the corresponding PMIC of the power domains in each sub-channel, as shown in Fig. 4. PMIC0 will be providing VDDQ & VPP for sub-ch.A and VDD for sub-ch.B; on the other hand, PMIC1 will handle VDD for sub-ch.A and VDDQ & VPP of sub-ch.B.

While we expect that the current configuration can fully support reliable operation of 2U MRDIMM, one thing that needs to be checked is that the voltage difference between VDDQ and VDD at DRAMs be below 200 mV at power-up sequence, as defined by JEDEC specification [2]. As VDD and VDDQ of each DRAM are provided by different PMICs, the difference between the two can exceed 200 mV if the enable point of the two PMICs differ by a lot. However, considering the small (few tens of μs) timing difference between PMIC enable commands, we expect that the difference will be small enough and it will be verified in the next chapter.

III. Verification of the Proposed Design Concept

A. SI/PI Simulation Results of 2U MRDIMM

Based on the design concepts discussed in the previous chapter, we have completed the design of 2U MRDIMM, of which the electrical models are extracted for further analysis. For SI analysis, we have done simulation for DQ, CMD, DQS, and special signals, such as reset and alert. While all pre-buffer signals are found to be able to operate at 8800 Mbps, they are highly dependent on the system channel such as CPU and motherboard; therefore, we focused more on post-buffer

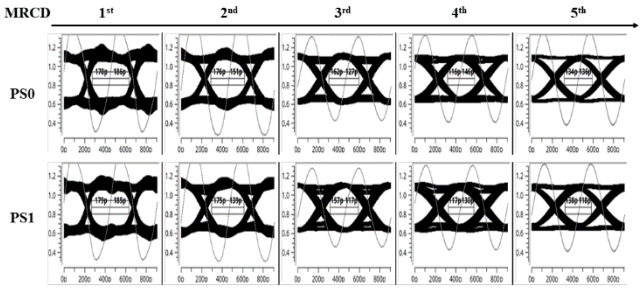

Fig. 5. QCA/QCK simulation results for sub-ch.A PS0/1 at 8800 Mbps

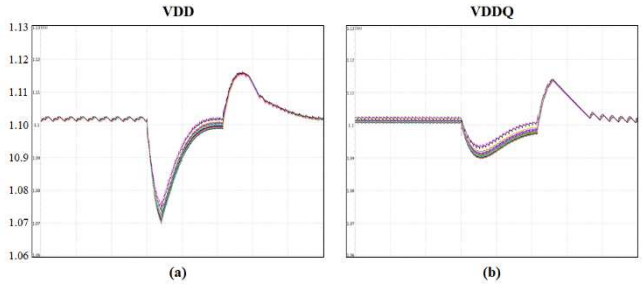

Fig. 6. Load transient characteristics of sub-ch.A (a) VDD and (b) VDDQ

TABLE I. SI/PI SIMULATION AND SIGN-OFF ITEMS

Category	Items for 2U MRDIMM @ 8800 Mbps		Results
SI	DQ	Pre-MDB RxDQ/RxV	Pass
		Pre-MDB TxDQ/TxV	Pass
		Post-MDB RxDQ/RxV	Pass
		Post-MDB TxDQ/TxV	Pass
	CMD	CA/CS min.tIS/tIH	Pass
		BCOM/BCS min.tIS/tIH	Pass
		DCaT/DCaV	Pass
	DQS	Pre-MDB WPRE	Pass
		Post-MDB WPRE	Pass
	Others	RESET	Pass
		ALERT	Pass
PI	Time-domain	Load Tran. @ BGA	Pass
		Load Tran. @ Die	Pass
	Freq.-domain	Z_self	Pass
		Z_self + Z_tranfer	Pass
	Ohters	DC IR Drop	Pass

characteristics in this paper. Fig. 5 shows the QCA/QCK simulation results at 8800 Mbps. The results show that, with the application of the proposed Y-topology, post-MRCD signals of 2U MRDIMM can meet the internal criteria and operate at its target speed, 8800 Mbps.

For PI analysis, load transient in time-domain, input/total impedance in frequency-domain, and DC IR drop characteristics are simulated. One of the main concerns regarding PI was aggravated Vdip due to the increased number of operating DRAMs. The load transient characteristics in Fig. 6 shows that the Vdip values for both VDD and VDDQ are well within the JEDEC specification value, 33 mV. Although this paper only shows the results for sub-ch.A, the same goes for sub-ch.B as well.

The summarized SI/PI sign-off items and results are listed in Table 1. We have confirmed that all of the sign-off items meet the internal criteria, and expect that the proposed 2U MRDIMM is capable of operating at 8800+ Mbps. The pre-buffer signals are marked gray as they depend heavily on the system channel and are easily subject to change.

B. Measurement Results of 2U MRDIMM

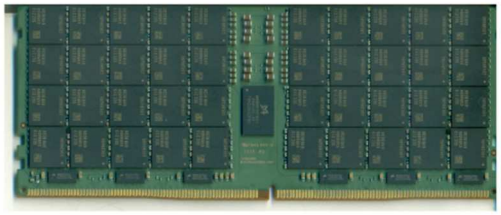

Fig. 7. Fabricated PoC sample of the proposed 2U MRDIMM (Top-side)

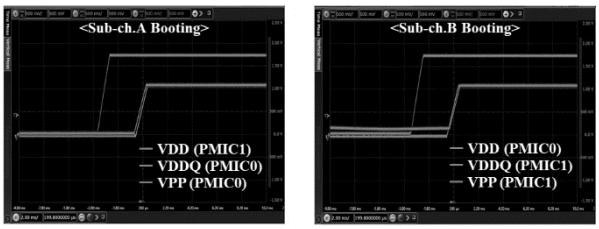

Fig. 8. 2-PMIC operation and power-up sequence of sub-ch.A & B

For measurement-based verification, we have also fabricated a PoC sample with the proposed design concepts as shown in Fig. 7, and performed a series of testing. Fig. 7 shows the top-side of the 2U MRDIMM, where DRAMs, MDBs, and MRCD are mounted; 2 PMICs, on the other hand, are mounted on the bottom-side of the DIMM and are not depicted in the figure. Since the system support for enabling 2-PMIC is currently under discussion, we have first verified the performance of 2U MRDIMM with Automated Test Equipment (ATE).

The ATE-based measurement results also showed that all of the SI/PI sign-off items meet the internal criteria at 8800 Mbps. Further, one last item we had to check through measurement was the power-up sequence, and whether the voltage difference between VDD and VDDQ is kept below the JEDEC specification value, which is 200 mV. As shown in Fig. 8, the timing difference between PMIC enable commands are found to be approximately 50 us and accordingly, the voltage difference between VDD and VDDQ is found be smaller than 200 mV for both sub-channels; in other words, even with 2 PMICs, 2U MRDIMM has been proven to operate robustly with negligible reliability concerns at ATE level. In order to fully validate its reliability, system-level verifications are required, which are still on-going and will be discussed further in future works.

IV. CONCLUSION

In this paper, we introduced the concept of 2U MRDIMM for the first time. 2U MRDIMM aims to achieve both high-speed and large-capacity through the use of MDBs and dual PMICs, along with optimized design concepts. Increased DIMM height and loadings of 2U MRDIMM are likely to cause a number of SI/PI risks; in order to hedge potential risks, we have proposed to use a new topology on post-MRCD signals and configured 2 PMICs so that the power capability and connectivity of the planes are not compromised. We have performed a series of simulations in both time- and frequency-domains and verified that our design can satisfy all of the sign-off items. Lastly, ATE-level testing, based on the fabricated PoC samples, has also confirmed the stable operation of the proposed 2U MRDIMM at the target speed. We expect that the proposed 2U MRDIMM will be widely adopted for numerous memory-intensive applications by supporting high-speed and large-capacity.

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