PCB-level Jitter Sensitivity Measurement and Hierarchical PDN-Z based PSIJ Estimation for PCIe Gen5 SSD

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***Abstract*—In this paper, we first propose a methodology to predict Power Supply Noise Induced Jitter (PSIJ) by accurately measuring Jitter Sensitivity Function (JSF) and Power Supply Noise (PSN) at PCB-level and then converting them into on-chip level characteristics, respectively for PCIe (Peripheral Component Interconnect Express) Gen5 SSD host serial interface design. As a result, we successfully obtained on-chip level JSF and PSN from 1 MHz to 100 MHz which is a targeting frequency range to estimate PSIJ caused by off-chip noise sources in the SSD device.**

Keywords—Jitter Sensitivity Function (JSF), Peripheral Component Interconnect Express (PCIe), Supply Noise (PSN), Power Supply Noise Induced Jitter (PSIJ), Solid State Drive (SSD)

I. INTRODUCTION

With the escalating digital system's transmission speeds, the demand for signal integrity (SI) and maintaining storage device performance has considerably increased in high-speed data transfers. Recently, high-performance mass-produced SSD device supplied to customers operate on the PCIe Gen5 host interface, operating at 32 Gbps per lane with a unit time interval of 31.25 ps [1]. Therefore, the timing margin of PCIe Gen5 eye-diagram is becoming extremely tight and vulnerable to various noise sources generated in SSD product. One of the significant factors is the power supply fluctuations that adversely affect the signal timing margin [2]. This power supply noise induced jitter (PSIJ) could be a significant contributor to timing uncertainty especially in PCIe interfaces between the SSD device and the customer's host system. Therefore, the effect of PSIJ on timing margin should be considered to achieve accurate system-level SI performance prediction.

To analyze PSIJ, information of the power supply noise (PSN) and the jitter sensitivity function (JSF) is essential. In the recent high-speed IP, JSF and PSN requirements are generally defined at the on-chip level and the exact physical location is defined at the die bump. The JSF represents the transfer function of PSN to signal jitter which is IP-level property. For PSN, the simultaneous switching noise (SSN) is considered by analyzing the self-switching current of the target PHY in the chip-level and the hierarchical self PDN-Z [3]. However, within a SSD solution product there are switching regulators and various other ICs on the same PCB which could share the same PDN causing transfer power noise to affect the target PHY. These off-chip level or PCB-level noise sources usually exists from a few MHz to several tens of MHz in the SSD. Although both JSF and PSN can be achieved through circuit-level simulations, a huge amount of computational resources are required to cover low-frequency characteristics and the simulation results may be inaccurate

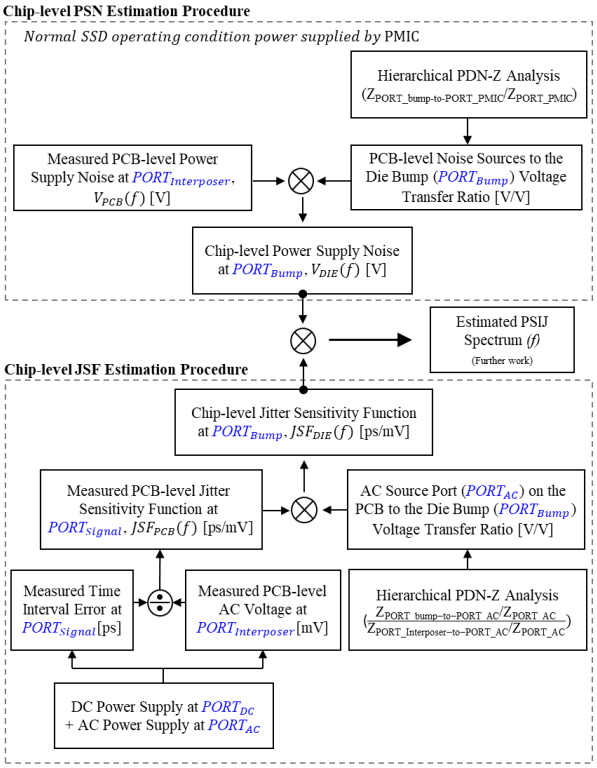

Fig. 1. Block diagram for the proposed PCB-level jitter sensitivity measurement and hierarchical PDN-Z based PSIJ estimation methodology. In this study, predicting both chip-level JSF and PSN procedure is completed and estimating PSIJ will be a future work.

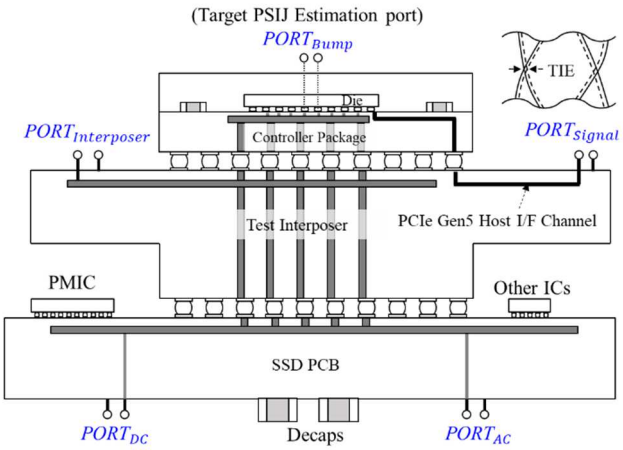

Fig. 2. Cross-sectional view of the architecture for the accurate PCB-level PSN ($\boldsymbol{V_{PCB}}$) and JSF ($\boldsymbol{JSF_{PCB}}$) measurement using the test interposer. The uses of the ports correspond to the purposes marked in the each process depicted in Fig. 1.

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due to process variations. The PSIJ simulation methodology and on-chip measurement techniques are introduced for single-ended memory parallel interface [4]. However, since direct voltage measurement at the on-die bump is not possible in the product level, an accurate PCB-level measurement method should be secured considering measurement equipment settings such as CDR bandwidth of the oscilloscope.

In this paper, we propose an accurate SSD PCB-level JSF and PSN measurement methods and then converting them into on-chip level characteristics for PSIJ estimation on PCIe Gen5 host serial interface channel for the first time as described in Fig. 1.

II. Accurate PCB-Level JSF and PSN Measurement Methods

Both JSF and PSN information at the chip-level defined at the die bump location cannot be directly measured through probing. Therefore, we fabricated the test interposer and connected it between the controller package and the SSD PCB to secure measurable ports so that conduct experiments for the PCB-level measurements, as shown in Fig. 2. In the actual SSD device used for the product, the PCIe host interface channel is designed to send and receive serial data to the host system via the channel of the SSD controller package and the PCB from PCIe PHY in controller die. However, PCIe channel is interconnected from the package to the test port ($PORT_{signal}$) on the test interposer to directly measure PCIe signal waveforms in this study. Since PCIe Gen5 interface transmits a signal at a speed of 32 Gbps, the PCIe test channel routed on the test interposer is designed to have low-loss and less impedance discontinuity enabling accurate high-speed jitter measurements without on-chip equalizers.

The PCB-level JSF (JSF_{PCB}) can be obtained by injecting frequency-varying sinusoidal noise and measuring the jitter response at the desired output on the test interposer. The DC power required for SSD device operation is supplied to $PORT_{DC}$ with a DC power supply equipment, and at the same time, sinusoidal power is applied to $PORT_{AC}$ with a signal generator equipment while varying the AC source frequency from 1MHz to 100MHz. The transmitted sinusoidal AC power source amplitude and signal time interval error (TIE) jitter are measured at $PORT_{Interposer}$ and $PORT_{Signal}$, respectively using the oscilloscope. Then, the jitter sensitivity of the signal TIE jitter to the AC power source voltage can be calculated by taking the ratio of their peak-to-peak amplitudes. For accurate JSF measurement, PMIC and all other ICs are disabled to minimize active components' noise coupling while all de-coupling capacitors are removed to transmit AC power source to the $PORT_{Interposer}$ with minimum distortion.

Fig. 3 shows the jitter transfer function (JTF) plots according to the second order CDR loop bandwidth in the oscilloscope equipment. The conventional jitter sensitivity measurement method with a fixed CDR bandwidth exhibits variations in the jitter transfer ratio within the equipment for different AC source frequencies. For example, in Fig. 3 (a), the measured jitter from AC source with frequency f_1 is attenuated by 3dB and the measured jitter from AC sources with frequencies f_2, f_3, and f_4 within the JTF damping region is amplified. Therefore, as shown in Fig. 3 (b), we proposed a method synchronizing the frequency of the AC power source with the CDR bandwidth to consistently

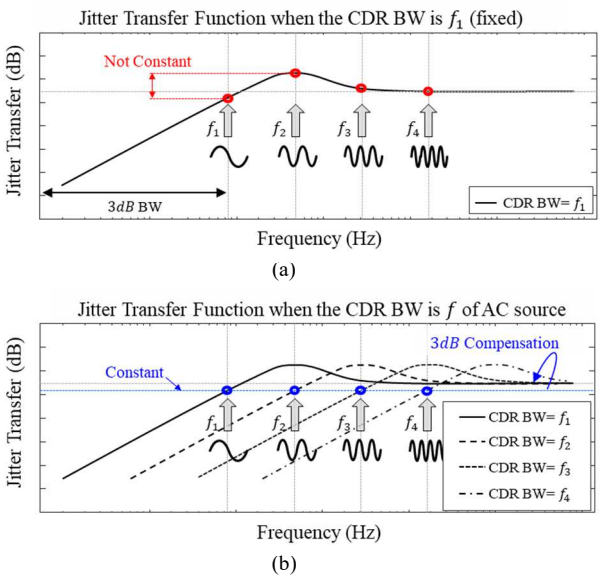

Fig. 3. Proposed jitter measurement method for improving accuracy through the adjustment of second order CDR loop bandwidth in the oscilloscope. (a) Jitter Transfer Function (JTF) with a fixed CDR loop bandwidth (b) JTF plots with the CDR loop bandwidth matched to the AC source frequencies

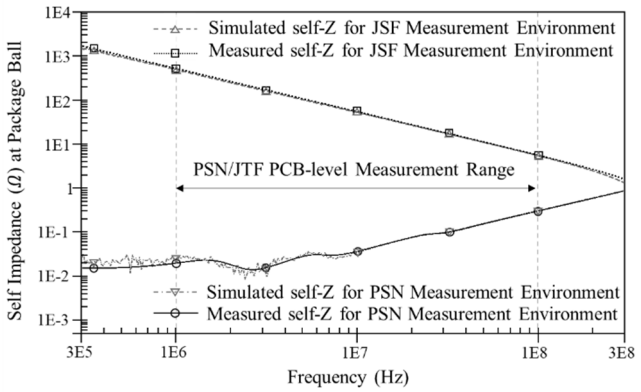

Fig. 4. Comparison of measured and simulated self-Z characteristics. Both self-Z models are for JSF and PSN measurement environment respectively. The simulated hierarchical PDN Z model is accurate enough to replace the measurement.

measure independently of the CDR loop JTF characteristics and compensating the measured jitter components by 3dB.

In the SSD product, there are off-chip noise sources from the various ICs mounted on the SSD PCB that can affect PI characteristics of PCIe PHY, such as PMIC switching noise and other ICs operation noise. Therefore, unlike JSF_{PCB} measurement, in order to calculate PSIJ generated by the PCB-level noise sources, the PCB-level PSN (V_{PCB}) is measured in an actual operating state in which all ICs and passive elements in the SSD device are powered by the PMIC. V_{PCB} is measured at $PORT_{Interposer}$ using an oscilloscope equipment with a low noise power rail probe which has mV sensitivity. Both of the measured JSF_{PCB} and V_{PCB} in this section need to be converted to the chip-level characteristics for PSIJ estimation using the Z-parameter related equations explained in the following session III.

III. Hierarchical PDN-Z Based Chip-Level JSF and PSN Estimation

As introduced in the [5], the hierarchical PDN model based analysis can predict on-chip level signal characteristics

that are difficult to measure directly. While the current transfer ratio can be calculated using the Y-parameter relationship, the voltage transfer ratio (VTR) can be calculated using the following Z parameter based equations, as defined in (1)-(2).

$$Z_{11} = \left|\frac{V_1(f)}{I_1(f)}\right|_{I_2=0}, \quad Z_{21} = \left|\frac{V_2(f)}{I_1(f)}\right|_{I_2=0} \tag{1}$$

$$VTR, \quad \left|\frac{V_2(f)}{V_1(f)}\right| = \left|\frac{Z_{21}}{Z_{11}}\right| \tag{2}$$

VTR between PCB and Chip for JSF,

$$\left|\frac{V_{Port\_bump}(f)}{V_{Port\_interposer}(f)}\right| = \left|\frac{Z_{Port_{bump}-to-Port_{AC}}/Z_{Port_{AC}}}{Z_{Port_{interposer}-to-Port_{AC}}/Z_{Port_{AC}}}\right| \tag{3}$$

VTR between PCB and Chip for PSN,

$$\left|\frac{V_{Port\_bump}(f)}{V_{Port\_interposer}(f)}\right| = \left|\frac{Z_{Port_{bump}-to-Port_{PMIC}}}{Z_{Port_{PMIC}}}\right| \tag{4}$$

Each VTR (3) and (4) for obtaining chip-level JSF (JSF_{DIE}) and PSN (V_{DIE}), respectively is based on hierarchical PDN model, (1) and (2).

The hierarchical PDN model is obtained by combining each PDN model that the package, the test interposer, the PCB and the die as describe in Fig. 2. Each PDN-Z model for the package, the test interposer, and the SSD PCB is extracted by commercial EM simulation tool, Ansys Siwave while the chip PDN model is obtained by chip power model (CPM) format by IP manufacturer. As discussed in Section II, the measurement condition for PSN and JSF are different that the hierarchical PDN-Z curves of each PDN model for measurement become significantly different by the presence or absence of the de-coupling capacitors.

In order to obtain JSF_{DIE} and V_{DIE} data, (3) and (4) are used respectively, and it is verified that the obtained hierarchical PDN Z model is accurate enough to replace the measurement. The self-Z of simulation and measurement are compared using an each different PDN for PSN and JSF respectively, as shown in Fig. 4. The accuracy of each hierarchical PDN model is verified in the proposed test structure except for the controller package since it is not possible to secure any measurable port. Both PDN-Z simulation models for PSN and JSF analysis show high correlations with Z-measurement results from 1MHz to 100MHz. Therefore, V_{DIE} and JSF_{DIE} can be obtained by multiplying measured V_{PCB} and JSF_{PCB} by PDN model based *VTR* in (3) and (4), respectively.

Fig.5 shows the overall JSF_{DIE} estimation procedure by the proposed method. Fig. 5 (a) is the results of JSF_{PCB} measurement explained in the section II. Fig. 5 (b) shows the *VTR* in (4) to PCB to chip-level conversion ratio for JSF. Finally, JSF_{DIE} is obtained by multiplying the results of Fig. 5 (a) and (b) as shown in Fig. 5 (c).

IV. Conclusion

In this paper, we proposed accurate PCB-level JSF and PSN measurement methods to predict PSIJ of PCIe Gen5 PHY at SSD. Especially, the test interposer is fabricated and connected between controller package and PCB, and a test

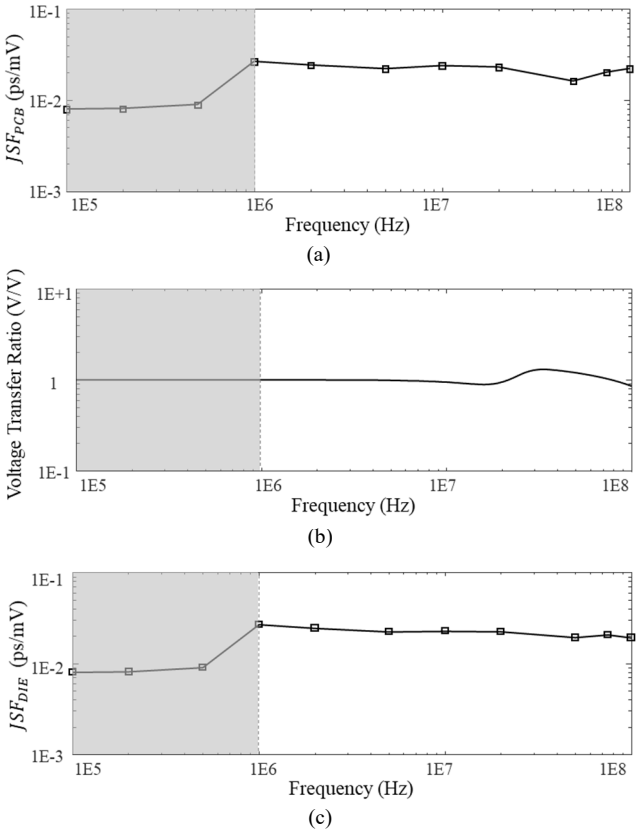

Fig. 5. Chip-level JSF estimation process by the proposed method (a) PCB-level JSF measurement results (b) hierarchical PDN model based voltage transfer ratio (c) converted on-chip JSF results

point is implemented on the test interposer for enabling precise measurements. We proposed the jitter measurement method for improving accuracy through the adjustment of CDR loop bandwidth in the oscilloscope, and the jitter could be measured without distortion. We were able to accurately predict on-chip level JSF and PSN through the proposed hierarchical PDN-Z model. Finally, we estimated the on-chip JSF through the proposed methods, which can estimate the PSIJ of the product with the hierarchical PDN-Z model. For further work, we will analyze PCIe Gen5 host interface SI margin considering PSIJ caused by various noise generated in the SSD product using the proposed methods in this study.

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