Analyses of Via-In-Pad Plated Over (VIPPO) and Dogbone in Fanout Routing High-Density Interconnects

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***Abstract*—The via-in-pad plated over (VIPPO) and the dogbone fanout structures for high-density interconnects are modeled and their high frequency performances are compared. Signal integrity (SI) metrics such as impedance matching, signal loss and crosstalk are analyzed. Compared to the traditional dogbone fanout, the VIPPO fanout features broader impedance matching bandwidth and reduced noise coupling length due to the removal of the parasitics from the dogbone. The SI benefits of the VIPPO vs. the dogbone fanouts are verified further with the eye diagram simulation in channel configurations of a back-to-back module-level channel and a 12dB-loss chip-to-chip system channel. It is shown that the VIPPO structure significantly improves the RMS jitter noise (~40% with the modules at 40Gb/s) and the eye openings (~25% at the system level at 32Gb/s).**

I. Introduction

It is becoming more challenging for the designs of high-speed interconnects with the trend of higher wiring densities and tighter PCB constraints, as the data rate advances (32Gbps and beyond). The conventional layout adopts the dogbone pad for the interconnect routing between the chip package and the PCB via, whereas it introduces the parasitic capacitance and inductance which degrades the impedance matching and the high-speed performances [1]. In addition, for high-pitch packages (the ball pitch~0.5mm), the dogbone pad tends to have the impractically thinner width at PCB clearance limits.

As PCB technologies develop rapidly, via-in-pad plated over (VIPPO) is becoming an alternative routing strategy to the dogbone fanout, where the package pad can be directly soldered with the PCB vias on the copper-plated surface [2]. In this way, the VIPPO fanout not only eliminates the dogbone's parasitics, but also effectively shrinks the signal path length and saves room for finer fanout arrangements. As a result, the VIPPO structure has been more preferred for escaping high-density interconnects including BGA and LGA packages. Accordingly, it is critically important to get deep insights of SI properties of the VIPPO structure over the dogbone counterpart to accommodate the needs of increased fanout densities and higher data rates with optimized SI performances.

In this paper, we simulate and analyze the SI properties of the VIPPO and dogbone structures with differential via models in the BGA fanout pinfield region. The paper is organized as follows. Section II presents the 3D full-wave modellings, and the simulations are carried out in the frequency-domain and the time-domain regarding the via impedance, the signal loss and the near-end and far-end crosstalk. Section III presents the eye simulation results for the module-level channel at 40Gb/s and the system-level channel at 32Gb/s, respectively. Finally, the conclusion is given in Section IV.

II. Modeling Description and Simulation

Figure 1 shows the model diagrams of the dogbone fanout and the VIPPO fanout via models as studied in this paper for the package escaping to PCB via. A total of eight differential vias are included in the model along with the ground vias shown in white color. Both the dogbone via and VIPPO via models share the same via padstack parameters. The via pad and drill diameter are 20mil and 12mil, respectively. The active via length is H_1=43.35mil from the top layer to the internal layer with a short stripline breakout. The via stub length is H_2=15mil extending below the stripline after back-drilling. The dogbone trace on the top layer is designed for 42.5ohm single-ended impedance in the width W=11mil and the length L=10mil, as it transitions the signal from the via pad to the solder ball pad. The 20mil-diameter solder ball is H_3=0.45mm high and is shorted to an above PEC (Perfect Electric Conductor) layer.

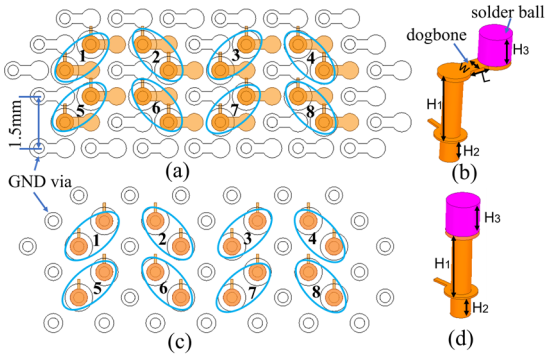

Fig. 1. HFSS models in the pinfield: (a) top view and (b) 3D view for the signal via in dogbone fanout structure; (c) top view and (d) 3D view for the signal via in VIPPO fanout structure. A total of 8 differential vias are included.

The dielectric material for the PCB via cross-section consists of of a hybrid construction including the dielectric constant ε_{r_1}=4.15 and the loss tangent tan_δ_1=0.021 @10GHz for the top dielectric layer and the dielectric constant ε_{r_2}=3.55 and the loss tangent tan_δ_2=0.0065 @10GHz for the rest bulk. The electromagnetic models are simulated using the 3D full-wave solver in Ansoft HFSS.

Figure 2 shows the simulated differential time-domain reflectometry (TDR) results for the via pair 3 with antipad diameters in 28mil and 32mil, respectively.

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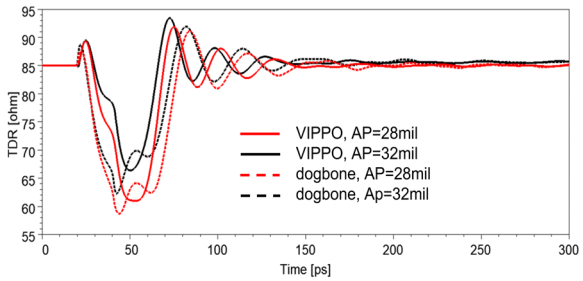

Fig. 2. Simulated TDR impedance for the differential pair 3 in the direction from the top solder ball to the internal stripline breakout (with 20ps rise time and 85ohm impedance reference).

The TDR pulse with 20ps rise time is launched from the top solder ball side to the internal stripline breakout. Both the VIPPO and dogbone via models exhibit the overall capacitive impedance, while both show about 5 to 7ohm impedance rise as the antipad size increases from 28mil to 32 mil. The benefit of using VIPPO is observed in which the dogbone via nearly doubles the impedance dip width compared to the VIPPO via, as the VIPPO via greatly shortens impedance mismatch length.

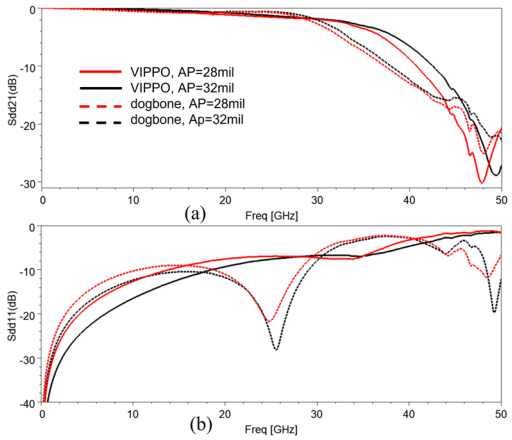

Fig. 3. Simulated (a) differential insertion loss and (b) return loss of the via pair 3. The curves are calculated with 85om reference.

Figure 3 shows the simulated differential insertion loss *Sdd*21 and return loss *Sdd*11. It is shown that the larger antipad helps improve the losses as it increases the via impedance. As compared with dogbone via model, VIPPO via has the 3dB bandwidth increased from 30GHz to 34GHz in *Sdd*21, and has more than 3dB lower loss in *Sdd*11 in the low frequency range to 16GHz. It is also noticed that a sharp dip near 25GHz in the return loss of the dogbone model is associated with the half-wavelength resonance of the signal path. On the other hand, the resonance behavior of the VIPPO is less noticeable and shifts toward higher frequency, indicating the effects of the signal path reduction.

Figure 4 shows the simulated power-sum near-end crosstalk (PSNEXT) and far-end crosstalk (PSFEXT), when the middle differential pair 3 is assumed as the victim and the other seven differential pairs as the aggressors. The crosstalk is observed from the top solder ball side. It is seen that compared with the dogbone via, VIPPO via has lower near-end crosstalk (~4dB down at 10GHz)) in the low frequency range to 20GHz. Also note that VIPPO via improves FEXT for higher frequencies (~4dB down from 20GHz to 28GHz). Note that the dogbone via model shows a dip around 25GHz in NEXT which matches the resonance location in the return loss curve.

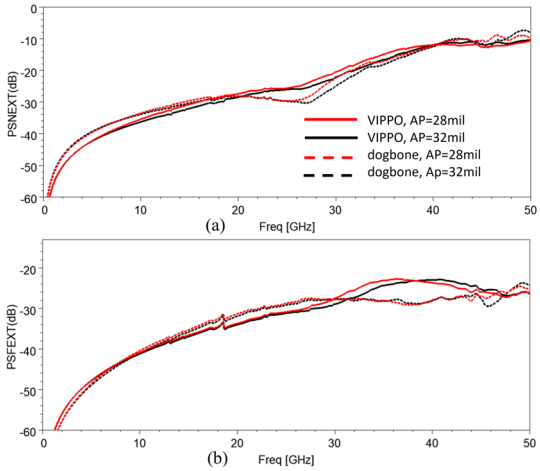

Fig. 4. Simulated (a) near-end and (b) far-end power sum crosstalk for the via pair 3 as the victim observed at the top side. A total of 7 aggressors are considered in the crosstalk calculation at 85om reference.

To further examine how the dogbone's parasitics affect the noise coupling, the transient waveforms are shown in Fig. 5, where the strongest aggressor (the pair 7) is driven with a 1V-amplitude signal in 20-psec rise-time from the top side.

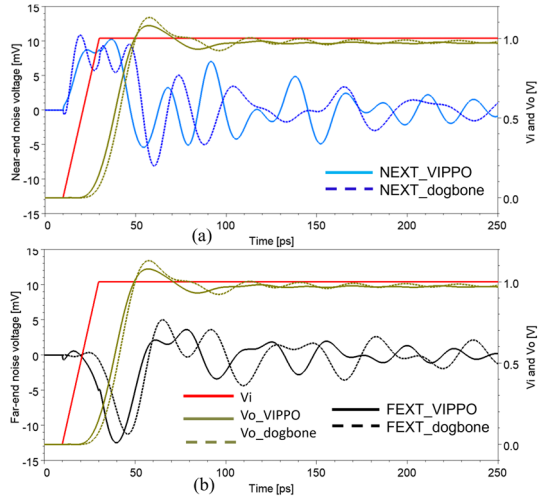

Fig. 5. Simulated (a) near-end and (b) far-end noise waveforms on the victim pair 3 due to the noise coupling from the aggressor pair 7 as observed on the solder ball side in the transient simulation.

The input voltage denoted by V_i is delayed 10ps on purpose and the output voltage denoted by V_o is observed at internal stripline side. Multiple reflections in the backward coupled noise waveform are caused by impedance mismatching with 85ohm terminations. The near-end noise is observed from the time 10ps to 50ps which is featured with relatively saturated amplitude. For the VIPPO via, it is observed that the near-end noise takes approximately 8ps faster travelling back to the top side compared to the dogbone via. Also note that the VIPPO via has smaller swing in the near-end noise voltage, while the dogbone via shows larger noise voltage swing (~5mV). Meanwhile, VIPPO shows the output waveform V_o nearly 3ps faster than the dogbone due to the shorter signal path. From the

far-end noise waveforms, VIPPO via shows around 8ps faster than the dogbone via in the transmission time, and lasts in the duration around the rise time of the incident signal. While the VIPPO via shows a slightly higher (~2mV) voltage peak than the dogbone via, it presents less voltage fluctuation within the entire signal route.

III. TIME-DOMAIN CHANNEL SIMULATIONS

To explore the eye metrics as performed exclusively from the fanout structures, the via models are configured and simulated in the module-level channel at 40Gbps. Differential pair 3 (with 32mil-diameter antipad) is driven directly (1V in amplitude) from the top solder ball side, while the rest pairs are 85ohm terminated. Figure 6 (a) and (b) show the eyes for the single via model, where the signal passes through the via down to the internal stripline escape side. Figure 6 (c) and (d) show the eyes for the via module, where two single via models are cascaded back-to-back so that the signal flows back to the top solder ball side. TX (the driver side) setting uses the peak voltage of 1volt, the bit pattern of PRBS23 and the rise time of 15ps. No equalization is used in the channel for both TX and RX (the receiver side).

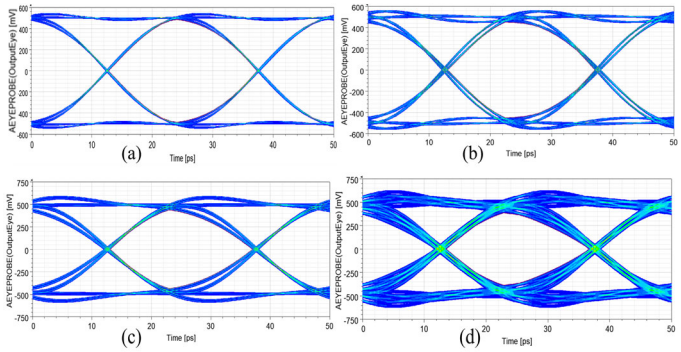

Fig. 6. Eye diagrams of module-level channel simulations at 40Gbps: (a) single VIPPO via module, (b) single dogbone via module, (c) the back-to-back VIPPO via module, and (d) the back-to-back dogbone via module.

As shown from Table 1, VIPPO via fanout shows improved eye metrics than the dogbone via fanout in eye height (EH), eye width (EW) and jitters. In particular, VIPPO back-to-back module channel highlights 15% increase in EH and 40% reduce in jitter compared to the dogbone back-to-back counterpart.

Model name	EH (mV)	EW (ps)	JitterP2P (ps)	JitterRMS (ps)
VIPPO_single	879.986	24.300	0.600	0.117
Dogbone_single	789.487	23.136	1.200	0.311
VIPPO_BB	691.258	23.235	1.300	0.294
Dogbone_BB	599.263	22.057	2.150	0.491

Table 1. Summary of eye metrics for module-level channels at 40Gbps.

Additionally, to evaluate the effects of the via fanout structures to the integrated system, a typical channel shown in Fig. 7 from a chip (the driver side) to a chip (the receiver side) is simulated at 32Gbps. Moreover, integrated assembly models are generated in combining HLGA connectors with the VIPPO and dogbone fanout vias, respectively. Those assembly models are then cascaded back-to-back in the channel with 1.5inch inner layer wiring in between. Both TX and RX ends adopt the same fanout structures: VIPPO-to-VIPPPO and dogbone-to-dogbone. The total channel loss is around 12dB at the Nyquist frequency 16GHz and a total of 9 differential lanes including 8 aggressors are included in the channel link.

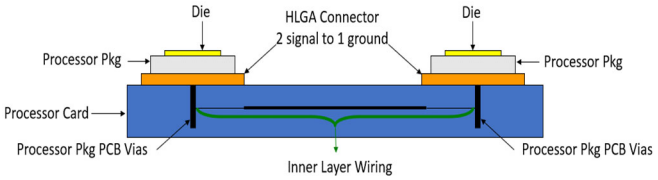

Fig. 7. A chip-to-chip system-level channel topology.

IBM's HSSCDR (High Speed SerDes/Clock Data Recovery) [3] simulation tool is used with optimized equalizations for both TX and RX ends. From 10 million bit by bit simulation, it is observed that at BER=1e-15 level, the channel with VIPPO fanouts has the eye opening in EH=60mV and EW=33.4% UI. With dogbone fanouts, the eye opening has EH=48mV and EW=26.6%. Compared with the dogbone, the VIPPO has the eye opening enlarged by 25% in both EH and EW.

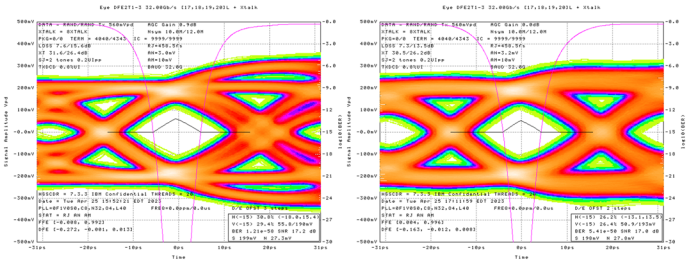

Fig. 8. Simulated RX eye diagrams with (a) VIPPO structures (on the left) and (b) dogbone structures (on the right) for both TX and RX fanouts.

IV. CONCLUSION

In this paper, VIPPO vs. dogbone fanout structures for high-density packages are studied with full-wave simulation models in the characterization of signal integrity properties. It has been shown that the VIPPO structure is better than the traditional dogbone structure in the shortened signal path and alleviated parasitic resonance, thus it greatly improves the impedance matching bandwidth and reduces the near-end and far-end coupling noises. The benefits of the VIPPO structure are verified further by the following eye diagram simulations with enlarged eye openings and reduced jitter noises. The SI characterization for VIPPO over dogbone structures provides useful insights and guidance for implementation with the VIPPO structure in fanout routing high-density interconnects.

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[3] T. Beukema, "Design considerations for high-data-rate chip interconnect systems," *IEEE Communications Magazine*, pp. 174-183, October 2010.