# Package Technology Enabling for 224 Gbps Electrical Signaling


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***Abstract*—224 Gbps is the next fundamental per-lane serializer/deserializer (SerDes) electrical signaling speed target for Ethernet for data centers. Package high-speed signaling performance is a key area of interest to enable competitive channel/platform solutions at this speed. This paper provides a comprehensive review of the package technologies developed for both routing and ball grid array (BGA) second level interconnect (SLI), including the corresponding modeling and validation data. With the proposed technology building blocks, we demonstrate that it is feasible to achieve -6.5 dB overall package loss at 56 GHz and 90˚ C for a typical switch type data center product.**



***Keywords—Package, BGA, SerDes, 224 Gbps, high-speed signaling, insertion loss.***


## I. Introduction

With the continuous increase in data center and cloud compute capability, the corresponding connectivity demand between compute nodes have also been increasing rapidly and consistently. A clear indicator of this trend can be observed in the Ethernet speed and bandwidth trends [1]. The next fundamental per-lane serializer/deserializer (SerDes) electrical signaling speed target for Ethernet is 224 Gbps [2, 3]. Achieving a reasonable reach using a passive electrical interconnect solution at 224 Gbps is very challenging as previously illustrated in [4] and [5]. Achieving a good solution space at this speed requires improvements across all the components in the electrical channel. The 'package' at either end of the channel is a key component, the performance of which is critical to have a competitive channel solution. Some expectations and assumptions about the high-speed signaling characteristic of the package for 224 Gbps electrical signaling are described in [4, 5]. In addition to the performance improvement enabled by the advanced package technologies, it is equally important to have accurate modeling and validation methodologies for both package routing [6] and second level-interconnect (SLI) [7].

This paper provides a comprehensive review of the package technologies developed for both routing and ball grid array (BGA) SLI for 224 Gbps electrical signaling. It also presents the corresponding modeling and validation data, and their correlation using the techniques described in [6, 7]. With the proposed technology building blocks, we demonstrate that it is feasible to achieve a total loss of -6.5 dB for a switch-type data center product package at 90˚ C and 56 GHz, the Nyquist frequency of 224 Gbps pulse amplitude modulation 4-level (PAM4) electrical signaling. To the best of our knowledge, this is the first-time validation data that can demonstrate such capability is presented.

The rest of this paper is organized as follows: Section II describes the routing technologies proposed for 224 Gbps signaling with validation and modeling correlation data. Section III shows the SLI technologies proposed for 224 Gbps signaling with validation and modeling correlation results. Section IV projects the performance of the overall package. Finally, conclusions are summarized in Section V.

## II. Routing Technologies and Validation

Routing is the largest contributor to the overall loss of a package. Technology enablers are required to scale the per-unit-length loss at the increasing Nyquist frequency.

### A. Routing Technologies for 224 Gbps

The package routing loss has been improved consistently over the past decade. This has been achieved by improving (i) dielectric material properties, and (ii) processes for smoother copper without resulting in delamination. Fig. 1 shows demonstrative package routing cross-sections with different copper roughness processes. With the enhancements on these two enablers, bulk conductor loss becomes a new bottleneck, especially with the presence of thinner build-up layer needed for common package line/spacing and via design rules. Typically, thicker dielectrics allow wider traces for the same impedance target, leading to lower conductor loss; but cause coarser overall design rules. Skip-layer routing [5], as shown in Fig. 2, can bypass such a limitation while allowing locally thicker dielectrics, and results in lower loss. An example routing loss breakdown normalized in dB scale with the enablers aforementioned is illustrated in Fig. 3.

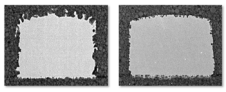

*Fig. 1. Routing cross-sections with different copper roughness.*

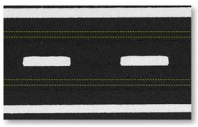

*Fig. 2. A cross-section illustration of the skip-layer design. Yellow dash lines indicate the voided ("skipped") metal layers.*

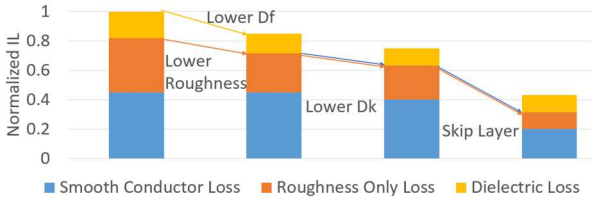


*Fig. 3. A breakdown of routing loss for varying dielectrics, roughness processes and routing architectures, i.e., skip-layer.*


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### B. *Performance Validation and Modeling Correlation*

A routing test vehicle (TV) was designed as shown in Fig. 4, including two skip-layer differential stripline (DSL) structures having the same cross-section but different routing lengths for de-embedding purposes. Insertion loss (IL) validation follows the methodology in [6] and is shown in Fig. 5. An excellent correlation is achieved up to 60 GHz. Similar level of correlation has been achieved for test structures of the standard stripline routing design. Furthermore, the technology with the demonstrated performance has been shown to satisfy long-term package reliability requirements.

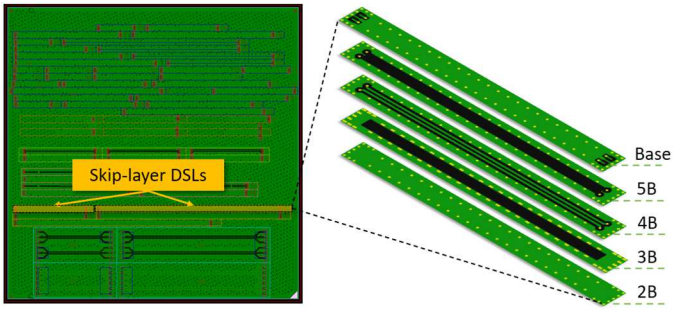


*Fig. 4. Routing TV with skip-layer DSLs.*

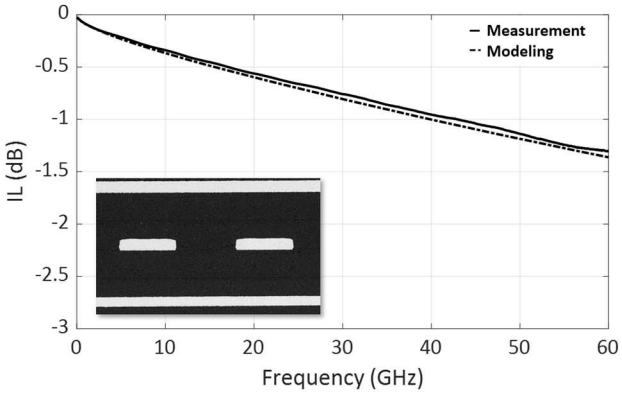


*Fig. 5. Measurement to modeling correlation for routing.*

## III. SLI Technologies and Validation

SLI is often the bandwidth limiter for package high-speed SerDes performance. Technology enablers are critical to push the roll-off frequency beyond the increasing Nyquist frequency.

### A. *SLI Technologies for 224 Gbps*

The typical SLI vertical transition includes micro-vias, plated through holes (PTHs) and BGA solder joints. The following enablers were pursued to meet the 224 Gbps demand.

#### 1) *BGA Solder Joint Dimensions*

The BGA solder joint is usually a capacitive structure, resulting in a low-impedance discontinuity. This typically causes a fast IL roll-off at high frequencies. To reduce the capacitance, it is critical to control the solder joint shape when mounting a package to a board and avoid using adhesives around the signal joints.

Fig. 6 demonstrates that the solder joint width has big impact on IL, therefore a well-designed and a well-controlled surface mount process is critical for 224 Gbps signaling. This requires an accurate warpage prediction methodology at the surface mount reflow temperature and a careful optimization of the die lid design and the board stencil design. As larger lane count pushes for bigger package form factor, a process with varied BGA ball sizes and materials [8] can be needed to both control the solder joint shape and achieve reliable surface mount. In addition to the joint shape, the pitch also needs to scale down gradually. On one hand, smaller pitch of the ball array keeps high-order modes further away from the Nyquist frequency [5]. One the other hand, smaller pitch can reduce the package form factor, which improves the packaging yield and lowers the package cost. The final BGA pitch should be determined after a diligent and a comprehensive trade-off analysis.

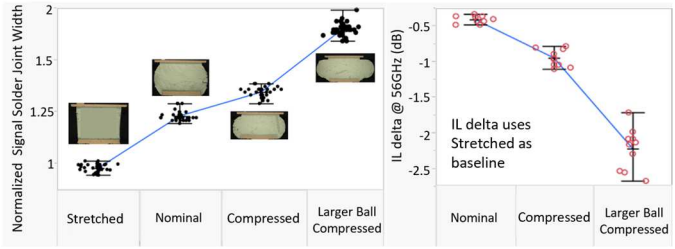


*Fig. 6. Measured impact of signal solder joint width on IL.*

#### 2) *Micro-via and PTH*

Besides the solder joint, SLI comprises a chain of micro-vias and PTH to connect the routing on the front side to the ball pad on the back side. Impedance matching of such a structure generally requires careful design optimization of stack-up, via pattern of signal and ground, via stacking and staggering, as well as anti-pad voiding. This is often a trade-off between electrical performance and mechanical stress. For example, 1000-um thick core sees the loss roll-off about 10-GHz higher than the 1400-um thick core, as shown in Fig. 7. However, the latter provides better warpage control and improves the yield of the surface mount process of ultra-large packages.

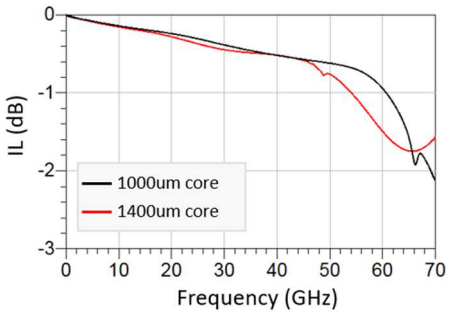


*Fig. 7. Modeled impact of core thickness on IL.*

### B. *Performance Validation and Modeling Correlation*

A SLI TV has been designed as shown in Fig. 8. The test package has 10-2-10 stack-up with 1040 um thick core. It is assembled to a board with 0.8 mm pitch. The measurement is on a symmetric loopback structure including front-side probing pads, package trace, SLI transition to-and-from the board, and a segment of board trace. The de-embedding process removes the probing pads and package traces, then divides the remaining structure in half. The final device and IL are shown in Fig. 9. It includes the SLI and the board transition.

Modeling of the final device uses the actual dimensions of shadow voiding, PTH, solder joint and trace, which are extracted

from 3D X-ray and cross-section measurements. It matches the measured IL very well across the whole frequency spectrum, as shown in Fig. 9. Based on modeling, the board transition contributes about 0.4 dB, thus the insertion loss of SLI in this TV is less than -1 dB.

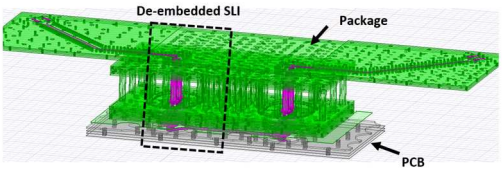


*Fig. 8. Full SLI test structure.*

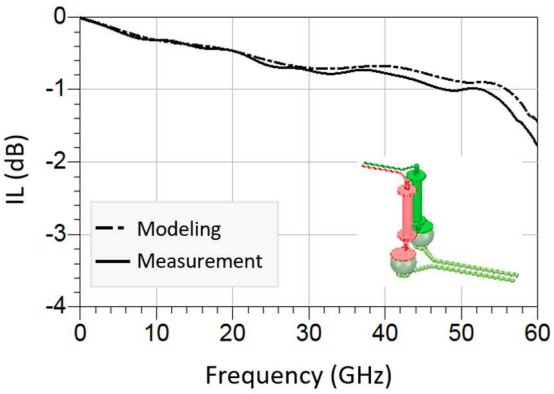


*Fig. 9. SLI Insertion loss correlation after de-embedding.*

## IV. Projected Overall Package Performance

The developed technology building blocks above have proven tremendous performance improvements required for 224 Gbps signaling. It is reasonable to assume about -0.125 dB/mm routing loss with the skip-layer design and -1 dB SLI loss at 56 GHz and 90˚ C. With these, the estimate of the overall package loss is shown in Fig. 10 for a range of routing lengths. It also compares four scenarios with different portions of the routing length in skip-layer design. To reduce the package loss, larger portion of the routing length should be converted to the skip-layer design. As an example, when 80% of 30-mm routing is skip-layer, the total loss is 2 dB less than the design without using skip-layer.

Practically, it may be challenging to use skip-layer design in high density routing regions, as it needs a larger lane width. Therefore, for switch type packages with 256 or 512 lanes, the practical skip-layer usage is no more than 50% and may require a few extra layers. The main goal is to increase the skip-layer usage for the longest lanes. Taking -6 dB as the target, Fig. 10 shows that lanes shorter than 24 mm do not need any skip-layer, lanes up to 27 mm long do not need more than 30% length as skip-layer, and lanes up to 30 mm long do not require more than 50% length as skip-layer.

It is always critical to minimize the routing length in the first place. However, the larger SerDes lane count requires more balls for signaling. In addition, the 56 GHz crosstalk of the vertical transition from package to board requires better shielding with the ground-to-signal ratio beyond 2:1. These lead to a larger ball count, hence larger package form factor and longer routing length. There are two important remedies. One is to reduce the ball pitch to below 0.9 mm. It directly reduces the package form factor. The other is the co-optimization between ball map and die/chiplet placement. A prototype study of the switch type package shows the feasibility of controlling all the 512 lanes under 33 mm. When half the length of the longest lanes is converted to skip-layer, the worst-case total package loss is calculated to be -6.5 dB.

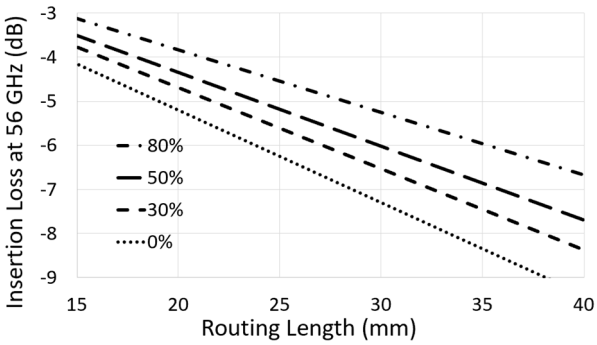


*Fig. 10. Total package loss based on the percentage of skip-layer.*

## V. Conclusions

This paper describes a set of package technologies along with the corresponding electrical validation data to meet the performance demands of the upcoming 224 Gbps SerDes interface. With the presented technologies, a path is shown to achieve -6.5 dB total package loss at 56 GHz and 90˚ C.

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