Analysis of Differential Stripline Routing Approaches within a PCB Via Field for Crosstalk Mitigation

Srijan Datta*, Yuechen Wang, Junyan Tang, Xianbo Yang, Yanyan Zhang, Pavel R. Paladhi, Mahesh Bohra, Joshua C. Myers, Sungjun Chun and Daniel M. Dreps

POWER Series Servers Hardware Development - IBM Corporation, Austin, TX 78758, USA

*srijan.datta@ibm.com

***Abstract*—Signal integrity (SI) in high-speed channels is becoming more critical by the day with increasing data rate of modern computer server systems. Crosstalk generated within the densely packed via/pin field is one of the major sources of SI performance degradation. This work focuses on the tightly pitched striplines within the pin field region of multi–layer printed circuit boards (PCBs) and studies the far-end crosstalk (FEXT) behavior for two frequently adopted routing approaches– "zigzag" and "arc". Electromagnetic modelling and SI analysis are carried out to analyze and quantify the FEXT effect in the two routing configurations with the inclusion of the PCB misregistration effect. Additionally, crosstalk study on the implementation of "tabbed lines" for the two types of pin area wiring is reported. Based on the observed results, routing guidelines are summarized and discussed for improving FEXT within a via filed.**

I. Introduction

As computing data rates continue to increase, crosstalk analysis and mitigation in multilayer PCBs is critical to the design and optimization of high-speed servers [1-3]. Moreover, hardware design trend towards small form factor further increases crosstalk issues due to the dense packing of multilayer PCB vias and wires. In the motherboard PCB, high-speed digital circuit channels of servers typically comprise of: (1) open area wires to carry signals within the same PCB layer in regions which are not space-restricted or noisy, (2) vias which are utilized either for grounding or to transition signals between PCB layers and (3) pin area wires to carry signals within the same PCB layer through a noisy via region. The impact of crosstalk on pin area wires is most significant due to the strong electromagnetic (EM) interference of closely spaced vias and transmission lines within the pin area. Routing of PCB striplines through such a via field is typically done when wiring in/out of module package components and hence cannot be avoided in many instances. Hence, wiring layout through such sensitive PCB regions should be optimized to manage crosstalk and ensure signal integrity at high-speed and high frequency of operation.

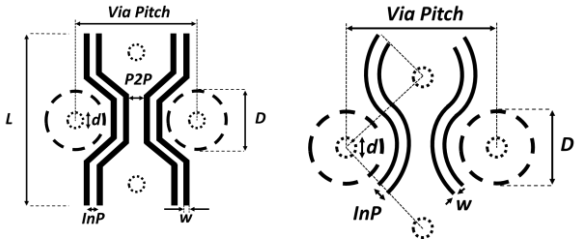
In this work, far-end crosstalk study on stripline pin area wiring is presented for two types of differential routing: zigzag and arc. Electromagnetic modelling is carried out to evaluate the crosstalk behavior for the two routing options. Multilayer PCBs with manufacturing misregistration are also considered to emulate the worst-case SI conditions for the actual hardware. FEXT amplitudes for all the cases are quantified to provide a guideline for pin area wiring designs involving zigzag and arc differential routing.

In some cases, pin area transmission lines are forced to be narrowed from their nominal width due to space restrictions, increasing the wire impedance in the process. Trapezoidal "tab" structures on such densely packed pin area wiring have been widely adopted for impedance management [4]. However, introduction of tabs on the pin area wires will also affect the crosstalk in the pin area region. To that end, the crosstalk impact of adding tabs on arc and zigzag pin area wiring is also reported in this work.

The paper is organized as follows. Section II introduces the 3D full wave EM model for the pin area wiring. Simulation results for the two types of routing are compared and presented in this section for various channel lengths. Section III reports the impact of applying tabs on pin area wiring FEXT. Finally, the conclusions and the recommended wiring guidelines are given in Section IV.

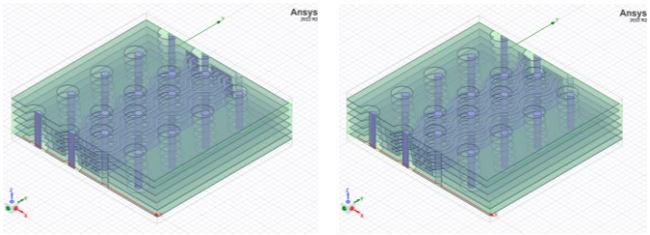
II. Modelling setup and analysis

Fig. 1(a) and 1(b) show the top-view schematic for the two sets of routing – zigzag and arc respectively. As can be seen from the schematic diagrams, the differential wiring is routed through the via field. The two wiring configurations are distinguished by the type of bending implemented to achieve the desired routing. Lane centering is implemented to ensure a symmetrical environment for the striplines when passing each section between the vias. Signal vias with anti-pads are modelled in this study to take into account layer to layer crosstalk through the anti-pad clearing. The dimensional parameters for the two models are: the trace/wire width (W), the via drill diameter (d), the diameter of the via anti-pad (D), and the length of the model (L). The zigzag routing is further parameterized by the pair to pair (P2P) distance. The via pitch is 1.5 mm for both the models. The dielectric material for the PCB has $\varepsilon_r = 3.46$ and $\tan\delta = 0.0052$ at 10 GHz. The trace thickness is 3.25 mils to target an 85 Ohm differential impedance. The thickness of each dielectric layer is 9 mils between the ground planes. The vertical separation from the bottom edge of the trace to the ground layer below is 4 mils. The HFSS models for the two configurations are shown in Fig. 2. A total of 9 differential stripline pairs are distributed in the multilayer PCB model with 3 pairs in each layer. Ground vias are placed between and outside of the differential pairs to simulate pin area wiring environment. Scattering parameters from the single section HFSS model are cascaded to form channels of various lengths (24 mm, 48 mm and 72 mm) and analyze the far-end crosstalk.



(a) (b)

Fig. 1. Pin area wiring schematic (a) Zigzag (b) Arc



(a) (b)

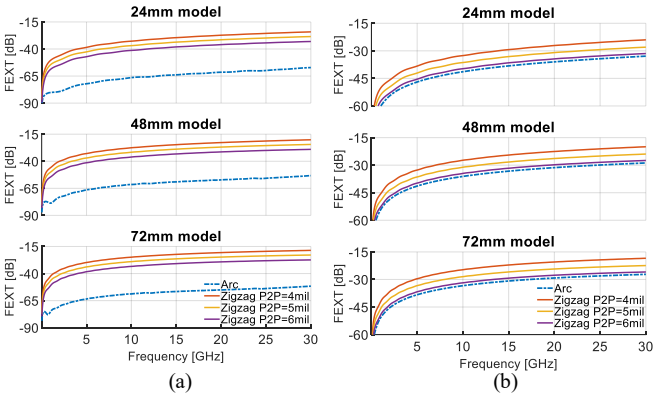
Fig. 2. HFSS model (a) Zigzag (b) Arc

Parameters	D	d	W	L	InP
Zigzag/Arc	28 mils	10 mils	3.25 mils	6 mm	3.5 mils

Table 1. Parameters of a single section of pin area wiring

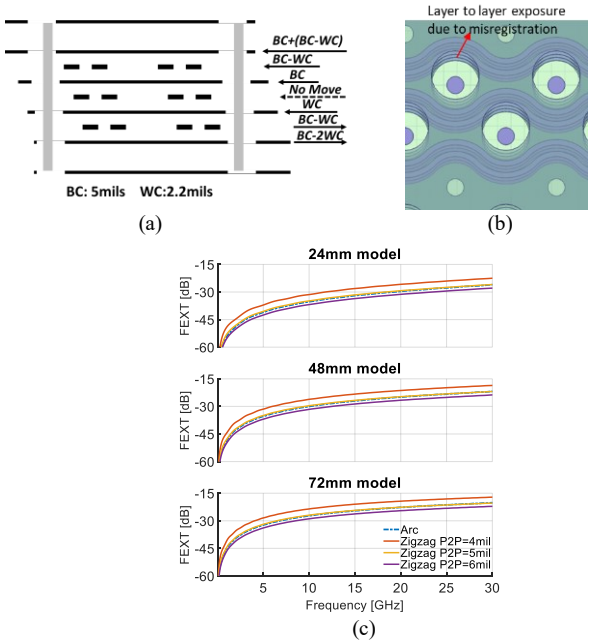
For all the following analyses, the center differential pair in the middle layer is chosen as the victim to cover the worst-case SI scenario. First, FEXT from the same (middle) layer aggressors are analyzed to form a baseline comparison for the two configurations. The pair to pair (P2P) parameter for the zigzag configuration is varied from 4 to 6 mils with a step size of 1 mil. The FEXT from single (middle) layer aggressors for the two routing configurations are shown in Fig. 3(a) to present the scenario when crosstalk coupling only exists within the same wiring layer. The arc configuration produces the least FEXT due to the larger separation between adjacent differential pairs throughout the length of the channels that is provided from the lane centering. Moreover, smooth bending of arc configuration ensures less EM leakage as sharp bends introduces larger discontinuity to the characteristic impedance of transmission lines. As expected, FEXT for the zigzag configuration is highest for P2P = 4 mils and decreases with increasing P2P distance. The FEXT values also increase consistently with increasing channel length for all the cases. FEXT amplitude at 16 GHz (fundamental frequency for a 32Gb/s NRZ high speed interface) for all the cases are summarized in Table 2. Based on the observations mentioned above, it is clear that the arc lines should be adopted for its better FEXT properties when adjacent aggressors only reside within the same layer as the victim net.

Next, FEXT behavior in multilayer PCB is analyzed for the two routing configurations to show the potential crosstalk impact when the pin area wiring is distributed across multiple layers. A total of 8 aggressors (3 each from top and bottom layer; 2 from middle layer) are considered in this case. Fig. 3(b) shows the FEXT powersum for the center victim pair within a multilayer pin area environment. As expected, the FEXT level is increased when more aggressors are included. Although the arc configuration still shows better FEXT properties as compared to the zigzag lines, the relative difference between the two configurations is diminished. As can be seen from the differential FEXT levels recorded at 16 GHz shown in Table 1, the FEXT for the arc lines reduces from -63 dB to -37 dB when three layers of aggressors are enabled. This indicates that the dominant FEXT aggressors for the arc lines are the striplines from the adjacent layers. This also suggests that the vertical coupling through anti-pad is significantly larger than the horizontal coupling for the arc lines. Besides, it is worth noting that, when enabling aggressors from only one layer to all three layers, the crosstalk increase for the zigzag lines are much less compared with that of the arc lines. The FEXT only increased by 0.18 dB, 0.53 dB and 1.59 dB for the three pair-to-pair separations of 4, 5 and 6 mils. This is because when zigzag lines travel near the anti-pads, only a small portion of the trace is in close proximity from the anti-pad while the distance from the arc line to the anti-pad is a constant. This results in a higher FEXT immunity of the vertical coupling for the zigzag lines. Based on the results from the 3-layers models with various lengths shown in Table 1, arc lines still demonstrate better FEXT properties than zigzag lines. However, the zigzag lines could achieve similar or close FEXT performance if an optimum P2P spacing is chosen.



(a) (b)

Fig. 3. FEXT (a) 1 layer (b) 3 layers



(a) (b) (c)

Fig. 4. (a) PCB Misregistration schematic (b) HFSS arc model top view with misregisration (c) FEXT with misregisrtation

Length			24 mm				48 mm				72 mm			
Model Type			Arc	Zigzag			Arc	Zigzag			Arc	Zigzag		
				P2P = 4 mil	P2P = 5 mil	P2P = 6 mil		P2P = 4 mil	P2P = 5 mil	P2P = 6 mil		P2P = 4 mil	P2P = 5 mil	P2P = 6 mil
FEXT [dB] 16 GHz	1 Layer	No Mis-registration	-63.22	-29.06	-33.23	-37.67	-58.54	-24.23	-28.36	-32.78	-56.3	-21.91	-26.03	-30.46
	3 Layers	No Mis-registration	-37.7	-28.88	-32.7	-36.08	-32.82	-24.05	-27.84	-31.22	-30.45	-21.74	-25.53	-28.91
		Mis-registration	-31.47	-27.65	-31.1	-33.08	-26.54	-22.87	-26.26	-28.22	-24.09	-20.6	-23.93	-25.85

Table 2. FEXT powersum amplitudes at 16 GHz

Finally, PCB misregistration is considered to account for the possible layer to layer misplacement during manufacturing process. With the inclusion of misregistration effect, the traces that were previously fully under the coverage of ground planes could become partially exposed in the anti-pad region thus resulting in a stronger vertical coupling. Fig 4(a) shows a cross-sectional representation of PCB misregistration. Fig. 4(b) shows the top view for HFSS arc model with PCB misregistration showing the potential layer-to-layer exposure. The between-core (BC) and within-core (WC) misregistration values used in this work are set to be 4 mils and 2.2 mils as per PCB manufacturer recommendation. The FEXT for the same models and channel lengths with misregistration is plotted in Fig. 4(c). It is observed that misregistration affects the arc configuration the most due to the greater exposure in the via anti-pad region. This pushes the FEXT for the arc model to be the third highest, with P2P = 6 mils producing the least FEXT. From the results discussed in this section, it is shown that the zigzag line with optimized P2P spacing could provide better far end crosstalk control than the arc line when routing in the active via field on multiple PCB layers with misregistration.

III. Tabbed Lines

Tabbed striplines have been applied for impedance management in pin area wiring. Trapezoidal shaped tabs are added to the edge of the transmission lines to increase the mutual capacitance and consequently decrease the differential impedance. This usually improves the impedance matching between the narrowed down pin area wiring and the open area

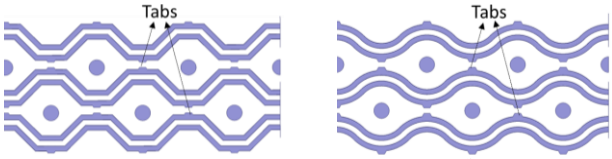


Fig. 5. Tabbed pin area wiring (a) Zigzag (b) Arc

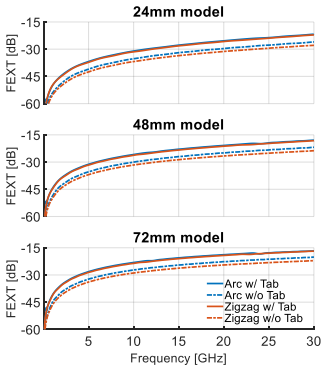


Fig. 6. FEXT for tabbed pin area wiring with misregistration

wiring. However, the introduction of tabs will also increase the mutual coupling between differential pairs and the FEXT will be affected consequently. To that end, tabs are introduced in both configurations (zigzag and arc) to study their effect on FEXT behavior. The top view models with tabs are shown in Fig. 5.

Similar to the previous section, channels of different lengths are simulated and the differential FEXT properties of pin area wiring with and without tabs are shown in Fig 6 for comparison. Without tab FEXT values are also plotted to show the comparison. It is observed that for a 24 mm channel with the introduction of tabs, the FEXT has increased by 8.39 dB and 10.43 dB at 16 GHz for zigzag and arc respectively. This can be attributed to the increased capacitive coupling due to proximity of tabs on adjacent differential pairs. Therefore, while adding tabs on the pin area wiring could be beneficial for impedance matching, the additional FEXT degradation due to the added tabs should also be taken into consideration.

IV. Conclusion

This work investigates the far-end crosstalk behavior of pin area wiring for different scenarios and channel lengths. Two types of differential routing (zigzag and arc) are studied and compared to provide a guideline for pin area wiring designs. While arc routing is observed to be the clear choice when single layer PCB is considered, the choice of wiring is complex in a multilayer PCB with misregistration. It is shown that the layer-layer crosstalk through the via anti-pads is larger for arc in comparison to zigzag routing. Finally, tabbed pin area wiring for both sets of routing are analyzed to study the crosstalk impact of using tabs on pin area wires. Future work will involve studying the full channel effects for all the pin area wiring scenarios using time domain simulations.

References

[1] J. Tang, J. A. Hejase, P. Roy Paladhi, W. D. Beckir and D. M. Dreps, "A Comprehensive Signal Integrity Study of Differential Pairs Routed within a PCB Via Field," *2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, 2018.

[2] J. Tang et al., "Far End Crosstalk Mitigation of Differential High Speed Interconnects Within Printed Circuit Board Via Fields," 2021 IEEE 30th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), Austin, TX, USA, 2021.

[3] J. C. Myers, J. A. Hejase, J. Tang, S. Chun, W. D. Becker and D. M. Dreps, "Signal Integrity Considerations of PCB Wiring in Tightly Pitched Module Pin Fields of High Speed Channels," 2019 IEEE 28th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), Montreal, QC, Canada, 2019.

[4] R. K. Kunze, Y. Chu, Z. Yu, S. K. Chhay, M. Lai and Y. Zhu, "Crosstalk mitigation and impedance management using tabbed lines", *Intel White Paper* 2015.