CISPR 25 Conducted Emission Simulation and Measurement Correlation of an Automotive Isolated Solid-State Relay

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Abstract — **Isolator integrated circuits (ICs) that employ AC switching to send power or data across magnetic or capacitive insulation barriers can create excessive transient di/dt and dv/dt loops that exacerbate electromagnetic emissions. In this work, we developed a robust system-level coupled circuit-to-electromagnetic modeling and analysis methodology to predict the CISPR 25 conducted emission performance of an automotive isolated solid-state relay during product development. The coupled method accurately captures the electromagnetic interactions between the nonlinear time-variant power switchers and the system. Preliminary silicon validation measurements on an automotive isolated solid-state relay are presented to validate the integrity of the predictive modeling methodology. In an EMC pre-compliance lab, good correlations between modeling and measurements are achieved (i.e., within +/- 2-5dB) for emission peaks within the frequency band of 0.15MHz-108MHz. The predictive EMC modeling methodology can be implemented to assess the performance of the initial silicon design during early IC development.**

I. INTRODUCTION

A solid-state relay is an electrically operated switch typically consisting of a solid-state switch that allows or disallows the passage of current between one or more I/O terminals in a high-voltage domain depending on the commands from an integrated circuit (IC) controller powered from an independent low-voltage domain. Additionally, an isolated solid-state relay typically features a high-performance insulation barrier. This high-performance insulation allows the controller IC to transfer power and send logic signals between high-voltage and low-voltage domains while preventing any hazardous DC or uncontrolled transient current from flowing across the domains [1]. Isolation is critical in high-voltage automotive and industrial applications to maintain functionality and protect against electric shocks [2].

Power and signal transmission through the isolation capacitors typically require sharp edge rates that potentially cause conducted and radiated emissions due to the generation of high di/dt and dv/dt transient loops in the system (viz. package and PCB). For conducted emission, the focus of this work, two primary mechanisms have been identified as significant contributors to noise. These include PCB edge and input-to-output dipole emissions [3]. The main emissions component is the common-mode current injected across the isolation barrier. Since isolators drive common-mode current across gaps in ground planes, the disruption in the return current path across the voltage domains creates an equivalent dipole antenna. The ability to predict conducted emissions through simulation is highly desirable to achieve first-pass design success for the stringent automotive CISPR 25 EMC regulatory standard [4].

In this work, we develop a predictive EMC modeling methodology to assess CISPR 25 conducted emission for an automotive isolated solid-state relay. Section II provides some key features and functionalities of the automotive device. The description of the device and system under test (i.e., package and PCB) is detailed in Section III. The modeling flow is reviewed in Section IV. Finally, a comparative analysis between simulation and EMC-certified laboratory measurements is presented and discussed in Section V.

II. ISOLATED SOLID STATE RELAY DETAILS

The device under test is a fully integrated isolated solid-state relay using capacitive insulation that requires no secondary side power supply (see Fig. 1). The primary side consists of a driver which delivers power and logic information through the isolation capacitors to each of the internal MOSFETs on the secondary side. There is also an on-board oscillator which controls the frequency of the driver's operation and employs spread spectrum techniques to optimize EMI performance.

Each MOSFET on the secondary side has a dedicated full-bridge rectifier to form its local power supply and a receiver. The receiver determines the logic state delivered from the primary side through the capacitive isolation barrier and uses a slew rate controlled driver to drive the MOSFET's gate. Each receiver performs signal conditioning on the signals received across the barrier in order to filter common mode interference and ensure that the MOSFETs are controlled according to the logic sent by the primary side driver and the system.
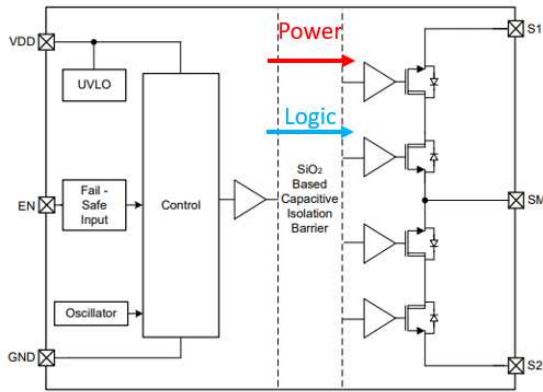
Fig. 1. Functional block diagram of an automotive isolated solid-state relay.

III. SYSTEM & MEASUREMENTS DETAILS

The device is packaged in a 10.3x7.5 mm^2 11-pin SOIC (small outline integrated circuit) package. The primary die, the secondary side and two channels of back to back MOSFETS, are all integrated into the package. The packaged device was mounted on an evaluation module (i.e., EVM) PCB for EMC characterization. It is a 2-layer PCB of size 42.7 mm x 74.25 mm.

Appropriate EVM PCB layout techniques to minimize signal and power integrity issues were employed. Provisioning for additional filter components (e.g., ferrite bead, common-mode chokes, among others) was designed accordingly. Additionally, the PCB design implements a large ratio of primary to secondary ground planes to minimize common-mode noise injection through the CISPR 25 cable. The power input of the system is a 12-V car battery (Fig. 2). The CISPR 25 conducted emission measurement was set up, in a pre-compliance EMC chamber, following CISPR 25 standard requirements [4].
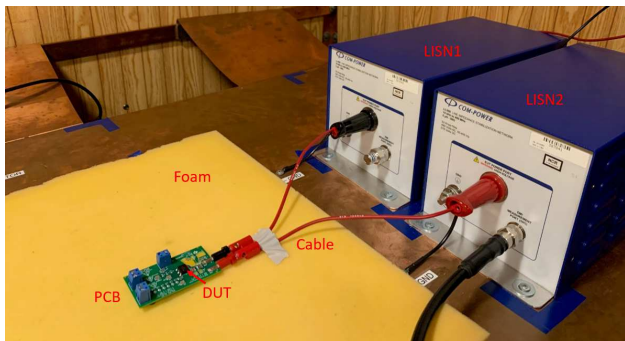

Fig. 2. CISPR 25 conducted emission measurements setup.

IV. EMC MODELING METHDOLOGY

The conducted emission modeling methodology developed and implemented here is formulated through a coupled circuit-to-electromagnetic scheme. A SPICE-based circuit simulator coupled with a 3D full-wave low-rank method-of-moment (MoM) solver solution captures the electromagnetic interaction between the circuit and the system. For full details on the methodology see reference [5]. The measurement setup was created in the modeling environment by developing models for the harness, LISN (line impedance stabilization network), and the DUT system (package and PCB). Measured switching noise sources performed on the EVM are employed as switching stimuli for the modeling.

V. SIMULATION VS MEASUREMENT CORRELATION

Fig. 3 shows the simulated conducted emission versus measurement results comparison. All the simulated peaks are recovered and compared well with measurements (within +/- 2-5dB magnitude). Every resonant peak that corresponds to switcher fundamental and harmonic frequencies is recovered. The discrepancy in the simulation to measurement results can be attributed to the inherent deviations in the measured switching noise stimuli arising from the probe and oscilloscope accuracy.
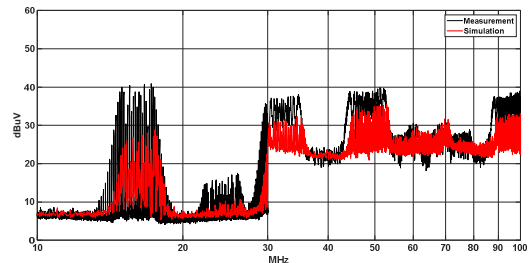

Fig. 3. Measurement vs. simulation correlation for conducted emission.

Once an acceptable correlation was achieved, the predictive modeling methodology was employed to optimize the system EMC performance. An understanding of the emission mechanism is critical to improving the system performance. As such, an equivalent representative circuit showing the path of current flow is shown in Fig. 4.

It can be seen that the emission is mainly due to the common mode noise flowing between the DUT ground net and table (showing by the red arrows). The introduction of a commom-mode choke (CMC) or a stitching capacitor across the primary and secondary ground (GND) nets can potentially reduce the noise flowing into the LISN. The stitching capacitor provides an additional return path to the switching noise between the primary and secondary grounds. The stitching capacitor value was optimized through extensive simulations. Conducted emission measurement was done with the optimized stitching capacitor to validate the simulation result. An approximated 10dB improvement was seen from the stich capacitor implementation. Both measurements and simulation are in agreement as shown in Fig. 5 and Fig. 6 respectively.
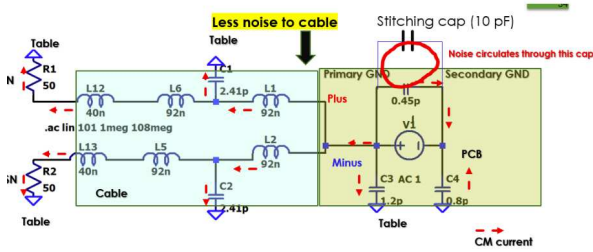
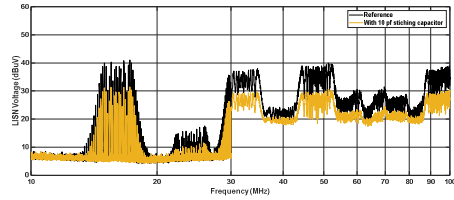Fig. 4. Noise flow path with stitching capacitor.

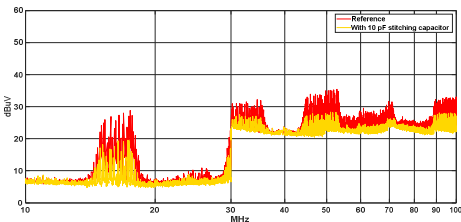Fig. 5. Measurement comparison with and without stitching capacitor.

Fig. 6. Simulation comparison with and without stitching capacitor.

An assessment of the CMC was also conducted. There was no impact on the conducted emission by the inclusion of the CMC. Through simulation, it was clear that the common mode noise was taking an alternate path when CMC was added to supply lines as shown in Fig. 7. The simulation findings (Fig. 8) was validated with direct measurements.
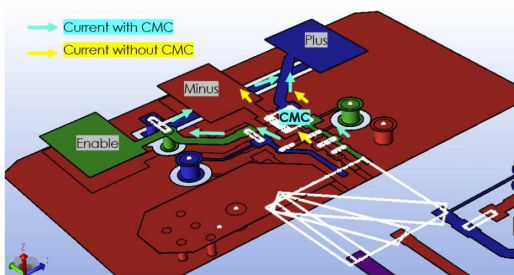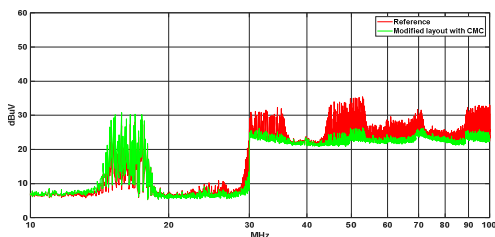

Fig. 7. Noise flow path with CMC included.

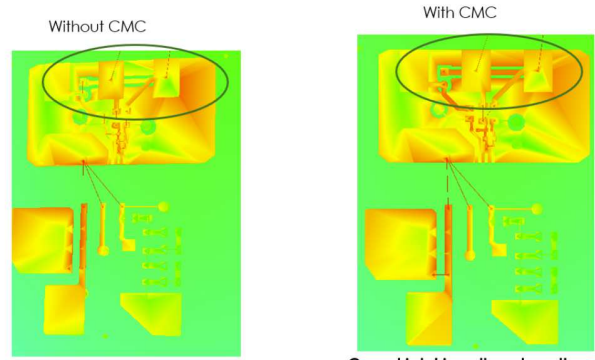Fig. 8. Simulation comparison with and without CMC.

Fig. 9. Current density with and without CMC at 70 MHz.

It is clear that common-mode current flows through the Enable net when Power-Ground line impedance becomes high in the presence of the CMC as shown in the current density compartive plot of Fig 9. With these findings, layout modification was implemented on the EVM to reduce the ground area in order to minimize the coupling between Enable and Ground nets.

CONCLUSIONS

A robust system-level EMC coupled circuit-to-electromagnetic modeling and analysis methodology for predicting CISPR 25 conducted emission has been demonstrated in this work. The coupled method accurately captures the electromagnetic interactions between the nonlinear time-variant power switchers and the system. Considering the inherent measured EVM switching noise stimuli arising from probe and scope accuracy, a good correlation (i.e., within +/- 2-5dB) was observed between simulation and measurements. The predictive modeling methodology developed here optimizes design performance before EMC compliance regulatory testing.

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