Full Wave IBM Plasma Substrate Benchmark By Cadence Clarity

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***Abstract*—The IBM Plasma substrate was first released in 2006 by IBM EIP group through IEEE EPEPS as a public challenge to advanced computational electromagnetic algorithms toward the full package simulation. It has been listed in the IEEE EPS EDMS Packaging Benchmark Suite to advance the state-of-the-art. In this paper, we report the up-to-date modeling performance using this package. After many years of its first release, we might be the 2nd next to Ohio State University to report the full wave whole substrate simulation result. Today, the whole benchmark could be finished from setup to post data processing using Cadence® Clarity Cloud within a very short time. The results from our first run match the measured data very well. The contribution of this paper is to answer the call from IEEE EPS and update the performance of modern computational electromagnetics solutions for electronic packages.**

Keywords— IBM Plasma Substrate, Finite Element Method, AFS, Cloud Computing, Cadence Clarity

I. Background Introduction

IEEE EPS EDMS Packaging Benchmark Sub-Committee created a publicly available suite of packaging benchmarks [1]. It becomes a powerful tool to promote research and applications of advanced modeling technologies for electronic packages, signal and power integrity, and multi-physics EDA solutions.

Among published benchmarks, the IBM Plasma Substrate (as shown in Fig. 1) was first issued by IBM EIP Group from IBM T.J. Watson Research Center in 2006. It was distributed to multiple universities and commercial EDA companies. Then a special session was organized at 2006 IEEE EPEPS to present all the simulation results from different parties. Interestingly, no one really demonstrated a full wave whole substrate simulation capability with a result that was comparable to the measured data. The most successful one might be a tool called IBM PATS [2]. However, PATS used certain quasi-static approximations to simplify the simulations. Hence, it could not be considered a real full wave solution. At IBM EIP team, we used IBM Blue Gene supercomputer and home-made integral equation method to obtain highly accurate result for a quarter of this substrate [3].

In 2010 Professor Jinfa Lee and Dr. Zhen Peng from Ohio State University (OSU) approached IBM through Dr. Lijun Jiang to test their novel nonconformal finite element domain decomposition method on this Plasma module. The first big trouble they encountered was how to mesh the whole substrate, which took them many weeks. In 2011, they published the first full wave full substrate simulation result for this package [4].

Plasma substrate was issued with the measured data made by Alina Deutsch using her short pulse measurement system and IBM EIP Tools [5]. Hence, it became a very rare and valuable real case benchmark that could help the public to challenge and verify novel algorithms and modeling capacities.

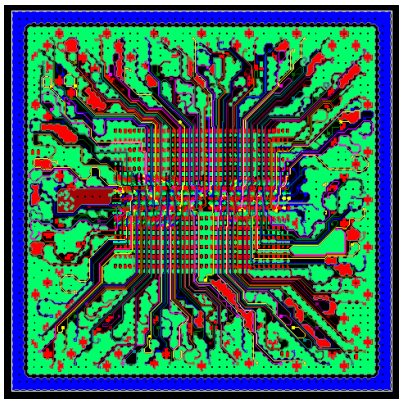

Figure 1. The fan out view of the IBM Plasma substrate.

After another 10 years, IEEE EPS EDMS brought it back to further advance the state-of-the-art solution methods. EDA tools also have been progressed to an unprecedent level. Simulation tasks that were not affordable became possible. In this benchmark work, we report the signal integrity modeling results for IBM Plasma package using Cadence ® Clarity tools. The experiment shows that the whole substrate can be meshed, simulated, and analyzed in an integrated system very efficiently. Boosted by novel computational electromagnetics algorithms, advanced parallelization methods, and powerful computing hardwares, we could easily finish the whole modelling process in a very short time and generate the results that match the measured data in the first run. Instead of months or weeks, the task was done within days.

This work answers the call from IEEE EPS EDMS Packaging Benchmark Sub-Committee as an effort to establish the state-of-the-art of electronic package modeling technologies.

II. Simulation Methods and Simulation Tool

A. Full Wave Solution by Cadence Calrity 3D

The finite element method (FEM) solution provided by Cadence Clarity 3D solver [6] has an elastic computing architecture, massively parallelized matrix solver, and cloud ready distribution capability. Specially, it has seamless integration with the popular chip design platform Virtuoso, the package and PCB designer Allegro, and many other EDA tools. Through them, the model's structural edition, material setup, mesh control, and post processing become convenient and reliable.

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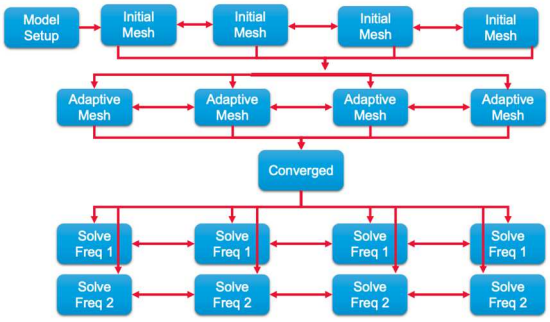

Figure 2. The distributed processing flow in the Clarity 2D solver.

B. *Distributed Processing Flow*

Parallel computing has been deeply planted into the simulation algorithms to use the power of multicores and distributed memories. Meshes are not only adaptive, but also distributed. The adaptive frequency sweeping is also made parallelized. A processing flow illustration is shown in Fig. 2.

This highly distributive computation is a collective result of the state-of-the-art domain decomposition algorithms. It enables the simulations of huge complex structures on multiple 32 CPU cores machines.

C. *Cloud Computing*

Because of the availability of various computing platforms, Clarity CX architecture supports various network possibilities, as shown in Fig. 3.

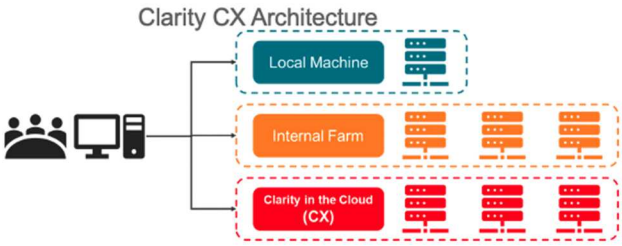

Figure 3. Clarity CX Architecture.

Specially, its web-based cloud solution allows designers to select lower cost cloud computing resources while maintaining the optimal performance in solving 3D structures. It can operate in the AWS cloud and keep the design data safely on local computers. It is very flexible in computer resources – users can assign the number of cores – from 32 to thousands on demand, as shown in Fig. 4.

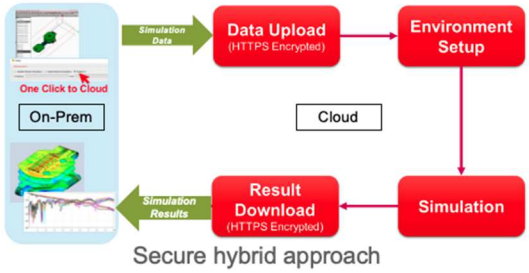

Figure 4. Clarity Cloud architecture.

III. Bencmark Results

IBM Plasma substrate has a 3-2-3 organic stackup. The material information is correct in its original board file. Back to 2006, a popular model setup was to target the lower left quarter that was measured by IBM EIP. Hence, in this benchmark, we started with this quarter first. Then we extended the model to the whole substrate.

A. *Simulation Resource Requirements*

Table I and Table II show the simulation resource usage summary. Table I is for the quarter session of the substrate while Table II is for the whole substrate. There were 20 signals with 40 ports modelled and simulated in one shot. A single Linux machine with 72 cores was used.

Table I. Simulation Summary for the Quarter Design

Initial Mesh	Adaptive Mesh	High Frequency	Low Frequency	Final Simulation	Total Time	# of Total Frequencies	# of Elements	# of Ports
0:51:19	2:31:5	12:8:35	0:23:43	12:32:34	15:55:23	87	13356365	40

Table II. Simulation Summary for the Whole Substrate

Initial Mesh	Adaptive Mesh	High Frequency	Low Frequency	Final Simulation	Total Time	# of Total Frequencies	# of Elements	# of Ports
4:24:39	8:40:6	47:51:3	1:6:23	48:58:47	62:5:18	128	35619469	40

A few observations are made from the above tables:

a. Over 13 million elements are generated for the quarter portion. Then over 35 million elements are generated for the whole substrate. It is a big problem challenging both algorithms and hardware.

b. Computing time in Table II is roughly 4 times of that in Table I, which is a reasonable scaling.

c. Whole substrate simulation was achieved.

By using the Clarity Cloud, the needed resource has been significantly reduced. The results and comparisons will be presented at the conference.

B. *Simultion vs Measurements*

The simulation results are prepared to demonstrate the quality of the benchmark. In Fig. 5, the return losses of one signal from C4 side and BGA side are plotted to check the design quality. From it, we could tell that the chip is matched below 10 GHz, which means it could support less than 20 Gbps single ended data rate.

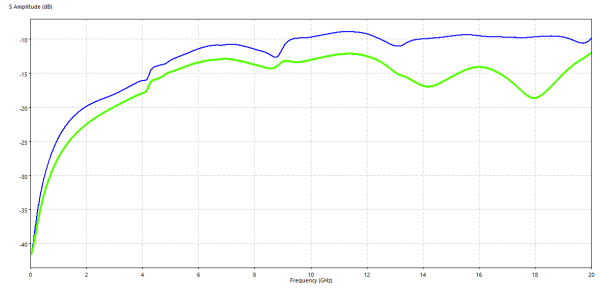

Figure 5. S_{11} of one signal trace looked from C4 side (Green) and BGA side (Blue).

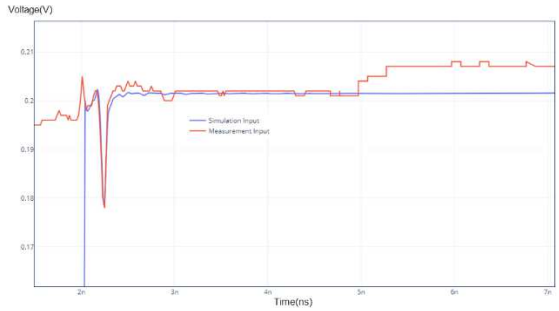

Figure 6. TDR at the input port of the signal trace.

The TDR at the input port of the trace is shown in Fig. 6. Compared to the measured data, discontinuity positions and impedance levels are accurately captured by the simulation. The measured data has more small ripples, which might be contributed to the probes in the measurement and the connectors used by the measurement system.

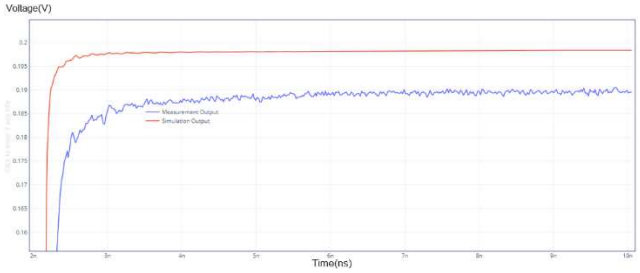

Figure 7. TDT at the output port of the signal trace.

The TDT at the output side of the selected signal is given in Fig. 7. We see that the simulation response is smoother, faster, and less lossy than the measured data. The reason might be that we do not have the surface roughness applied to the copper surface in the model. With the 25um typical trace width, surface roughness could affect the loss and response significantly. Hence, it could cause the difference between simulations and measurements.

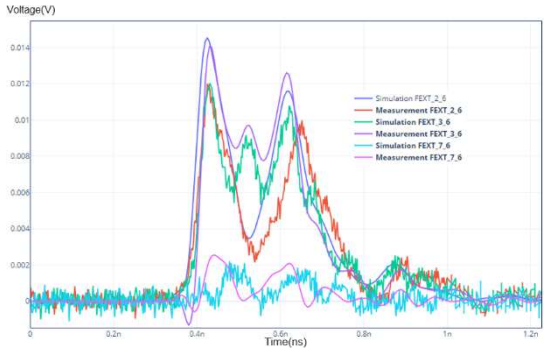

Figure 8. FEXT from aggressor signal 2, 3, and 7 to the victim signal 1.

The crosstalks to a victim signal from two neighborhood aggressor signals (2 and 3) and from a well separated signal (7) are simulated and compared with the measurements. Unused C4 and BGA balls are assumed open during the test. The results of FEXT are shown in Fig. 8. From it, we can see that simulations can correctly predict the crosstalk signal's ripple shapes and voltage levels.

Similar comparisons for NEXT can be found in Fig. 9. The consistency between measurements and simulations is clearly demonstrated. Considering these results were achieved directly from the first run, the modeling efficiency from geometry input to data collection is very helpful to complex packaging designs.

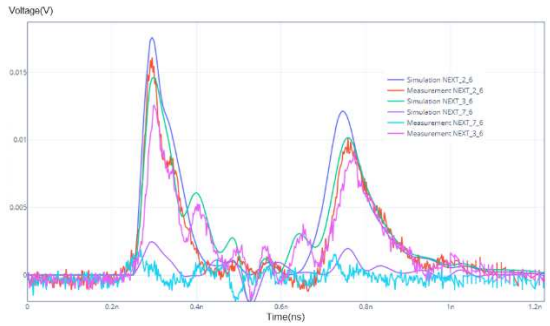

Figure 9. NEXT from aggressor signal 2, 3, and 7 to the victim signal 1.

IV. Conclusions

In this paper, we use Cadence Clarity to test run the IBM Plasma substrate benchmark to answer the call from IEEE EPS EDMS Packaging Benchmarks Committee. The simulated data match the measurements very well. It is demonstrated that using advanced CEM algorithms and parallelization methods, we could efficiently model and simulate complex package problems that were very difficult or impossible.

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References

[1] http://www.packaging-benchmarks.org

[2] B. Krauter , M. Beattie, D. Widiger , H. Huang, J. Choi and Y. Zhan, "Parallelized Full Package Signal Integrity Analysis Using Spatially Distributed 3D Circuit Models," *2006 IEEE Electrical Performane of Electronic Packaging*, Scottsdale, AZ, 2006, pp. 303 306, doi : 10.1109/EPEP.

[3] J. Morsey, A. Deutsch, J.P. Libous, C. Surovic, B. J. Rubin, L.J. Jiang, and L. Eisenberg, "The use of accelerated full-wave modeling to analyze power island coupling in a HyperBGA SCM," *IEEE Trans. on Adv. Packaging,* vol. 30, no. 2, pp. 288-294, May. 2007.

[4] Y. Shao, Z. Peng and J. Lee, "Full Wave Real Life 3 D Package Signal Integrity Analysis Using Nonconformal Domain Decomposition Method," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 2, pp. 230 241, Feb. 2011, doi : 10.1109/TMTT.

[5] A. Deutsch, G. Arjavalingam , G. V. Kopcsay and M. J. Degerstrom , "Short pulse propagation technique for characterizing resistive package interconnections," in IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 15, no. 6, pp. 1034 1037, Dec. 1992, doi : 10.1109/

[6] https://www.cadence.com/en_US/home/tools/system-analysis/em-solver/clarity-3d-solver.html