Efficient Boundary Element Methodology for Analyzing Interconnects in Multilayered PCBs

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***Abstract* — An efficient methodology to analyze interconnect structures in multilayered printed circuit boards is presented. The proposed methodology demonstrates significant speed up over a state-of-the-art boundary element commercial solver alongside some added accuracy benefits. The proposed methodology is employed to analyze packaging benchmark structures for demonstrating accuracy and efficiency.**

Keywords—Multilayered Green's function, magnetic current, method of moments, domain decomposition, measurement correlation.

I. INTRODUCTION

Boundary element analysis is an efficient method for analyzing 3D electromagnetic fields in printed circuit boards (PCB) interconnects. Its efficiency is primarily due to surface discretization of homogeneous regions and availability of O(NlogN) algorithms to setup and solve the system matrix. It is well known that the efficiency of boundary element method can be further improved by using layered medium Greens functions to model layered dielectrics in printed structures without having to explicitly discretize the dielectric interfaces [1]. In that case the unknown current is distributed only on the metallic structures and effect of the layered dielectric is computed using the Sommerfeld integrals without increasing the system matrix size.

However, even with the above advances in boundary element method, the modern trend of high pin count and demanding accuracy requirement for ultra-high speed signaling can often make the computation cost prohibitive, especially for thick boards with large layer count and long high-speed channels. This is mainly driven by the large mesh count needed to discretize this structure with sufficient resolution for the current that flows on the metal surface. With a closer look at the typical PCB interconnect geometry, it is easy to see that the signal path consists of signal traces, vias and return path on the larger reference planes in close proximity to the signal paths. It is obvious that a very large portion of the mesh elements are used to discretize the reference planes due to their large area and complex shapes to accommodate many voids to allow other nets. For a boundary element analysis, it is possible to implicitly model these reference planes within the Greens function computation without having to explicitly mesh them. This can lead to significant savings in terms of mesh elements. Of course, in reality, for a multilayered PCB structure these reference planes are never solid metals. Typically, they have voids accommodating via transitions, routing and area fills for other nets. So special treatment must be done for the void areas when these reference planes are modeled without explicit discretization.

The paper presents such a methodology for modeling interconnect structures with via transitions without explicitly meshing the reference planes. The presented methodology and a standard commercial tool employing boundary element with fast solvers and layered medium Greens functions are employed to analyze the EPS benchmark problems and more to demonstrate the validity of the presented method in analyzing realistic interconnect structures.

Similar approach was proposed earlier in [2][3] for shielding and scattering analysis. To our knowledge, there is no published work reporting this methodology for analyzing broadband digital interconnect structures, where there are vias passing through the implicitly modeled reference planes.

II. LAYER-BASED DOMAIN DECOMPSITION

As briefly introduced in the previous sections, the Boundary element or Method of Moments (MoM) is a widely used numerical algorithm for the electromagnetic analysis of structures embedded in layered dielectric media, such as integrated circuits (ICs) and PCBs. The MoM, thanks to the use of the Dyadic Green's Functions, does not require explicit modeling of reference planes and dielectric interfaces, leading to a remarkable reduction in the total number of mesh elements with virtually no penalty in terms of the accuracy. In this approach, the effect of signal traces and apertures is modeled by using equivalent magnetic and electric currents radiating in a homogeneous environment [1].

To illustrate the strategy adopted in this paper, let us consider the structure reported in Fig. 1. The developed technique will decompose the via transition into a number of homogeneous regions $R_{1,2,\ldots,n}$, electromagnetically described by the equivalent currents $J_{1,2,\ldots,n}$ and $M_{1,2,\ldots,n}$.

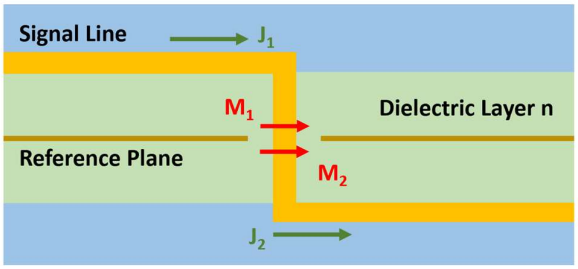

Fig. 1. Via transition.

As a first level approximation, we can assume $M_1 = - M_2$ (reference plane with no thickness) and impose the continuity of the electric and magnetic fields on the conductive structure and apertures. The finite conductivity and surface roughness of the signal structures is considered by applying a surface impedance condition for the associated metallic patches [2]. It is worthwhile mentioning that the finite conductivity of the reference plane can be taken into account by modifying the Green's function calculations accordingly.

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We discretize the domain under analysis by using triangular patches which can easily conform to any geometrical surface or boundary. The current density induced on each conductor / aperture is approximated as linear combination of Rao-Wilton-Glisson (RWG) basis functions and the Galerkin testing procedure is finally applied to derive the linear system reported in (1):

$$\begin{bmatrix} L^{EJ} & K^{EM} \\ K^{HJ} & L^{HM} \end{bmatrix} * \begin{bmatrix} J \\ M \end{bmatrix} = \begin{bmatrix} V \\ 0 \end{bmatrix} \quad (1)$$

where L^{nm} and K^{nm} represents the L Electric Field Integral Equation (EFIE) and K Magnetic Field Integral Equation (MFIE) operator for n-type field and m-type source, respectively.

The presented methodology can accurately model slots (assumed to be homogeneous) in thick reference planes by including additional regions for each continuous aperture (Fig. 2). By applying the equivalence principle, the top and bottom surfaces of each aperture are covered with Perfect Electric Conductor (PEC) patches where equivalent magnetic currents M_1 and M_2 are defined [3].

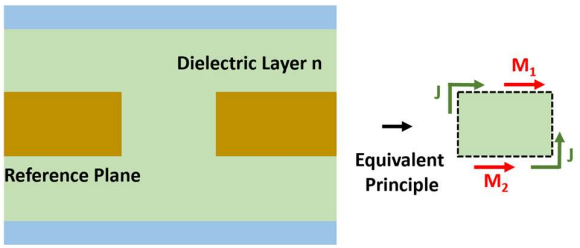

Fig. 2. Equivalent Principle.

In order to take into account the effect of the newly formed cavity and reduce the problem to a homogeneous one where we can derive an analytical Green's function, an equivalent electric current J is defined over the whole thick aperture surface.

It is worthwhile noticing how the interaction between vertical electric currents and horizontal magnetic ones is generally numerically difficult to handle. When the mentioned sources are near each other, the analyzed problem can become unstable at very low frequency (Fig. 3). As indicated in [4], particular care needs to be dedicated to the loop over loop interactions for the K-operator to avoid the mentioned issues.

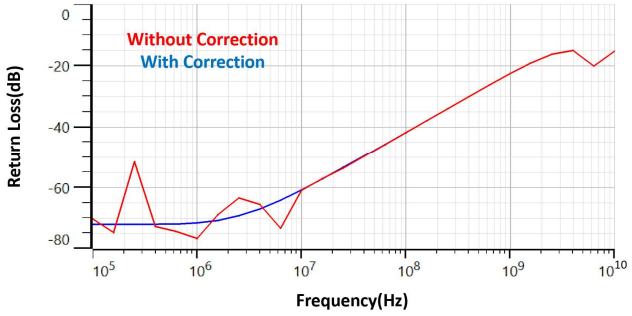

Fig. 3. Low frequency stability.

III. NUMERICAL RESULTS

Several test cases were used for validation including external, publicly available test cases such as Package Microstrip [5] (Fig. 4) and Plasma Package [6] (Fig. 5) from IEEE Electronics Packaging Society (EPS) Technical Committee on Electrical Design, Modeling and Simulation (TC-EDMS) Packaging Benchmark Suite [7] as well as internal designs.

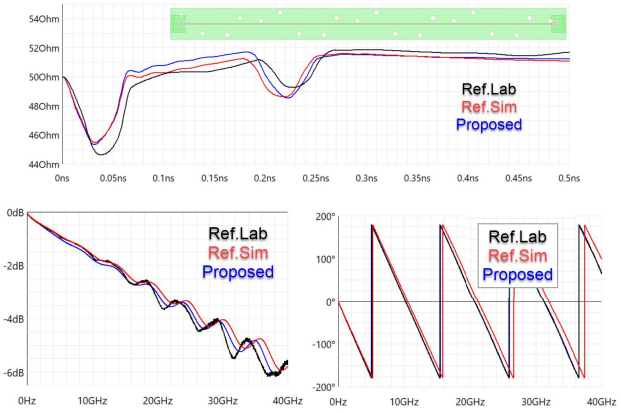

Fig. 4. Microstrip model, TDR impedance (top), Insertion Loss in dB (Left) and Insertion Loss angle (right).

For the microstrip example, using the suggested dimensions and material properties yielded an initial fair match with the reference measurements and simulation, including the difference in the insertion loss angle seen between reference measurement and sim with a higher than measured impedance in the Time Domain Reflectometry (TDR). Adjusting the dielectric constants from 3.4 to 3.58 to match the delay yielded a much better match from both insertion loss angle (delay) and impedance perspectives (Fig. 4). For this benchmark, the proposed solver results are characterized by a 4x speed up compared to a commercial EFIE based solver [8].

Fig. 5. Plasma package model, measured (left) and simulated (right) Far End Noise (Top) and Near End Noise (Bottom).

Excellent correlation for the Plasma package was achieved as can be seen in Fig. 5 both for amplitude and relative features of the Far End and Near End Noise.

In addition to the public domain benchmarks, we present in Fig. 6. Further Correlation with EFIE Solver comparisons showing how the proposed solver's results correlate with EFIE. In Table 1, significant speed up of the proposed method over existing methodology for most cases was achieved.

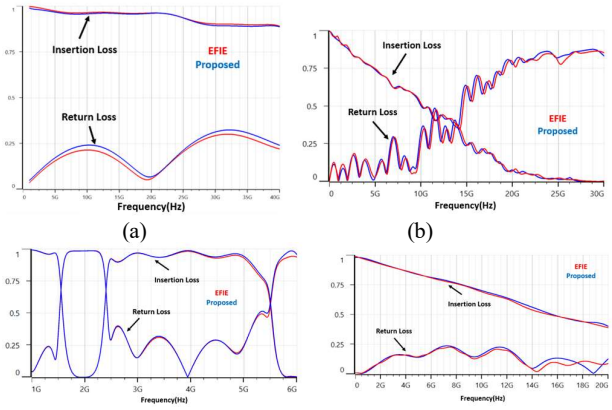

Fig. 6. Further Correlation with EFIE Solver.

TABLE 1. COMPARING PERFORMANCE OF PROPOSED METHOD WITH EFIE.

	Metal Layers	Ports	EFIE unknowns	Proposed unknowns	Speed up(%)
(a) Via transition	7	16	56792	31276	240
(b) Full channel	16	2	562224	172350	536
(c) RF filter	1	2	11374	3644	293
(d) Plasma Benchmark	10	40	897411	667355	112

IV. CONCLUSIONS

In this paper, we present a methodology to analyze multilayered PCB interconnects where reference planes are not explicitly meshed. We demonstrate the accuracy and performance benefit of the methodology by comparing it with commercial field solvers using EPS benchmark examples. Using this methodology, in addition to reducing the number of unknowns on the reference planes, we achieve several advantages over an EFIE formulation with explicit meshing of the reference planes.

- Since reference plane metal is modeled analytically it does not suffer from discretization error [9].
- When analyzing cropped portion of a PCB, it is important to suppress artificial resonances coming from the cropped cavity boundary. For boundary element implementation special methodology needed to approximate matching termination for the cavity [9][10], in this way, reference planes are modeled as infinite therefore the cavity resonance is naturally removed.
- This methodology naturally decomposes the vertical dielectric stacks into several decoupled regions. Thus, the cost to fill up the Green's function interpolation table [11] is significantly reduced.
- We achieve some sparsification of the system matrix, as J_1 does not interact with M_2 or J_2 in Fig. 2, this leads to further improvement in performance and memory.

Continued work includes further performance optimization of the proposed method by tuning the mesh for the traces, vias and void regions and additional steps towards improving the stability of the system matrix for better iterative solver performance.

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