Integral Equation-Based Solver for the Simulation of Integrated Circuit Packages

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***Abstract*—A full wave simulation using an integral equation-based solver on the IEEE plasma package benchmark problem [1] is performed. The integral equation approach offers advantages over traditional Finite-Element Method (FEM) solvers, as it uses a surface-based mesh and shows excellent efficiency for large-scale structures like IC packages. With its large amount of geometries, The benchmark is used as a test case to validate the full wave solvers on integrated circuits**

***Index Terms*—Packaging Benchmark Suite, Integral Equation Solver, Integrated Circuit (IC)**

I. Introduction

Computer chips and Integrated Circuits (ICs) play a pivotal role in modern technology, serving as the backbone of countless electronic devices. Their importance lies in their ability to process and store vast amounts of information swiftly and efficiently. Over the years, these chips have undergone remarkable advancements, with notably reduced dimensions and higher frequencies.

With clock speeds now reaching multiple gigahertz and component sizes shrinking to the single-digit nanometer scale, unintended electromagnetic effects like interference, susceptibility, coupling, and signal integrity loss have emerged. These effects have rendered traditional circuit-based modeling increasingly inaccurate, giving rise to a pressing demand for full-wave EM simulation solutions.

However, these solutions experience significant challenges in terms of scalability and the need for ensuring accuracy, particularly when examining high frequency effects. To this end, the IEEE plasma package benchmark [1] problem has emerged as a way to validate that both challenges are properly handled.

This article examines the use of an integral-equation based solver for running a full wave simulation on this benchmark package without the need for any geometrical partitioning or external domain decomposition [2].

II. IEEE Plasma Package Benchmark Problem

A. Origin

The plasma package benchmark problem is an 8 layer full package design containing over 40,000 geometrical elements (shapes) intended for use in research and industry to test new methodologies and tools. The benchmark problem includes design files of the full plasma package, as well as measured time domain data, a section of which is shown in figure 1.

Fig. 1. A small cut portion of the 3D geometry with dimensions 3.5 x 0.9 x 0.732mm. [3]

B. Usage

The use case outlined in this article for the plasma package comes from its ability to assist in the validation of EM solvers. It was originally developed in 2006 as a challenge problem with the intent of extracting 20 nets to run simulations on the relevant traces and compare it with the measured time domain data that is included in the package. [1] However, since this case was large to begin with, running full EM simulations with all 300 nets simultaneously still poses a substantial challenge

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to any software even with recent advances in computing power. A vector image of the full geometry is shown in figure 2 below.

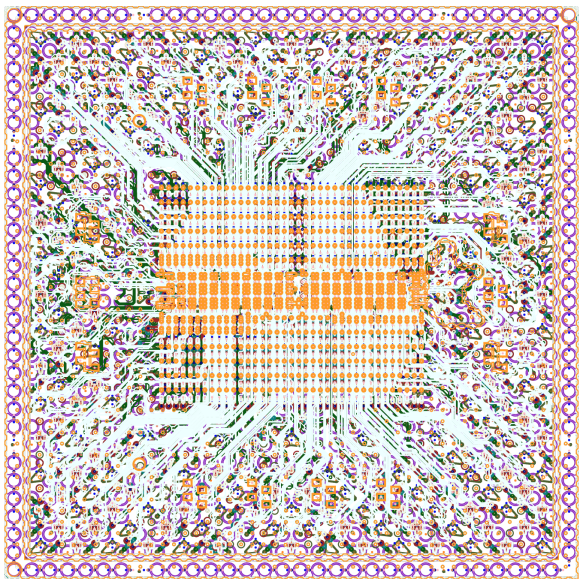

Fig. 2. The full geometry of the plasma package

III. Methodology

In IC package simulations, integral-equation (IE) electromagnetic field solvers are emerging as a promising alternative to the commonly used Finite-Element Method (FEM) based solvers. Our recent work focuses on utilizing this solver approach, which inherently exhibits excellent efficiency and accuracy for large-scale structures, a notable advantage for IC packaging problems. This section discusses the potential benefits of IE solvers and their methodology for modelling IC packages compared to FEM.

A significant differentiator between FEM and integral-equation solvers lies in their meshing techniques. FEM deploys a volumetric mesh, whereas IE solvers predominantly utilize a surface-based mesh of the interface between conductors and the dielectric substrate and between two dielectric surfaces. The surface mesh tends to produce orders of magnitude fewer unknowns for large-scale problems, thus augmenting the computational efficiency. In the case of the plasma package, the meshing generates approximately 3,000,000 unknowns. A small section of the generated mesh can be seen in figure 3.

The treatment of ports also varies between FEM and IE solvers. While FEM methods typically utilize wave ports attached to the package's bumps, we adopted implicit lumped ports between the signal pads and their corresponding ground pads. While deviating from standard practices, this approach aligns well with the IE methodology and matches measurements well, as shown in the next section. However, in general, the results from FEM and IE solvers may lead to slight discrepancies due to assumptions inherent to the model setup, including the configuration of the ports. These discrepancies must be considered and weighed against the solver's merits, particularly its proficiency in handling large-scale simulations.

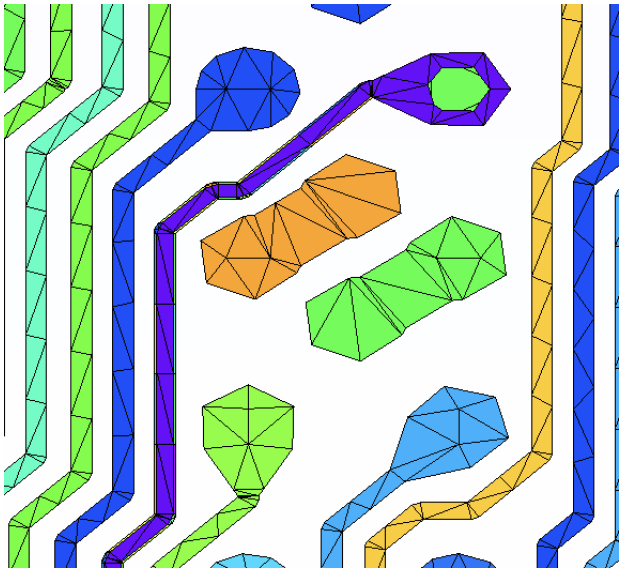

Fig. 3. Visualization of a surface mesh example of one metallic layer featuring traces and vias.

In this study, the IE solver operates in the frequency domain and employs compressed hierarchical expansions to store the system matrix. The compact matrix representation reduces the memory complexity from $O(N^2)$ to approximately $O(NlogN)$ and similarly accelerates computational speed. We utilized a reduced-order modeling technique to generate a pole-residue form of the S-parameters, adaptively sampling frequencies from the DC point (0Hz) to a pre-defined maximum.

A final consideration is that for simulation, the voltage source is in series with the source impedance, Device Under Test (DUT), and termination. During measurements, the input voltage measurement probe is placed after the source impedance and hence takes into account the drop across the source impedance. Source impedance and termination are equal, and assumed to be much higher than DUT impedance. Therefore, measured input voltage is multiplied by a factor of two when using as an input for time-domain simulations.

IV. Results

Using this IE solver, we conducted a frequency sweep from DC to 20GHz at 1GHz intervals to obtain S Parameters on the ports outlined in the benchmark package. We then interpolated these results to obtain Time Domain Transmission (TDT) and Time Domain Reflection (TDR) voltage data in order to compare it with available measured data. The wave forms show strong agreement. Results can be seen in the figures 4 and 5.

All simulations were conducted on a 16 core Intel Xeon E5-2686 processor with 128GB of available memory. The process of creating the geometry representation required 49 minutes, while the generation of S parameter solutions averaged 68 minutes per frequency.

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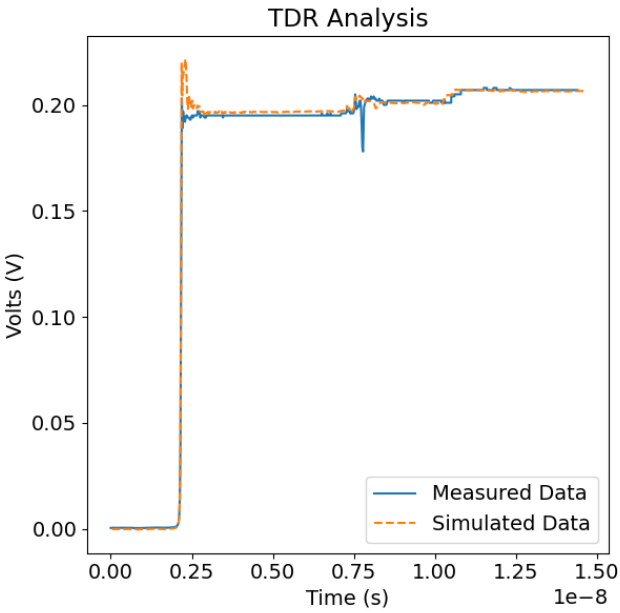

Fig. 4. A comparison of simulated and measured results with input waveform and outputs at the chip side of the package

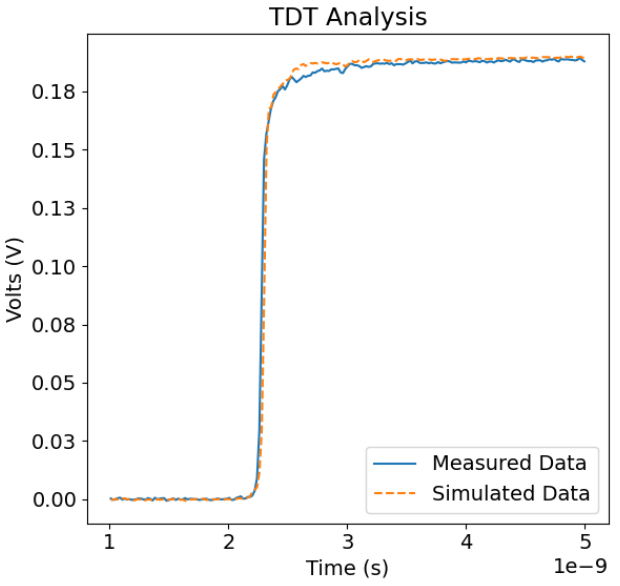

Fig. 5. A comparison of simulated and measured results at the BGA side of the package

V. Conclusion

Applying an IE-based solver with lumped ports and S-parameter pole residue interpolation to simulate IC packages introduces several benefits, particularly in computational efficiency and accuracy for large-scale problems with no partitioning or domain decomposition required. Results show very close agreement with measured data from the the IEEE plasma package benchmark problem.

VI. Acknowledgement

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References

[1] IEEE EPS Technical Committee on Electrical Design, Modeling and Simulation, 'Packaging Benchmark Suite', 2021 [Online]. Available: https://packaging-benchmarks.org/.

[2] Z. Peng, Y. Shao, H.-W. Gao, S. Wang, and S. Lin, "High-Fidelity, High-Performance Computational Algorithms for Intrasystem Electromagnetic Interference Analysis of IC and Electronics," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 7, no. 5, pp. 653–668, May 2017, doi: https://doi.org/10.1109/TCPMT.2016.2636296.

[3] E. Gjonaj, M. Perotoni, and T. Weiland, "Large Scale Simulation of an Integrated Circuit Package," 2006.