Signal Integrity Design and Analysis of Redistribution Layer Interposer Channel with Diagonal Meshed Ground in Memory Interface of High Bandwidth Memory

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Abstract— In this paper, we designed and analyzed redistribution layer (RDL) interposer channel with with diagonal meshed ground (dia-GND) in memory interface for high bandwidth memory (HBM). Therefore, the RDL interposer is emerged to solve cost and electrical performance. However, the RDL interposer memory channels have a critical signal integrity (SI) issue at high datarate. Specifically, RDL interposer channels with orthogonal meshed ground (ortho-GND) has impedance mismatch because of low channel capacitance which also causes severe overshoot voltage. To overcome this issues, we proposed dia-GND for RDL interposer channels. We analyzed SI of the proposed RDL interposer memory channels in the frequency and the time domain and compared with ortho-GND. As a result, it showed improved not only insertion loss (IL), return loss (RL) and crosstalk but also overshoot voltage which is improved 50% with dia-GND.

Keywords— high bandwidth memory (HBM); overshoot voltage; RDL Interposer; signal integrity (SI);

I. INTRODUCTION

Recently, development of artificial intelligence (AI) has required advanced HBM modules for high computing performance. The high bandwidth memory (HBM) has arisen as one of the promising solutions. The HBM which consists of 3D stacked DRAM achieves high bandwidth by integrated on silicon interposer which serves thousands of input/outputs (IOs) with fine pitch routing. However, the silicon interposer consists of through silicon via (TSV) which result in degrading electrical performance and increasing fabrication cost, respectively [1]. Therefore, to overcome this disadvantages, another type of interposer is required to achieve not only high electrical performance, but also fabrication cost reduction.

The redistribution layer (RDL) interposer emerges to mitigate those limitations of silicon interposer. The RDL interposer for HBM is depicted in Fig. 1. RDL interposer does not contain TSV and consists of one dielectric material which has low relative permittivity which are main difference compared to silicon interposer. This results in reducing fabrication cost and signal loss, respectively. Hence, researches for RDL interposer memory channels are actively have been



Fig. 1. The cross-section view of RDL interposer for HBM

conducted to verify the electrical performance [2], [3]. In those researches, signal integrity (SI) and overshoot voltage issues are caused at high datarate. Moreover, SI analysis were not conducted depending on the GND types. Because effective characteristic impedance which affects to SI can be changed according to the GND type, it is necessary to consider different GND type to tackle SI issue and the overshoot voltage.

In this paper, we proposed RDL interposer memory channel in the HBM with variance of topology of meshed GND for improved SI performance. Conventionally, the interposer used orthogonal meshed GND (ortho-GND). However, the variance of GND pattern should be considered because it causes a different channel characteristics and SI performance. Therefore, we designed diagonal meshed GND (dia-GND) for improving SI of RDL interposer memory channels. We analyzed RDL interposer memory channel with dia-GND in the frequency domain and the time domain and compared with ortho-GND. In the frequency domain, we analyzed insertion loss (IL), return loss (RL) and crosstalk. Furthermore, we conducted eye diagram simulation to analyze the overall frequency domain result in the time domain. As a result, it showed improved not only IL, RL



Fig. 2. Proposed design of RDL interposer for HBM

and crosstalk but also overshoot voltage which is improved 50% in the RDL interposer memory channel with dia-GND.

II. THE PROPOSED DESIGN OF RDL INTERPOSER MEMORY CHANNEL

We designed RDL interposer channels to have 5 metal layers with 2 signal layers by considering HBM 3 micro-bump ball map. Fig. 2 and Table I represent the proposed design of RDL interposer, and its martial properties. Metal 2, 4, 5 layers were used for power or GND of IO interfaces. Metal 1 and 3 layers were utilized as signal layers. Those proposed design employed microstrip line (ML) and strip line (SL) structure, which are suitable for the interconnection of thousands of IOs [4]. The polyimide was used for dielectric material of RDL interposer due to its lower relative permittivity than dioxide which is used for silicon interposer [5].

TABLE I Physical Dimension and Material Properties of RDL Interposer

Parameters	Symbol	Value		
Channel	W_{ch}/S_{ch}	2/2µm		
width/Space		•		
Channel Length	$l_{\rm ch}$	5mm		
Metal(M1-M5)	tah	2um		
Thickness	C CII	2µ111		
Distance to GND	$d_{ m gnd}$	1µm		
Relative	CDI	3 35		
permittivity of PI	CPI	5.55		
Loss tangent of PI	$tan \delta_{ m PI}$	0.012		
Conductivity of Cu	$\sigma_{ m Cu}$	5.8x10 ⁷ S/m		

Fig. 3 shows two types of GND which were designed to conventional ortho-GND and dia-GND. We designed that memory channel had a same width of perforated region at the middle of the GND to consider only effect of GND pattern. Moreover, we designed that both width and space of meshed GND are 5 μ m and maintained the metal density as 75 % [6]. This design made memory channels of dia-GND were more aligned with GND than ortho-GND. Therefore, we can expect capacitance of memory channels can be higher and inductance can be lower in case of dia-GND.

III. SIGNAL INTEGRITY ANALYSIS OF RDL INTERPOSER MEMORY CHANNEL DEPENDING ON THE GND TYPES

In section III, we analyzed the RDL interposer memory channel with the dia-GND and compared with ortho-GND. Because the different types of GND cause the different



Fig. 3. Two types of GND which are (a) ortho-GND and (b) dia-GND.

effective characteristic impedance of memory channel, we analyzed the effect of the different GND type in both frequency domain and time domain.

A. Signal Integrity Analysis in the Frequency Domain

Fig. 4 shows IL, RL and crosstalk with 16 Ω termination depending on the GND types because HBM 3 memory channel uses 16 Ω termination at driver [7]. The detail of driver set-up is stated in sub-section B. IL and RL are represented in Fig. 4(a) and (b). For ML with dia-GND, IL was slightly higher than ML with ortho-GND at Nyquist frequency. On the other hand, RL of ML with dia-GND was lower than that of ML with ortho-GND. By using the equation (1) and Table II, we can analyze IL and RL results. Characteristic impedance (Z_0) and resistance (R), inductance (L), capacitance (C), conductance (G) is represented at the equation (1). Furthermore, Table II shows RDL interposer memory channel RLGC, mutual inductance (L_M) and capacitance (C_M), and effective characteristic impedance (Z_0) for both of GND types. Higher R and L, and lower G, C for ML with ortho-GND caused higher Zo which results in worse reflection due to impedance mismatch than ML with dia-GND. Therefore, the reason of degraded IL and RL for ML with ortho-GND is worse impedance mismatch. In case of SL, it has a same tendency for IL and RL because of worse impedance mismatch.

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \left[\Omega\right] \tag{1}$$

Fig. 4(c) and (d) represent the near-end crosstalk (NEXT) and far-end crosstalk (FEXT) of ML for both of GND. From the equation (2) and (3), NEXT and FEXT is represented by L, C and L_M, C_M. Additionally, FEXT is related to memory channel length (l), wave velocity (v) and rise time (t_{rise}). However, this values are constant in simulation because datarate is fixed. Hence, we consider the L, C and L_M and C_M.

$$NEXT = \frac{1}{4} \left(\frac{C_M}{C} + \frac{L_M}{L} \right) \tag{2}$$

$$FEXT = \frac{1}{2} \left(\frac{l}{v * t_{\text{rise}}} \right) \left(\frac{C_M}{C} - \frac{L_M}{L} \right)$$
(3)

For ML with dia-GND, NEXT and FEXT are smaller than ML with ortho-GND at Nyquist frequency. Because not only the ratio of C_M and C but also L_M and L are decreased for memory channel of dia-GND. This tendency is also represented in SL. Furthermore, SL for both of GND types has small NEXT and FEXT results than ML. Since L_M and C_M are largely decreased,



Fig. 4. (a) IL, (b) RL, (c) NEXT, and (d) FEXT of the ortho-GND and the dia-GND

TABLE II EXTRACTED RLGC PARAMETERS OF RDL INTERPOSER MEMORY CHANNEL DEPENDING ON THE GND TYPES

		R	L	L _M	С	См	G	Zo
		$[\Omega]$	[nH]	[nH]	[pF]	[pF]	[mS]	$[\Omega]$
ortho-	ML	19.7	1.36	0.09	0.43	0.43	0.02	48.4
GND	SL	16.8	1.04	0.03	0.81	0.26	0.04	44.0
dia-GND	ML	18.7	1.22	0.07	0.50	0.41	0.02	47.2
	SL	15.6	0.92	0.02	0.92	0.24	0.05	42.4

electromagnetic coupling is reduced in SL which results in improving crosstalk.

B. Signal Integrity Analysis in the Time Domain

We also conducted eye-diagram simulation in the time domain for analysis of RDL interposer memory channel depending on the GND types at 6.4Gbps. Fig. 5 represents the simplified eye-diagram simulation set-up based on nominal current of I/O driver in HBM3 JEDEC standard [7]. In Fig. 6, the overshoot voltage of ML was worse than that of SL because RL and crosstalk were severe in ML along the overall frequency. Moreover, compared to Fig. 6(a) and (b), the overshoot voltage for ML and SL of ortho-GND was more degraded than that of dia-GND because of reflection and crosstalk. The overshoot voltages were 19.25% of V_{DD} for ML and 7.75% of V_{DD} for SL. On the other hand, those of dia-GND 16.5% of V_{DD} for ML and 3.75% of V_{DD} for SL. Because not only the difference between impedance and termination but also crosstalk is small in the dia-GND case, low overshoot voltages are represented in the eye diagram for memory channels with dia-GND. As a result, the overshoot voltage is improved 14.28% and 50% in ML and SL with dia-GND.

IV. CONCLUSION

In this paper, we analyzed RDL interposer memory channel with proposed dia-GND compared with conventional ortho-



Fig. 5. The simplified model of set-up to simulate eye diagram for singleended channels



Fig. 6. The eye diagrams of ML and SL for (a) ortho-GND and (b) dia-GND

GND. In the frequency domain, IL, RL and crosstalk were analyzed depending on the GND types. IL, RL and crosstalk were improved in ML and SL with dia-GND because of enhanced impedance mismatch with L_M and C_M . Nevertheless, in the time domain analysis, overshoot voltage emerged in ML and SL with the both GND types. With the proposed dia-GND, the level of overshoot voltage was dramatically decreased. This is because of well-matched impedance and decreased crosstalk effect with the proposed dia-GND. Consequently, overshoot voltage is decreased by 14.28% and 50% in ML and SL with the proposed dia-GND.

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REFERENCES

- You, Se-Ho, et al. "Advanced fan-out package SI/PI/thermal performance analysis of novel RDL packages." 2018 IEEE 68th Electronic Components and Technology Conference (ECTC). IEEE, 2018.
- [2] Jang, Jae-gwon, et al. "Advanced RDL interposer PKG technology for heterogeneous integration." 2020 International Wafer Level Packaging Conference (IWLPC). IEEE, 2020.
- [3] Jeng, Shin-Puu, and Monsen Liu. "Heterogeneous and Chiplet Integration Using Organic Interposer (CoWoS-R)." 2022 International Electron Devices Meeting (IEDM). IEEE, 2022.
- [4] Cho, Kyungjun, et al. "Design optimization of high bandwidth memory (HBM) interposer considering signal integrity." 2015 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS). IEEE, 2015
- [5] Sitaraman, Srikrishna, et al. "Optimization of 2.5 D Organic Interposer Channel for Die and Chiplets." 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC). IEEE, 2022.
- [6] Cho, Kyungjun, et al. "Signal integrity design and analysis of silicon interposer for GPU-memory channels in high-bandwidth memory interface." *IEEE Transactions on Components, Packaging and Manufacturing Technology* 8.9 (2018): pp. 1658-1671
- [7] High Bandwidth Memory (HBM) Dram, Standard JESD238, 2023