A Comprehensive Methodology for Optimizing Power Integrity of High-Performance IC Packages

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***Abstract*— With semiconductor technology scaling down to 5nm node, more stringent requirements have been raised to power delivery network (PDN) design in integrated circuits (IC) on silicon, package, and board. On package level, the design challenges include DC IR drop control, balancing current distribution on package, limiting maximum current per ball grid array (BGA) ball and AC noise optimization. In this paper, key aspects of power delivery network (PDN) design challenges with Field-Programmable Gate Array (FPGA) packages and enablement solutions are presented.**

Package routing optimization method for reducing IR drop and, re-balancing current distribution as well as AC noise control are demonstrated in this paper.

Keywords—power integrity, power delivery network, IR drop

I. Introduction

Development of optimum power delivery network (PDN) has been increasingly critical in CPUs, field programmable gate arrays (FPGAs), and AI platforms which demand intensive computing, signal processing and high data communication rate, ultra-low power, etc. [1][2] When supply voltage is decreasing in sub-5nm CMOS, it is critical to design high-performance PDN network to ensure that network provides enough power supply to all transistors with certain noise margin for all possible operations [3]. If voltage seen at the CMOS node decreases too much due to DC voltage IR drops and AC noise, the IC may have timing issues such as setup/hold violations; and in extreme cases, when voltage falls below threshold, it leads to chip functionality failure [4][5].

Alongside with silicon development, advanced packaging technologies, such as Intel's Embedded Multi-die Interconnect Bridge (EMIB) technology is developed for high-density electrical connections and for high-speed communications between heterogeneous silicon in the same package. To leverage EMIB, importance of signal integrity (SI) and power integrity (PI) design on package is emphasized to guarantee undistorted signal and optimum power supply to multiple chips on package [6].

Thereby it imposes more stringent specs including low voltage IR drop, AC noise, fast pull-up/down response time, etc. Recently, researchers and IC designers have put endless efforts to ensure minimal DC IR drop and clean-of-AC noise power supply to transistor cells.

In this paper, we presented a comprehensive methodology to perform DC IR drop, maximum current per package BGA ball and AC noise analysis on high-performance compact IC packages.

II. DC Voltage IR Drop And Current Analysis

A. Power Network and Decoupling Capacitors

As depicted in Fig.1, a common platform comprises of voltage regulator module (VRM), PCB board, package, and ICs, together with various de-coupling capacitors. VRM is the source of the power supply, and it always has bulk decoupling capacitors in its vicinity to provide enough charge to power supply and filter out noises to the ground. After power takes off from VRM, it first travels through PCB power rails with on-board decoupling caps, and in nowadays cost-effective designs, several power rails are combined on board, therefore, on-board de-caps may be selected to be functional for different functions. Therefore, we may notice large number of board de-caps with different values from pF to several thousand of μF. Package is in between PCB and silicon, with ball grid arrays (BGA), signal/power routing layers, through vias and bumps.

Commonly used package and PCB capacitors are ceramic capacitors (commonly called MLCCs). On-die capacitors include metal-oxide-metal (MOM) capacitors, metal-insulator-metal (MIM) capacitors, or deep trench capacitors, etc. [1] Recently, Intel's advanced Super-MIM technology brings higher density to the capacitor development on silicon, which delivers up to 5 times of regular MIM capacitance density within same silicon area.

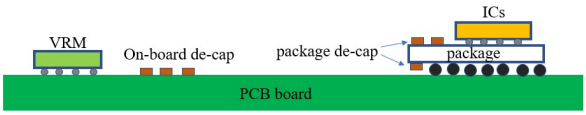

Fig. 1. Package and FPGA Die Structure

B. DC Voltage IR Analysis

Demonstrated in Fig. 2 is an equivalent circuit model representing PDN that can be decomposed of three blocks: voltage regulator module (VRM), PCB, package, and ICs current sinks. In ideal systems, VRM can deliver power to IC with minimal loss; however, in an actual design, each section

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will include resistive, inductive components, where resistive component generating DC IR drop and inductance causing AC noise. System voltage IR drop is directly calculated in (1)

$$\Delta V_{IR} = R_{system} \times I_{drawing} \quad (1)$$

where ΔV_{IR} is the induced voltage drop through the power supply from VRM to silicon die C4 bumps; R_{system} is the path parasitic resistance consisting of PCB, package, interposer power plane, trace and vias as shown in Fig. 2.; $I_{drawing}$ the current drawn by the silicon current sink.

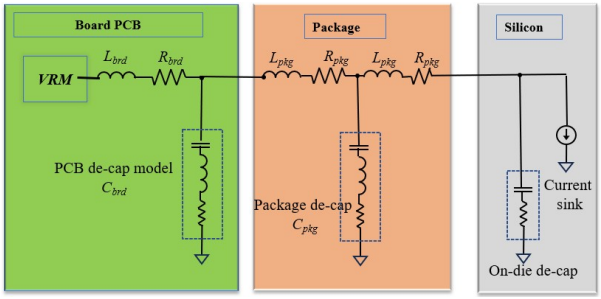
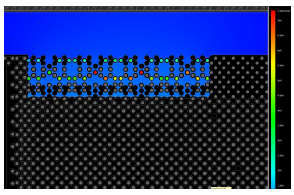
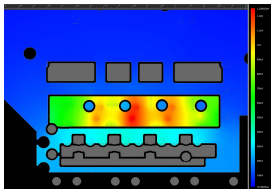


Fig. 2. power delivery network (PDN)

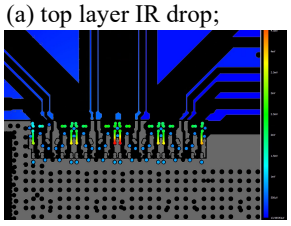
The non-ideal PDN network's inherent parasitic resistance is the reason of DC IR drop development, as the components shown as R_{brd}, R_{pkg} and R_{die} in Fig. 2.

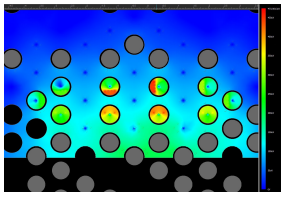


(a) top layer IR drop;



(b) plane below core layer;





(c) connect trace above core;(d) VRM BGA on bottom layer;

Fig. 3 IR drop distribution on key layers of package.

In this paper, the DC IR drop on the package due to $R_{package}$ is analyzed. The voltage drop is characterized for one analog power rail, as illustrated in Fig.3. PowerDC tool is used for simulation, where current sink is set up at the 36 package bumps with equal current distribution and VRM set up at the 10 BGA balls. From color indication information in Fig. 3(a), 2 bumps (with deep red color) have worst voltage drop of 7.31mV and 7.29mV below nominal voltage on the BGA ball, which are both within 1% spec of 7.8mV. The current package layout routing of this power rail satisfies the IR requirement in this study. However, in many designs, because of number of power rails, signal channels and ground plane requirement, there is not enough space for a perfect power rail plane or enough number of power vias. In such scenarios, it is required to balance all rails and sacrifice some non-key rails' performance to meet the specification.

C. Maximum DC current per package ball

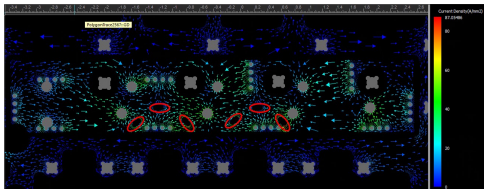
IC Packages have a designated specification for maximum current through its BGA ball. The max current is limited to the spec under all usage circumstances, otherwise, the BGA ball may be damaged resulting in failure of IC. In this package technology, the max current per ball can reach up to 1.5A, meaning no higher current is allowed to pass through any BGA under worst usage cases.

When in initial designs, more current goes through several balls than others, we may notice unbalanced current distribution among the BGAs, which may result some failing max current spec. To get current flowing map, it is straightforward to obtain the current density first [4]. From Maxwell's equation, the current density $\boldsymbol{J}$ in a conductor is defied as

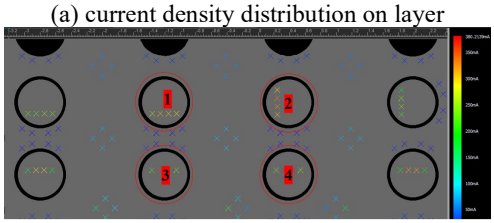
$$\boldsymbol{J} = \sigma \boldsymbol{E} \quad (2)$$

where σ is electrical conductivity of conductor and $\boldsymbol{E}$ the electric field.

Using power simulation tools, such as PowerSI or SIWave, it is straightforward to obtain current density with flowing directions on each layer with knowledge of voltage supply value and total current. Therefore, one effective way of rebalancing the current distribution is purposely adding voids to block current flowing into worst BGAs, as the 6 voids in Fig. 4(a). On the current flowing path, such void disturbs current density distribution and guides current to flow from hot spots to other vias and finally balance current distribution on BGAs. In this design example, a total current of 14.05A is added at the bumps side as current drawing. Fig. 4(b) is an illustration of BGA current after the rebalance, where the worst 4 BGAs have current value of 1.14A (ball 1), 1.23A (ball 2), 1.17A(ball 3) and 1.23A(ball 4), all of which are well below 1.5A specification.



(a) current density distribution on layer



(b) max current per BGA ball

Fig. 4 Current per ball and current desity analysis.

III. Power Supply AC Noise Analysis

Modern ICs require different low voltage supply rails to supply large quantity of logic cells, input/output circuits, transceivers, and memory, etc., [6] each with its own voltage and current specifications based on noise requirements. Therefore, after the DC performance is optimized to meet design specs, a comprehensive frequency domain AC noise analysis is necessary.

In frequency-domain analysis, all resistance, inductance and capacitance of major PDN components are modeled to create the PDN impedance profile.

In an accurate modeling of PDN, the frequency spans from DC up to several GHz to cover the frequency components from VRM, PCB, package and die interconnects. VRM and its bulk capacitors have impact within 1MHz to several MHz; PCB inductance and capacitors mainly manifest below tens of MHz; package inductance, on-package decoupling caps are most influential up to several hundred MHz; while on-die decoupling capacitors dominate higher frequency range up to several GHz [6].

In recent design procedure, there are several commercial electromagnetic (EM) tools such as Cadence PowerSI, Ansys Electronics to conduct full EM solving and extract S-parameters model of the package and PCB layout structure within a frequency range of DC to interested high frequency. This model includes VRM port at BGA side, current sink port at package bumps side, and on package capacitors ports at the actual OPD locations on package. After model extraction, system simulation tool such as HSpice or Keysight ADS is deployed for system performance. As mentioned earlier, placing on-package decoupling capacitors are effective method to reduce the power impedance profile. Fig. 5 is a demonstration of efficacy of on-package decoupling capacitor (OPD) with sweeping values from 10nF to 1uF, which gives a direct demonstration of how 10nF OPD reduced the peak impedance from 4.5ohm at f_3 of 135MHz to 3.2ohm at f_4 of 150MHz. The impedance profile of package inductance and 10nF intersects in vicinity of f_2 of 102MHz as a valley on 10nF's trace, therefore, impedance can be dragged down for a better power supply. With 22nF OPD, we note the intersection point at 58MHz, not close enough to the main peak at f_3; and with higher values, the frequency is moved to even lower end, rendering OPD not as effective, as the 100nF, 470nF and 1uF traces.

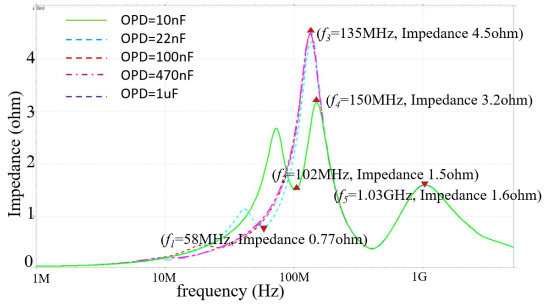


Fig. 5. Frequency domain impedance profile with different on-package capacitor values

To verify the noise effects in actual application scenario, one analog power rail of 0.78V supply voltage is applied, lumped RLC model is applied for PCB and die, and extracted s-param model for the package. An actual usage current ICCT profile is applied to the silicon current sink, where chip logic elements are switching on or off simultaneously, thereby drawing tremendous current within short period of time.

Fig. 6 plots the simulated supplied voltage waveform at C4. When large current is pulled up instantaneously on at t_1, the power supply cannot supply enough charge immediately, forming the 1st droop as seen at 777.5mV position. Then package decoupling capacitors start to function, and we can see the voltage gradually pulls up to its nominal value at time t_2. The AC noise peak-to-peak value measured at power rail C4 bump is 14mV (1.8% of 780mV nominal value), which is within the spec of 3%. It is noted that the high frequency noise components with the power supply after t_2 is due to the high-frequency switching activities of logic cells and cannot be eliminated by using on-package decoupling capacitors. Even with the high-frequency noise included, the AC noise is still below 3% spec, proving the well optimized package power network.

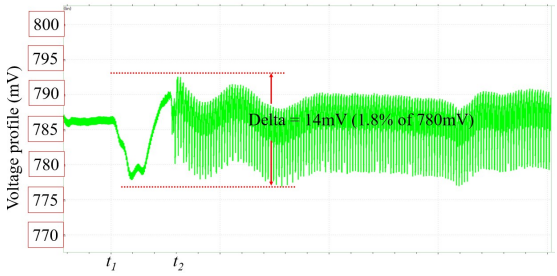


Fig. 6. AC noise probed at C4 bumps on package.

IV. CONCLUSIONS

In this paper, a comprehensive methodology of optimizing PDN in DC and AC domain is proposed. The methodology is used for DC maximum current per ball, IR drop optimization, and simultaneously meeting AC noise specifications. Implementing current voids helps DC performance, and using OPDs effectively reduces impedance profile peak and AC. The procedure presented in this paper can be universally applied to optimize power networks on compact high-performance IC packages.

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