Signal/Power Integrity Co-Simulation of Die-to-Die Interface Customized for Augmented Reality

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***Abstract*— There is a rising demand for customized accelerate-and-compute hardware in emerging augmented reality (AR) and virtual reality (VR) wearables to enable the next generation computing platforms. Customized die-to-die interconnects, critical in heterogeneous system integration, provide significant flexibility in architecture definition and efficient data transfer with potential power advantage. Although custom silicon (and heterogeneous design) is crucial to meet key performance indicators such as power/performance, thermal envelope, and miniscule form factor in AR devices, it poses challenges for robust system design particularly in the context of high-speed signal integrity (SI) and power integrity (PI) considerations. To address these unique challenges, accurate signal and power integrity co-simulation is critical to ensure intact system performance. This paper highlights SI/PI co-simulations required to address the unique challenges applicable to custom die-to-die interface for AR/VR devices.**

Keywords—augmented reality, chiplet, die-to-die interconnect, SI/PI co-simulation.

I. Introduction

The rising demand for all-day wearable augmented reality (AR) devices with a socially acceptable form factor mandates customized hardware to satisfy key performance indicators such as minimal industrial design (ID), thermal envelope, and power/performance/area, all of which pose various challenges to robust system design and integration [1]. Trending away from traditional monolithic system-on-chip (SoC) design, a converging solution to address above-mentioned challenges is to adopt heterogeneous design which consists of integration of base-die (application processor) and chiplets (co-processors), using some form of die-to-die interface. In the past few years chip design industry has been leaning heavily towards heterogeneous integration and this new paradigm not only facilitates efficient and scalable modular designs with more flexibility, but it also mitigates issues around high cost and low yields of smaller (more advanced) process nodes [2]. As such, to design and implement robust custom (or standardized) die-to-die interconnect, accurate noise and jitter characterization of high-speed interfaces become increasingly critical [3]. In general, die-to-die interfaces take advantage of very short channels to connect (either laterally or vertically) two dies inside a package to yield higher bandwidth efficiency and low latency. As heterogenous technology continues to mature, the need for die-to-die interfaces becomes even more evident in variety of electronic systems. As it relates to this paper, a die-to-die interface typically consists of a PHY and a controller block which offers a seamless connection between the internal interconnect fabric on two dies. The PHY is typically implemented using a high-speed SerDes architecture or high-density parallel architecture, which are optimized to support various advanced 2D, 2.5D, and 3D packaging technologies loaded with high-density and closely coupled signal lines as well as power tracks. Such highly dense and noise-prone channels complicate reliable data and power transfer; hence it is crucial to accurately model and co-simulate both signal and power to predict the overall system performance. This paper highlights the SI/PI analysis required to address unique challenges of the die-to-die design for AR/VR devices, including all non-ideal effects such as inter-symbol interference (ISI), crosstalk, simultaneous switching noise (SSN), as well as power distribution network (PDN) noise, and their contribution to the overall system timing budget. Finally, the paper emphasizes the significance of identifying and addressing critical SI/PI components in designing custom silicon solutions for AR/VR wearables.

II. SI/PI Co-Simulation Methodology

Although die-to-die interface enables high-density on-chip interconnection, careful attention is required to address potential SI/PI issues caused by tight coupling among signal nets and power traces. For instance, as the number of on-chip signals increases, bump pitch becomes smaller which leads to stronger coupling between signals and power nets that requires to co-simulate both signal and power traces to accurately capture channel's and PDN's contribution to the overall link performance. This requires including all non-ideal effects such as ISI, crosstalk, impedance mismatch, PDN noise, and SSN [4]. To achieve this goal, in this paper transistor-level spice netlists are used to model both transmitter (TX) and receiver (RX) of the single-ended source-synchronous parallel die-to-die interface. Channel models are extracted and converted to spice models for

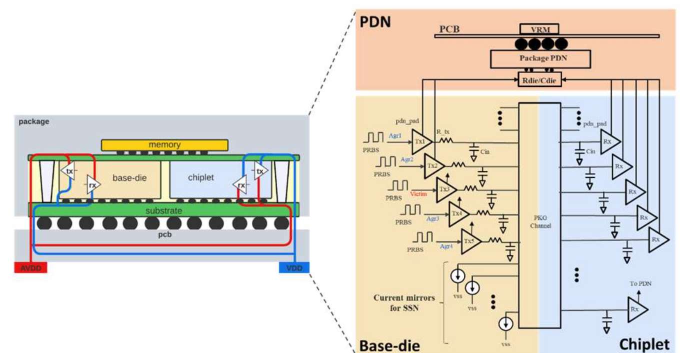

Fig. 1. Conceptual block diagram of SI/PI co-simulaion setup.

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simulation accuracy. Then, relevant PDN models are attached to the victim and all aggressor drivers to enable capturing SSN. Finally, end-to-end link co-simulations are performed, and transient eye diagrams are generated to verify the interface compliance and quantify channel's contribution to the overall timing budget. The remainder of this paper describes the modeling process in more detail.

A. End-to-End Simulation Setup

Figure 1 shows the conceptual block diagram setup supporting SI/PI co-simulations for a package-on-package (PoP) design. A victim TX is surrounded by ×4 crosstalk aggressors, all of which are modeled with transistor-level circuits. Since using the full transistor-level models for SI/PI simulations is time-extensive and computationally expensive, current mirrors are used to model the remaining drivers in which the current consumption from the full-model drivers is captured and scaled to represent SSN aggressors. Additionally, PDN subsystems including voltage regulator module (VRM), board, package, and on-die decoupling capacitors are attached to the power pins of both TX and RX blocks.

Regarding victim and aggressor assignment for channel analysis, it should be noted that while channel's ISI manifests itself as energy loss at the end of the link, worst-case crosstalk is captured by considering surrounding drivers/bumps/pins coupling in the victim line and corresponding termination conditions. As indicated in Fig. 2a, the PRBS pattern stimulates victim driver while the same (but out-of-phase) pattern is used for crosstalk aggressors (Fig. 2b). To stress the PDN, SSN drivers are switched in-phase and at the same time at the highest valid switching frequency (Fig. 2c). Finally, SSN drivers are modulated at the PDN's resonant frequency to generate the worst-case SSN plus PI stress patterns, as shown in Fig. 2d.

To capture the entire link's contribution to jitter, all the critical blocks from TX (pre-driver and driver) to RX (input buffer and sampler) are included in the analysis. Using such low-level models allows for internal probing and characterizations (e.g., TX driver strength optimization, RX sensitivity analysis) of the system that may not be feasible with traditional behavioral models. Table I summarizes the configuration, stimulus, process, voltage, temperature conditions, and the models used in the simulation for each test case.

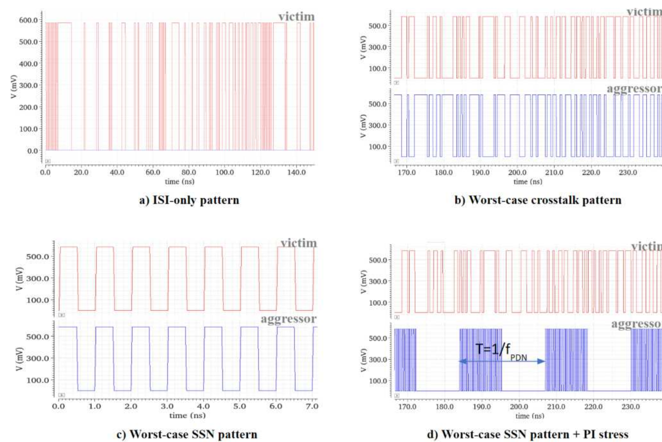

Fig. 2. Victim and aggressor stimulus patterns.

TABLE I. SIMULATION SETUP

Test	*Setup & Stimulus*	*Models*
ISI-only	victim (x1): prbs15 aggressor (x4): quiet ssn driver: none PI stress: none	tx: spice netlist pkg: s-parameter rx: spice netlist pdn: ideal
ISI+crosstalk	victim (x1): prbs15 aggressor (x4): prbs15 ssn driver: none PI stress: none	tx: spice netlist pkg: s-parameter rx: spice netlist pdn: ideal
ISI+crosstalk+ SSN+PI stress	victim (x1): prbs15 aggressor (x4): prbs15 ssn driver: 25 drivers PI stress: modulated ssn	tx: spice netlist pkg: s-parameter rx: spice netlist pdn: vrm+pcb+pkg+die

B. Power Distribution Network

To perform accurate SI/PI co-simulation, system-level (i.e., board, package, chip) PDN models need to be separately extracted, concatenated, and then connected to the power pins of active circuits in the simulation testbench. Figure 3a indicates system PDN components, and Figs. 3b-c illustrate the impedance profiles of both base-die and the chiplet consisting of lumped models of board, worst-case package, and on-die capacitance (both metal-insulator-metal and device capacitors). Since both base-die and chiplet PDNs are routed in a relatively symmetric fashion (refer to Fig. 1), similar in-package and on-die path impedance are observed from chip standpoint at mid- to high-frequency range, while the impedance kept low at lower frequencies to avoid board decoupling capacitors given the tight form factor for AR devices. The resonant frequency of the PDN is used for modulation of SSN aggressors to excite the worst-case PI pattern as described earlier.

III. SIMULATION RESULTS

Once all SI and PI components of the link are integrated, the transient simulations were performed to measure the eye diagram margins against the pre-defined eye mask @0.8UI, +/-60mV at RX pad and after the level-shifter, quantifying end-to-end channel jitter. Figures 4a-c show the eye diagram simulations (for the test cases listed in Table 1), and their contribution to channel margin loss by incremental addition of the non-ideal effects. It can be inferred from the graphs that by adding non-ideal effects, through manipulating the stimulus patterns and channel configurations, channel margin loss

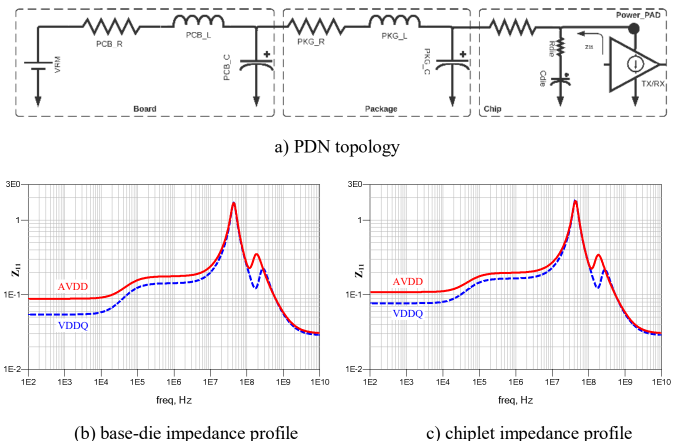

Fig. 3. Power distribution network.

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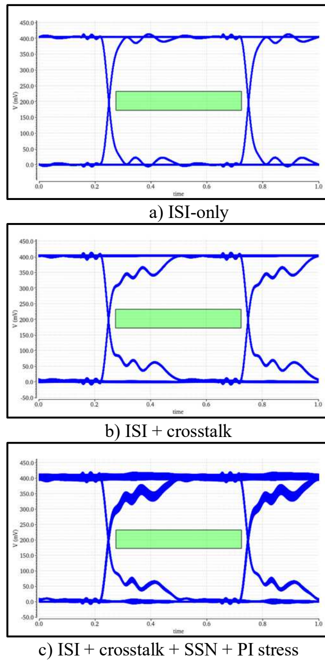


a) ISI-only

b) ISI + crosstalk

c) ISI + crosstalk + SSN + PI stress

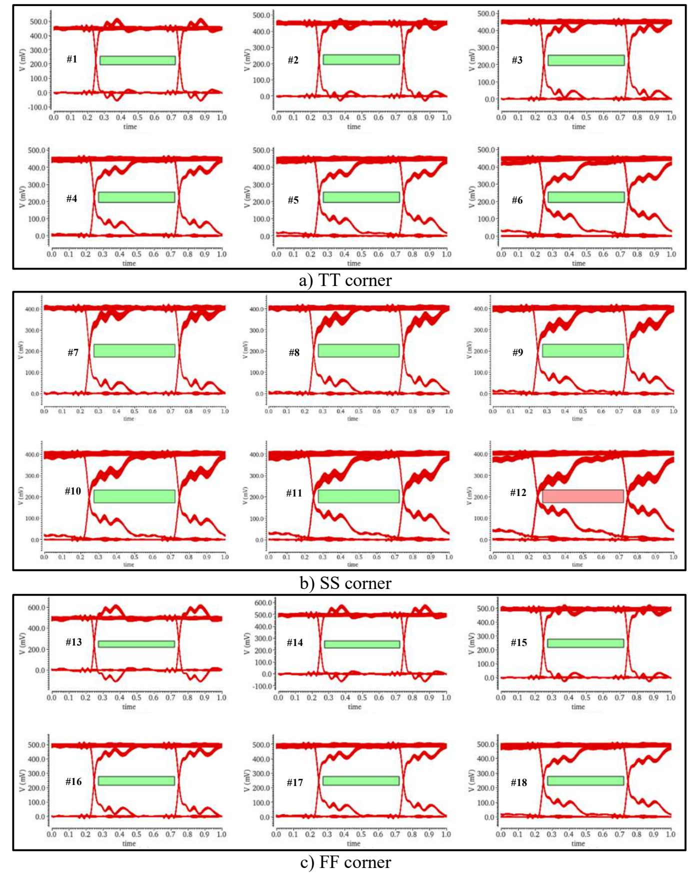
Fig. 4. Transient eye diagrams.

increases, and the maximum loss occurs when all the non-ideal effects are present in the system. Although channel margin loss difference may not be significant (between 1%-2% UI), one should recognize that for higher data transfer rates under more stringent conditions, the contribution of SSN and PI stress to the overall timing margin of the link can be more pronounced.

In addition to quantifying channel's contribution to the timing budget, SI/PI co-simulations can also be leveraged to perform what-if analysis to characterize the driver and optimize the allowable driver strengths or to study the robustness of the design to process variations. Figure 5 shows the results of RX sensitivity to a subset of PVT corners at different driver strengths as listed in Table II. As can be seen from the eye diagrams (tests #13, #14), although very strong driver strengths at fast corner cases pass eye mask comfortably, they may violate overshoot specifications and cause reliability issues. On the other hand, using very weak driver strengths (test #12) causes eye closure and data transfer failure. These kinds of analysis are important at the early stages of the design and should be performed to inform the design team, for example, to optimize calibration algorithms early in the design process.

IV. CONCLUSIONS

This paper emphasizes the significance of SIPI co-simulation for die-to-die interfaces in the design of high-performance/low-power wearables in the AR/VR space. It was shown that by accurate transistor-level simulation of signal and power integrity, including non-ideal effects, such as inter-symbol interference, crosstalk, and simultaneous switching noise, system designers can ensure the overall system's performance is met. The co-simulation approach allows for the identification of critical SI/PI components early in the design process which supports the designers in building and optimizing customized silicon solutions that meet the demands of all-day wearable AR/VR devices.



a) TT corner

b) SS corner

c) FF corner

Fig. 5. RX sensitivity across PVT and driver strength.

TABLE II. RX SENSITIVITY ANALYSIS

Test	***PVT***	***Driver***	***Test***	***PVT***	***Driver***
#1	tt/0.65/0.45/25	very strong	#10	ss/0.585/0.40/-40	moderately weak
#2	tt/0.65/0.45/25	strong	#11	ss/0.585/0.40/-40	weak
#3	tt/0.65/0.45/25	moderately strong	#12	ss/0.585/0.40/-40	very weak
#4	tt/0.65/0.45/25	moderately weak	#13	ff/0.715/0.49/105	very strong
#5	tt/0.65/0.45/25	weak	#14	ff/0.715/0.49/105	strong
#6	tt/0.65/0.45/25	very weak	#15	ff/0.715/0.49/105	moderately strong
#7	ss/0.58/0.40/-40	very strong	#16	ff/0.715/0.49/105	moderately weak
#8	ss/0.58/0.40/-40	strong	#17	ff/0.715/0.49/105	weak
#9	ss/0.58/0.40/-40	moderately strong	#18	ff/0.715/0.49/105	very weak

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