Signal and Power Integrity Design of Advanced Interface Bus (AIB) for FPGA Packages

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Abstract*— Advanced Interface Bus (AIB) is a die-to-die interface that connects chiplets or tiles of different functions in a single package through organic package substrate (AIB-O) or Silicon-based Embedded Multi-die Interconnect Bridge (EMIB). In Intel heterogeneous SiP (System in Package) products, AIB is widely used to connect the peripheral dies and the FPGA logic die for flexibilities of tile reuse and integration of different process nodes. Comparing to the monolithic package integration, the challenges with interconnecting different dies through AIB while keeping performance and power close to what would be possible with monolithic solution need to be addressed. These challenges include crosstalk, multi-reflection, power delivery noise, hence the reduced timing margin. In this paper, we investigated the signal integrity, power integrity and architecture optimization of AIB-O. With the proposed novel clocking scheme and power sharing strategies, as well as the trade-off of horizontal/vertical cross talk through optimized bump planning, and effective removal of pessimism in channel jitter, we were able to make the system margin sufficient to enable our new product solutions that meet the cost and performance targets.

Keywords— Signal and Power Integrity (SIPI), die disaggregation, die-to-die, timing margin, crosstalk, Advanced Interface Bus (AIB), Power Supply Induced Jitter (PSIJ)

I. Introduction

Die disaggregation (DD) paves a way to reduce the die size, and to improve the product yields with known good die integration. AIB, as one of the die-to-die interconnects in the die-disaggregation, is widely used in FPGA applications in Intel. This interface uses high-density IO to connect FPGA die to its peripheral dies through either EMIB or package substrate. The challenges come from the high IO signal density at the silicon and package sides, and the associated ISI and crosstalk that impacts the timing on one hand, and on the other hand the greater part of the timing margin is taken up by the jitter caused by the power supply noise due to the limited AIB routing space. We conducted a comprehensive analysis of signal integrity and power integrity. Based on our findings, we formulated the following integrated recommendations: 1. Minimize crosstalk in package and silicon routing to enhance signal integrity. 2. Mitigate power delivery noise to ensure stable power integrity. 3. Address Power Supply Induced Jitter (PSIJ) by considering architectural changes to reduce its impact.

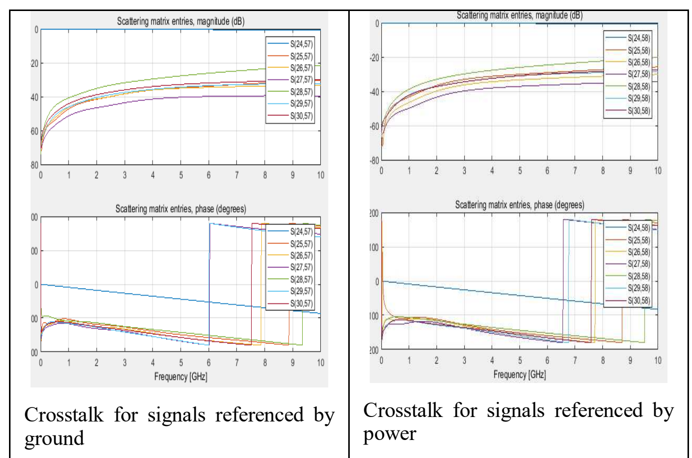
This paper primarily discusses package optimization with a focus on minimizing crosstalk and power supply noise for AIB-O and proposes architecture recommendations to mitigate PSIJ.

II. Signal Integrity Design Optimization

A. DOE for package design

Interconnect behaviors were captured by DOE, to figure out the sensitivity of parameters. For channel loss, crosstalk is one of the main factors impacting the eye diagram. Crosstalk could be caused by vertical vias and horizontal routing, hence we need to identify the bottleneck, and to optimize the bump map or even propose package layer count change while considering cost impact.

Channel crosstalk is examined for different situations. In Fig. 1, crosstalk is compared for cases of reference by ground and power rails. This study is used to design shielding by power or ground routings. In Fig. 2, eye diagrams are shown for different data bits. We figured out the worst signaling bit, and to improve the signal integrity on those worse lines. In Fig. 3, common eye diagrams are shown to identify the cases, when one channel and both channels are simulated. The results showed the impact of crosstalk among channels.



Crosstalk for signals referenced by ground

Crosstalk for signals referenced by power

Fig. 1 Comparison of crosstalk when referenced by gorund or power

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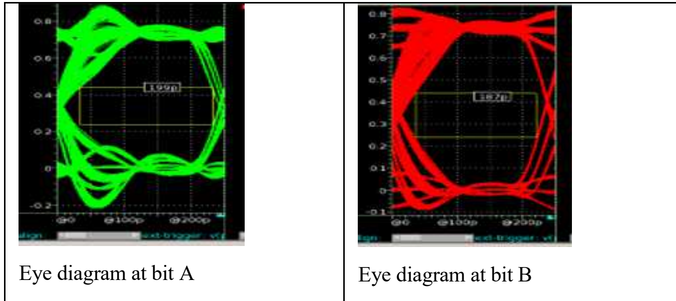
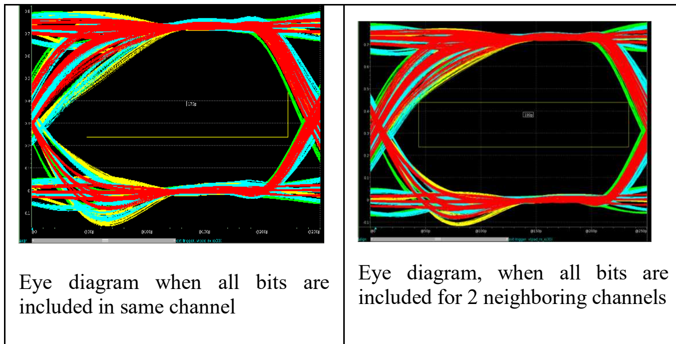
B. *Bump map to minimize the crosstalk*

After the sensitivity is examined, we optimized the package routing to reduce the crosstalk. Change of bump map minimized the crosstalk, and to balance the crosstalk at vertical and horizontal routing. To reduce simulation time, and have good accuracy, 3-D modeling was conducted at one channel. Finally, 2 channels are simulated to check the impact of crosstalk from neighboring channels (as shown in Fig. 3).



Eye diagram at bit A | Eye diagram at bit B

Fig. 2 Eye diagram for different bits



Eye diagram when all bits are included in same channel | Eye diagram, when all bits are included for 2 neighboring channels

Fig. 3 Eye diagram when one channel and two neighboring channels are simulated.

III. Power Delivery Network Design and Optimization

Power delivery network (PDN) consists of PCB, package and silicon power/ground routing and associated capacitance (PCB/package capacitors and device parasitic capacitance). The PDN delivers power to the transistors and regulates power supply noise generated due to transistor switching activities. The PDN design decisions can impact the AIB system performance from power sharing scheme, power delivery and power integrity perspectives.

A. *Power Sharing Scheme Considerations*

Power supply connection scheme determines how the supplies for different IPs and subsystems are connected at the silicon, package and board level. Power scheme optimization helps simplify system PDN design, minimize decoupling challenges, and ensures optimized system performance. AIB interface consists of 4 IP blocks including analog IO drivers, PHY, bit streamer and spreader. The nominal voltage of all IPs blocks is 0.8V. These IPs can be simply combined into a single power supply rail, which greatly simplifies the PDN routing. However, other considerations need to be factored in when we determine the AIB-O interface power sharing scheme:

The need to raise voltage to improve the yield: The transceiver tile has single speed bin. This has impact on yield as the slow process parts cannot be used as they do not meet AIB interface performance requirement. There is need to raise the voltage of AIB interface power supply to improve the yield. But raising voltage increases the power consumption. Increasing power supply voltage from 0.8V to 0.85V causes more than 10% power increase, which is not desired.

The need to reduce power supply induced jitter: Isolation helps reduce the power supply noise and the power supply induced jitter (PSIJ). This is important as the AIB-O interface has higher channel induced jitter comparing to regular AIB interface due to crosstalk increase.

Fig. 4 illustrates the recommended power scheme for the AIB-O interface. The clock path and circuitry that is critical for the performance are separated from AIB-O related circuit on die and at package level under an individual power rail VCC_CLK. This provides flexibility for adjusting the power supply voltage as needed and minimize resulting power increase. The isolation also helps eliminate the coupled noise from switching AIB IO drivers and digital circuitry. The analog IO drivers, the streamer and adapter are powered by the same VCCH_AIB power supply at the package level. Power sharing reduces the package and PCB routing complexity. The package power routing for analog IO driver and digital IPs is combined below the package core layer to reduce the high frequency noise coupling. The VCC_CLK can be combined or separated with VCCH_AIB at board level depending on the nominal voltage required. The detailed simulation data is shown in the following sector.

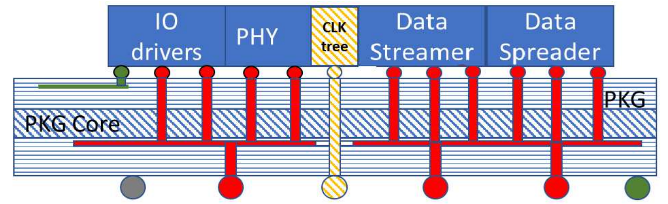


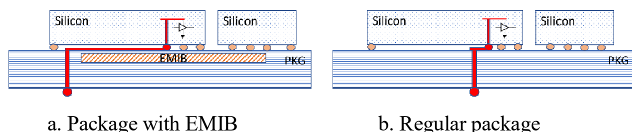
Fig. 4 Power sharing scheme of AIB-O interface

B. *Power Delivery Considerations*

Power delivery design ensures the voltage at the transistor level meets the minimum required voltage for the performance at the reasonable worst case (RWC) power consumption condition.

The power delivery (PD) for AIB-O interface is less challenge than that for regular AIB interface. Signal routing occupies the major portion of the silicon routing area in the IP and package routing is needed to assist the PD. The regular AIB uses EMIB bridge for inter die signal connections and the EMIB bridge blocks the vertical routing through it. The power can only be brought in via limited horizontal routing from EMIB bridge edge, which adds additional IR drop. The bridge design and the package surface routing must be carefully planned and optimized for the power delivery (Fig. 5 a). The AIB-O interface does not

use the EMIB bridge. The vertical package power connection can be added where the power C4 bump locates. The package horizontal power routing is less constrained (Fig. 5 b). As the result, the power delivery (PD) of AIB-O is much improved comparing to the AIB interface.



a. Package with EMIB   b. Regular package

Fig. 5 Package power delivery routing

C. Power Integrity Considerations

The worst-case noise is triggered by the silicon mode change from system PDN design perspective. For parallel IO interface, this happens when IOs activities start/stops. The 1st droop can be reduced by minimizing the inductance to the decoupling capacitors and increasing the on-die capacitance. On-package decoupling capacitors (OPDs) are added. The OPDs are closer to the silicon and has smaller inductance comparing to the PCB mount capacitors, which helps lower the 1st droop. We combine multiple IP blocks as described in previous chapter. This increases device capacitance count. We also reviewed the silicon floor plan with IP team and allocated unused die edge area abutting the analog IO driver region for additional on-die decoupling cap and MIM capacitance fill.

The capacitance from additional die edge area doubles the ODC count of the analog IO driver IP, which greatly helps reduce the high frequency noise due to IO switching.

IV. Architecture Recommendation to Reduce PSIJ

Both transmitter and receiver are built up by circuit blocks, which are powered by different power rails. Each block has its routing length and sensitivity to power rail noises. PSIJ is the accumulation of jitter from PD noise spectrum with respect to the circuitry sensitivity and jitter tracking capability. Hence assigning power rails is a critical process which is not only depending on the voltage level, but also the circuitry sensitivity with its capability to track jitter across different noise spectrum. We did thorough analysis to identify the circuitry path that was more sensitive to jitter and re-assignment the power domain accordingly to mitigate the issue, which changes design electric architecture for better performance. This approach provides a more effective way of improving jitter instead of continuing to dampen the PD noise by costly optimizing the PDN with more decoupling capacitors either at die, package, or board level.

In Fig 6, PD noises were simulated with PDN across different power rails and corresponding current profiles. These noise profiles were added as input to our internal tool which were developed to run the PSIJ analysis [1][2][3]. Delay of each circuitry blocks were simulated and extracted from the transistor model simulation. The jitter sensitivity of each block to the PD noise were then calculated for the PSIJ analysis. These inputs were used to capture the total system jitter which consists of both the transmitter and receivers.

With this in-depth analysis, optimal power supply assignment was recommended to minimize the PSIJ, which also ease the PDN design with lower cost approach.

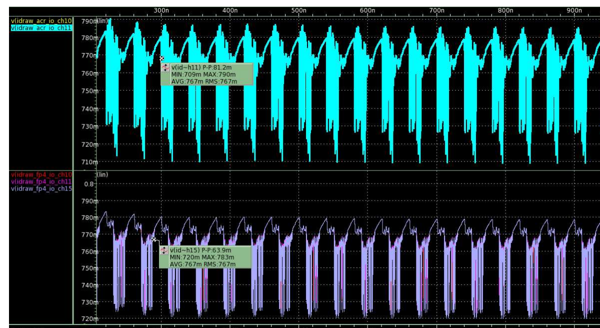


Fig. 6 PD noises across different power rails

V. Conclusion

In this paper, we demonstrated SI, PI, and system level analysis to optimize channel crosstalk through improved bump map and routing techniques. Additionally, we devised a power delivery network to effectively mitigate the PD noises. We proposed an enhanced architecture to reduce PSIJ. As a result, we have successfully achieved high-speed performance for the AIB-O interface.

The learnings from AIB-O performance enhancement include: 1. The routing density is very high for this interface, so the bump map and signal/power/ground routings need to be carefully taken care of to minimize the overall crosstalk. 2. Separation of clock power rail is critical to minimize the PSIJ, though we must compromise the routing complexity. 3. Simulation accuracy needs to be ensured for cost-performance trade-off, when the margin is small.

Acknowledgment

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