Broadband RF Interconnects in a Multi-Layer Advanced Packaging with a Si Interposer

Sofia Mvokany[#1], Jack Molles[#2], Zoya Popović[#3]
[#]Microwave Research Lab, University of Colorado Boulder, USA
{[1]Sofia.Mvokany, [2]Jack.Molles, [3]Zoya.Popovic}@colorado.edu

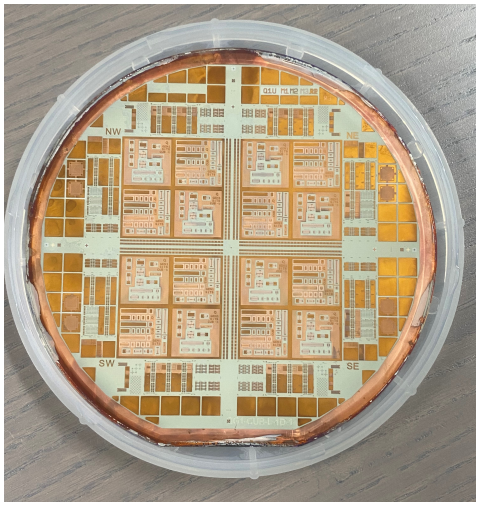
***Abstract*— This paper presents results obtained for multiple types of interconnects using a packaging technique for heterogeneous high-frequency (dc – 50 GHz) integration. The process has three organic dielectric layers laminated on each side of a central silicon interposer. The process allows for metalization of each dielectric layer, leading to 6 possible metal layers. A through-silicon coaxial via (TSV) using all available metal layers is designed. A back-to-back 50-Ω interconnect using two TSVs is measured and shows a return loss higher than 10 dB from dc to 50 GHz with an estimated insertion loss of 1 dB per TSV at 50 GHz. Measured results are compared to previously tested interconnect structures between different transmission lines in the same process.**

***Keywords*— multi-layer, advanced packaging, interconnects, silicon interposer, Through-silicon-Via (TSV)**

I. Introduction

In this work, an experimental process intended for heterogeneous integration of microwave circuits, is used for the design of various interconnects. Heterogeneous integration allows the combining of different chip and passive technologies, chosen for best performance, to be packaged in a single unit. For example, silicon chips can be used for mixed signal and digital functions, and implemented in the same process with GaAs or InP circuits for good noise performance at microwave frequencies, and GaN integrated circuits for high power handling capabilities [1]. Additionally, integration using both sides of a wafer can be achieved through the use of larger vias extending through the wafer core or interposer made from glass [2], silicon [3] or redistribution layers [4]. These "through-interposer-vias" allow for low-loss and broadband signal paths between both sides of a two-sided packaging process, resulting in a compact multichip package.

This work presents a through-silicon-via (TSV) designed using the packaging process developed by Qorvo and Applied Materials which consists of 3 resin-filled organic dielectric layers laminated on both sides of a 100-μm thick rigid high-resistivity not doped silicon interposer, allowing 6 potential metal layers on top of the dielectric layers. A photograph of a 10-cm (4-inch) wafer with numerous test structures is shown in Fig. 1a. An annotated cross-section of the wafer in Fig. 1b shows the 6 low-permittivity dielectric layers with the silicon core, the 6 metal layers and various metalized vias between layers. The simulated and measured results for a TSV utilizing 6 metal layers are presented here. Simulations are performed with the Ansys HFSS 3D full-wave electromagnetic solver, and the



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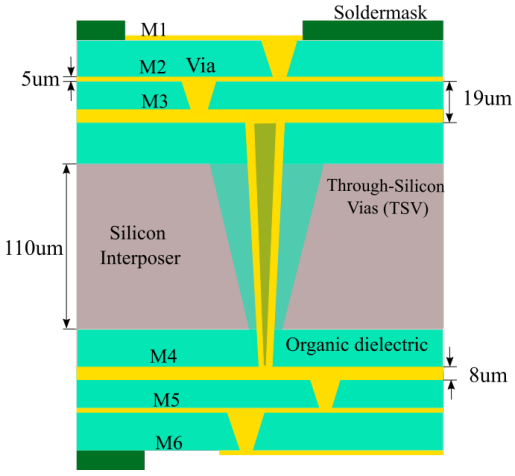

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Fig. 1. (a) Photograph of a 10-cm (4-inch) wafer with 6 organic dielectric layers on a Si interposer. (b) Sketch of the cross-section of the wafer, showing dielectric and metal layers of the stack-up and metalized vias between all layers. Approximate dimensions are given in μm. The thicknesses of layers M1, M2, M5 and M6 are the same, as well as those of M3 and M4.

fabricated designs are measured using an Agilent 38364C PNA with ACP-50-A-GSG-150 FormFactor probes and a Summit 9000 probe station. The calibration is performed using a Cascade Microtech 101-190 C Alumina Impedance Standard Substrate, placing the measurement reference plane at the probe tips. This method is standardised throughout all simulations and measurements presented in this work.

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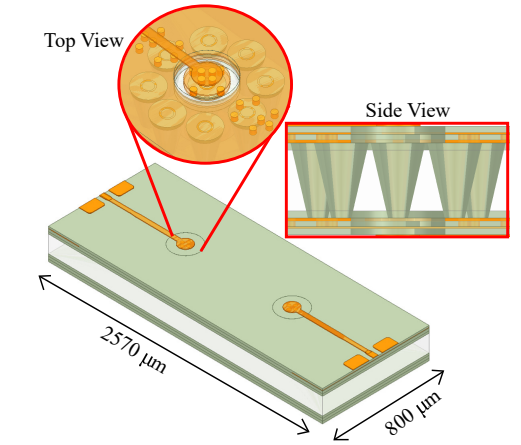
Additionally, the measured results of two previously tested 3-metal-layer interconnect structures in the same process are compared with the TSV measured results and previously published TSVs.

II. Through-Silicon Via Interconnect

The through-silicon coaxial via presented here connects the bottom layer of the wafer to the top through a central silicon interposer. Fig. 2a shows a top, side and 3-D view of the test structure with dimensions of 2570 μm by 800 μm. The coaxial interconnect consists of a central TSV surrounded by 8 vias within the silicon, as highlighted by the top and side views in Fig.2a. The microstrip signal line starts on metal M1, on top of the wafer, with a ground plane on metal layer M2. Metal layers M3 and M2 are connected by solid copper vias. A dielectric-filled hole is opened through metal layers M2 and M3, and an array of copper vias establishes the transition between layers M1 and M3. The TSV starts on the M3 layer, and connects to M4 through the Si interposer.



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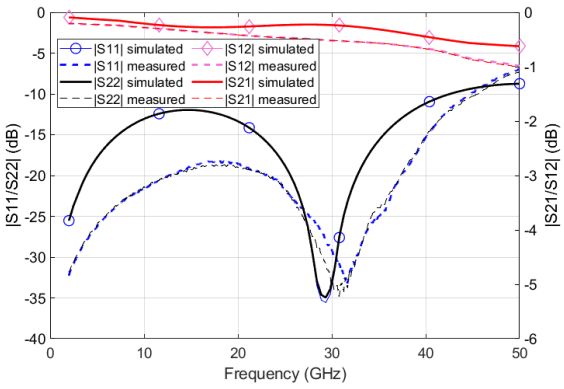

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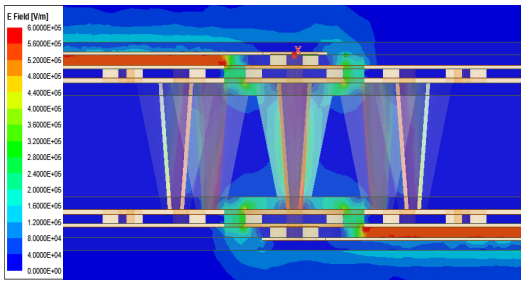
Fig. 2. (a) Three-dimensional view of through-silicon-via (TSV) interconnect with transitions from M1-M2 microstrip, through the silicon interposer to the M6-M5 microstrip. (b) Simulation and measurement results from 2 to 50 GHz for TSV structure deembedded to a single transition.

The TSV is designed to be a 50 Ω coaxial transition between the microstrip lines on M1 and M6 with ground layers on M2 and M5, respectively. It consists of a dielectric core, surrounded by a 5–7 μm thick copper conical conductor tapering from 65 μm to 30 μm in diameter. The conductor is surrounded by an organic dielectric outer layer through the silicon. Its overall diameter tapers from 160 μm to 100 μm when connecting M3 to M4. The measured back-to-back test structure consists of two TSVs. Referring to Fig. 2a, the signal travels from the input ground-signal-ground (GSG) pads on M1 to M6, through the TSV, and back to M1 along an identical path to the output GSG pads.

Fig. 2b shows the reflection and transmission coefficients of a single TSV transition deembedded from measured data from the back-to-back test structure. The match is below 10 dB to 45 GHz, while the insertion loss remains below 1 dB to 50 GHz. Simulations are performed using electrical properties provided by the manufacturer at 20 GHz and 40 GHz. This data given at two points within the band of interest is linearly extrapolated across the dc to 50 GHz frequency range. Increased loss is observed in measurements compared to simulations, due to the early stage of this experimental process and a lack of loss tangent and permittivity data for the organic dielectric at microwave and millimeter-wave frequencies.



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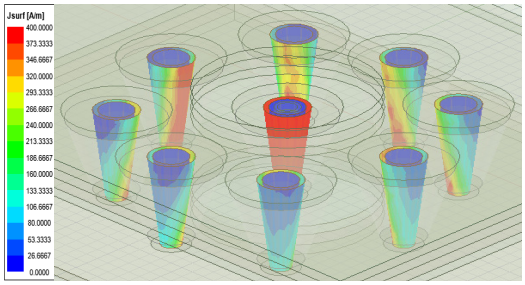

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Fig. 3. (a) Side view of simulated electric field magnitude distribution at 26 GHz through the TSV structure. (b) Simulated surface current magnitude distribution at 26 GHz through the TSV and surrounding "coaxial shield". The simulations are normalized to 1 W input power.

Additionally, the magnitude of the complex electric field is simulated, overlayed on a side view of the structure and shown in Fig. 3a as a visual representation of the signal path. The electric field along the TSV is concentrated within the organic dielectric cladding and has a comparatively low magnitude within the surrounding silicon interposer. The magnitude of the surface current density along the TSV and surrounding coaxial-shield-vias is also simulated and shown in Fig. 3b. As suggested by the electric field distribution, the bulk of the current is concentrated along the TSV and the interior faces of

the shield vias. The simulation results are obtained using wave ports in HFSS, and are normalized to 1 W of input power.

III. Discussion and Conclusions

On the same wafer, various interconnects are designed and measured using metal layers M1, M2, and M3. This includes microstrip-to-microstrip and grounded co-planar waveguide (GCPW)-to-microstrip interconnects described in more detail in [5]. Both structures, 1650 μm by 800 μm in dimensions, transition from a signal line on M1 to a signal line on M2 with the ground layer on M3. Fig. 4 shows the measured S-parameters compared with those of the TSV. For all three interconnects, the measured data is de-embedded to show results for a single transition. It is important to note that the TSV has increased loss because it transitions between six dielectric layers in addition to the silicon core, in contrast to the single dielectric layer transitions. Table 1 gives a comparison of the three interconnects with other TSVs found in the literature. Here the return loss is RL= $-20\log|s_{11}|$, and the insertion loss IL= $-20\log|s_{21}|$. The IL is given in dB/mm because it takes into account the length of the interconnecting lines, which differ for all cases. The microstrip line for the first interconnect is 1.65 mm long, the GCPW line is 1.65 mm long, while the lines of the three TSVs in the table are 2.57, 3.15 and 1 mm long, respectively.

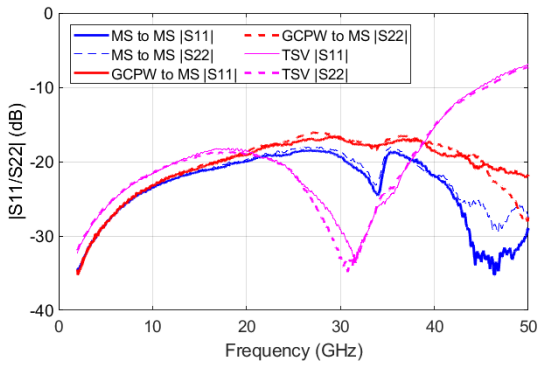
Table 1. Measured return loss (RL) and insertion loss (IL) comparison for three interconnect types at 10 and 40 GHz.

Interconnect	**RL(dB) 10 GHz**	**IL(dB/mm) 10 GHz**	**RL(dB) 40 GHz**	**IL(dB/mm) 40 GHz**
MS – MS	24	0.06	22	0.12
GCPW – MS	24	0.06	18	0.18
TSV	22	0.11	15	0.27
TSV in [6]	10	0.16	10	0.29
TSV in [7]	27	0.11	15	0.22

In summary, this paper presents a through-silicon-via (TSV) interconnect designed in a multi-layer resin-filled organic dielectric-on-silicon interposer process developed by Qorvo and Applied Materials. The TSV transition highlighted in this paper provides low loss through the silicon interposer core and utilizes all six metallic layers of the process. It is simulated and measured from 2 to 50 GHz, but also operates down to dc and simulations show that insertion loss increases to 1.01 and 1.62 dB at 75 and 100 GHz, respectively. It is expected these values will be higher in measurements.

IV. Acknowledgment

This work is funded by Qorvo, award AWD-21-03-0167, on the United States Navy SHIP program, in partnership with Applied Materials.



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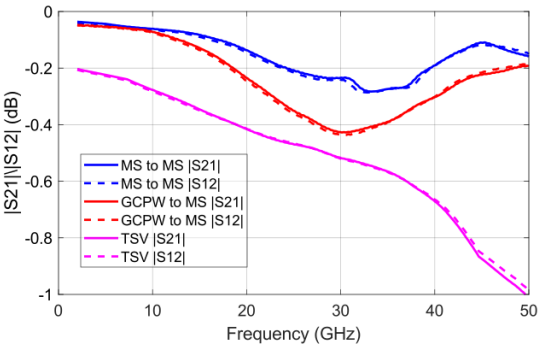

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Fig. 4. (a) Measured reflection coefficient of microstrip-to-microstrip interconnect, GCPW-to-microstrip interconnect and TSV, all fabricated on the same wafer. (b) Measured deembeded transmission coefficient of the three single transitions.

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