Method of Exploring HVM Process Corner Cases for Loss and Impedance in High Speed Designs

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***Abstract*— High-speed signals are becoming more sensitive to impedance and loss variations. In this paper, we show that the correlation between factors that impact loss and impedance is weak. A methodology is proposed to find corner case loss and impedance models for a given stack-up using an inverse stack-up optimization problem (ISOP) [1]. By using this proposed approach, corner case loss and impedance models can be derived in seconds. The proposed approach results outperform the worst-case Monte Carlo analysis with uniform distribution in all the experiments in terms of accuracy and speed-up.**

***Keywords*— ISOP, Surrogate models, Harmonica**

I. Introduction

With the doubling of high-speed serial link signal speeds every generation, there is an increased sensitivity to loss and impedance variations. Fig. 1 shows a cross-sectional analysis of a stripline differential trace. It is seen that there are around 15 variables that impact loss, impedance, and crosstalk. When designing a high-speed system, electrical design engineers optimize these variables to come up with a stack-up that achieves the target impedance with low loss and crosstalk. Converging at the optimal choice of variables often requires a lot of iterations and engineering judgment. In the past, the inverse stack-up optimization framework (ISOP) [1] was proposed to perform the stack-up optimization efficiently. The challenge this paper discusses stems after the optimal cross-section is determined.

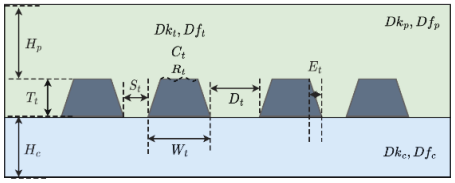

Fig. 1. Structure of a Differential Stripline Layer [1].

Even after optimizing the stack-up variables, a lot of these variables still exhibit small variations due to process and manufacturing tolerances [2]. This is the same reason why the target impedance of a high-speed signal is never a fixed number like 85 ohms or 100 ohms but usually 85 ohms ±10% or 100 ohms ±15% tolerance. PCB manufacturing vendors cannot control these variables, and these variables usually exhibit around 10-15% variation, which in turn impact signal loss and impedance. High-speed design engineers should consider these impedance and loss corner cases due to process and manufacturing variations to ensure their designs survive high-volume manufacturing (HVM).

This paper is arranged as follows: Section II describes ISOP at a high-level, and Section III discusses the proposed approach to determine the worst-case impedance and loss corner cases. Section IV shows the results of a few experimental test cases. The results compare the speed-up and accuracy of the proposed approach against the worst case of uniformly distributed Monte Carlo analysis. Section V concludes the paper.

II. Inverse Stack-up Optimization Problem (ISOP)

The inverse stack-up optimization enables fast and efficient automation of stack-up design. In a conventional setting, stack-up optimization is done iteratively using time-consuming simulations. This process sometimes relies on a designer's heuristics and intuition, which does not guarantee an optimal solution.

To overcome these challenges, a systematic approach to inverse stack-up design by formulating the problem as a hyper-parameter optimization (HPO) [3] process is adopted [1], [4]. The inverse stack-up optimization task with HPO efficiently explores the design space (S) to find a set of parameters ($\mathbf{x}$) that best optimizes the performance figure-of-merit (f^{FoM}) and meet the performance constraints (f^{C}). This task can be formulated as shown in Eq. (1).

$$\mathbf{x}^* = \underset{\mathbf{x}}{\operatorname{argmin}}\, f^{FoM}(\mathbf{x}) \quad (1)$$
$$\text{subject to} \quad x_i \in S_i \text{ for } i = 1, \dots, d$$
$$f_j^C(x) \le 0 \text{ for } j = 1, \dots, k.$$

where d is the number of design parameters and k is the number of constraints.

ISOP [1] addresses the inverse stack-up optimization problem by leveraging Harmonica [5], a discrete domain HPO technique with a spectral approach. Fig. 2 shows the overall flow of ISOP. ISOP consists of two stages: early search space exploration and candidate roll-out.

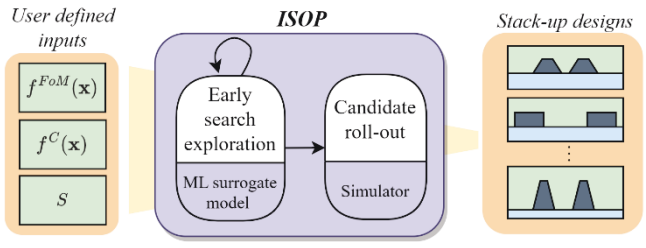

Fig. 2. ISOP Flow [1].

During the first stage, the design space is efficiently narrowed down by identifying the set of design parameters that significantly optimizes the specified optimization objectives. This process is achieved by utilizing a machine learning (ML) surrogate model based on a multi-layer perceptron (MLP) structure. This allows fast evaluation of our optimization objectives. The second stage finalizes that

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design solution within the reduced design space by evaluating different candidates using precise simulation results. In this paper, a different use case for ISOP that incorporates HVM variation to study corner case models is investigated.

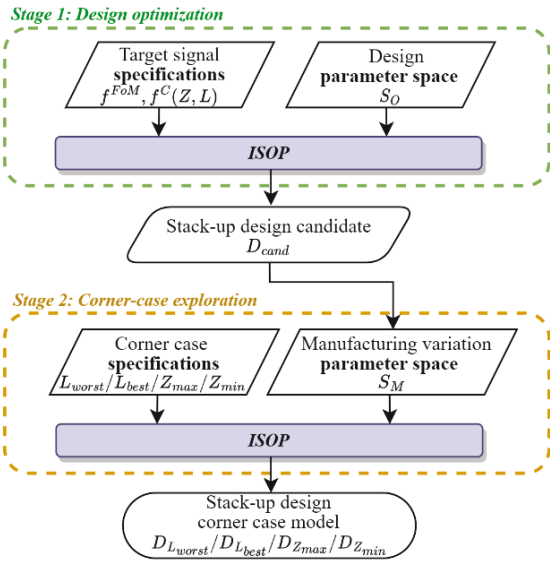

Fig. 3. Proposed approach for capturing HVM corner cases.

III. Proposed Methodology

We can effectively identify corner case models that consider manufacturing and process variations by adapting the ISOP framework. ISOP has two inputs, target signal specification, such as characteristic impedance (Z) and insertion loss (L), and the design parameter space (S_o) that constrains the optimization space. By utilizing and modifying these two inputs, we can customize ISOP to our particular application of identifying corner case models.

Fig. 3 illustrates the overall flow of the proposed corner case modeling process. In Stage 1, we perform design optimization to generate the initial stack-up design candidate (D_{cand}). While D_{cand} is optimized for optimal performance, constructing a stack-up with this design candidate will not capture the worst-case signal behavior resulting from variation in HVM. Table I illustrates these variations for each of the stack-up design parameters. All parameters are approximated to have Gaussian distributions with their sigma (standard deviation) values. The distribution types (like Uniform or Gaussian) and sigma values for each design parameter are programmable. To account for the uncertainty caused by various parameters and to predict the worst-case scenario, the Stage 2 for corner-case exploration is proposed.

Stage 2 takes corner case specifications (L_{best}, L_{worst}, Z_{max} or Z_{min}) and manufacturing variation parameter ranges (R_M) as inputs. Table II shows a detailed description of the corner case specifications. L_{best}, L_{worst}, Z_{max} and Z_{min} define the optimization objectives. For example, the optimization objective for L_{best} and L_{worst} is to find the best and worst loss model within an acceptable impedance range of Z±10%. Z_{max} and Z_{min} find the model that has Z+10% and $Z-10\%$, respectively. The second input R_M is determined by computing the sigma values using D_{cand} and the data from Table I. The bounds of each parameter are set at five sigma points. Similar to S_O from Stage 1, $S_M$confines the optimization design space.

The final output from corner-case exploration stage are the design parameters for corner case, $D_{L_{best}}$, $D_{L_{worst}}$, $D_{Z_{max}}$, or $D_{Z_{min}}$. Utilizing these corner case models generated by the proposed process, we can anticipate potential worst-case scenarios. This allows us to take preemptive measures, such as adjusting the D_{cand} or implementing other relevant actions to mitigate any adverse effects.

TABLE I. Manufacturing Variation In PCB Stack-up

	Sigma Equation		Sigma Equation
W	$0.02 \cdot W$	E	0.04
S	$0.02 \cdot S$	Dk	$0.01 \cdot Dk$
H	$0.03 \cdot H$	Df	$0.03 \cdot Df$
T	$0.03 \cdot T$	C	400000
D	$0.1 \cdot \min(H_C, H_P)$	R	0.04

TABLE II. Coner Case Task Specifications

Case	Task Description
L_{best}	Minimize $\|L\|$, while $0.9 \cdot Z_{tar} \le Z \le 1.1 \cdot Z_{tar}$
L_{worst}	Maximize $\|L\|$, while $0.9 \cdot Z_{tar} \le Z \le 1.1 \cdot Z_{tar}$
Z_{max}	Minimize $\|Z - 1.1 \cdot Z_{tar}\|$
Z_{min}	Minimize $\|Z - 0.9 \cdot Z_{tar}\|$

IV. Results

In this section, the experimental result for our proposed methodology and present design solution examples is presented.

A. Design solution example

Two experiments are designed for two different task settings, E1 for when $Z_{tar} = 85\Omega$ and E2 for when $Z_{tar} = 90\Omega$. The first ISOP design optimization stage finds a set of design parameters D_{cand} that minimizes L within the Z of Z_{tar}±1%. Then, we compute S_M with respect to D_{cand} by finding 5 sigma points using the manufacturing variation data from Table I. With this information, we find the corner case models $D_{L_{best}}$, $D_{L_{worst}}$, $D_{Z_{max}}$, and $D_{Z_{min}}$ for each experiment.

Table III describes the experiment results and following corner cases. Columns 2-16 display individual design parameters, and columns 17-18 present the predicted Z and L value from the ML surrogate model. The last two columns present the actual simulation result on the final corner case design parameters. Results for E1 demonstrates that the proposed method successfully identified all corner case model for loss and impedance. Also, it is interesting to note that the corner case Z model does not correlate with L model, and vice versa. The corner case Z model had L similar to D_{cand}'s L, whereas the corner case L model had Z similar to D_{cand} 's Z. This result emphasizes the importance of examining the Z and L corner case models separately. The result for E2 exhibits the same trend as E1.

TABLE III. D_{Cand}, R_M AND CORNER CASE MODELS FOR EACH EXPERIMENT E1 AND E2

E1		W_t	S_t	D_t	H_C	Dk_t	Df_t	H_t	Dk_c	Df_c	E_t	R_t	C_t	H_P	Dk_P	Df_P	Pred Z	Pred L	Z	L
D_{Cand}		5	4.5	40	5	3.6	0.01	1.2	3.6	0.01	0.25	-10	5.6e+7	7	3.6	0.01	85.91	-1.239	85.84	-1.245
S_M	Min	4.5	4.05	37.5	4.25	3.42	0.0085	1.02	3.42	0.0085	0.05	-12	5.4e+7	5.95	3.42	0.0085	N/A	N/A	N/A	N/A
	Max	5.5	4.95	42.5	5.75	3.78	0.0115	1.38	3.78	0.0115	0.45	-8	5.8e+7	8.05	3.78	0.0115	N/A	N/A	N/A	N/A
Corner Case Models	$D_{L_{best}}$	5.5	4.95	42.5	5.75	3.42	0.0085	1.38	3.42	0.0085	0.05	-12	5.8e+7	7.44	3.42	0.0085	85.88	-0.976	85.6	-1.004
	$D_{L_{worst}}$	4.5	4.05	39	4.25	3.78	0.0115	1.02	3.78	0.0115	0.45	-8	5.4e+7	5.95	3.78	0.0115	85.59	-1.547	85.3	-1.552
	$D_{Z_{max}}$	4.6	4.575	38.75	5.52	3.55	0.0115	1.055	3.77	0.0085	0.42	-9.35	5.77e+7	6.21	3.4325	0.0085	93.50	-1.257	93.42	-1.252
	$D_{Z_{min}}$	5.34	4.2	42.25	4.25	3.6775	0.0085	1.335	3.7625	0.0115	0.07	-10.5	5.74e+7	6.61	3.495	0.0115	76.50	-1.233	76	-1.258
E2		W_t	S_t	D_t	H_C	Dk_t	Df_t	H_t	Dk_c	Df_c	E_t	R_t	C_t	H_P	Dk_P	Df_P	Pred Z	Pred L	Z	L
D_{Cand}		5	4	40	3	2.8	0.002	0.6	2.8	0.002	0.25	-10	5.6e+7	6	2.8	0.002	90.57	-0.774	89.94	-0.786
S_M	Min	4.5	3.6	38.5	2.55	2.66	0.0017	0.51	2.66	0.0017	0.05	-12	5.4e+7	5.1	2.66	0.0017	N/A	N/A	N/A	N/A
	Max	5.5	4.4	41.5	3.45	2.94	0.0023	0.69	2.94	0.0023	0.45	-8	5.8e+7	6.9	2.94	0.0023	N/A	N/A	N/A	N/A
Corner Case Models	$D_{L_{best}}$	5.5	4.4	41.5	3.45	2.66	0.0017	0.69	2.66	0.0017	0.05	-12	5.8e+7	6.73	2.66	0.0017	91.66	-0.596	91.02	-0.604
	$D_{L_{worst}}$	4.5	3.6	40.25	2.55	2.94	0.0023	0.51	2.94	0.0023	0.45	-8	5.4e+7	5.1	2.94	0.0023	89.52	-1.009	88.04	-1.069
	$D_{Z_{max}}$	4.57	4.4	40.75	3.18	2.765	0.0017	0.61	2.89	0.0017	0.42	-8.425	5.72e+7	6.09	2.87	0.0017	99.00	-0.796	98.2	-0.814
	$D_{Z_{min}}$	5.37	3.6	41.5	2.73	2.85	0.0023	0.54	2.795	0.0023	0.05	-10.775	5.65e+7	5.27	2.83	0.0023	81.00	-0.803	80.1	-0.823

TABLE IV. EXPERIMENT RESULT COMPARISON WITH BASELINE METHODS

E1		**Pred *Z***	**Pred *L***	***Z***	***L***	**Run time (s)**
$D_{L_{best}}$	3M GMC	86.49	-1.144	86.38	-1.155	109.83
	3M UMC	88.04	-1.021	87.84	-1.472	95.95
	Proposed	**85.88**	**-0.976**	**85.6**	**-1.004**	**12.31**
$D_{L_{worst}}$	3M GMC	86.20	-1.331	86.16	-1.333	109.83
	3M UMC	84.49	-1.470	84.23	-1.042	95.95
	Proposed	**85.59**	**-1.547**	**85.3**	**-1.552**	**18.53**
$D_{Z_{max}}$	3M GMC	91.95	-1.262	91.91	-1.253	109.83
	3M UMC	93.50	-1.279	93.51	-1.264	95.95
	Proposed	**93.50**	**-1.257**	**93.42**	**-1.252**	**12.33**
$D_{Z_{min}}$	3M GMC	79.91	-1.265	79.68	-1.280	109.83
	3M UMC	76.50	-1.201	76.09	-1.230	95.95
	Proposed	**76.50**	**-1.233**	**76**	**-1.258**	**10.17**
E2		**Pred *Z***	**Pred *L***	***Z***	***L***	**Run time (s)**
$D_{L_{best}}$	3M GMC	91.96	-0.696	91.5	-0.699	151.45
	3M UMC	92.24	-0.627	91.75	-0.631	80.93
	Proposed	**91.66**	**-0.596**	**91.02**	**-0.604**	**9.44**
$D_{L_{worst}}$	3M GMC	88.14	-0.857	87.04	-0.886	151.45
	3M UMC	90.46	-0.956	89.09	-0.992	80.93
	Proposed	**89.52**	**-1.009**	**88.04**	**-1.069**	**11.21**
$D_{Z_{max}}$	3M GMC	97.57	-0.737	97.15	-0.739	151.45
	3M UMC	99.00	-0.805	98.67	-0.818	80.93
	Proposed	**99.00**	**-0.796**	**98.2**	**-0.814**	**17.77**
$D_{Z_{min}}$	3M GMC	83.54	-0.801	82.66	-0.817	151.45
	3M UMC	81.00	-0.714	79.93	-0.726	80.93
	Proposed	**81.00**	**-0.803**	**80.1**	**-0.823**	**12.52**

B. Evaluation of Corner Case Exploration

This section describes the results for the proposed method and compares it with the baseline methods. Two different brute force Monte Carlo (MC) [6] sampling approaches are used, Gaussian-distributed MC (GMC) and uniformly distributed MC (UMC), of three million samples each. The solutions are evaluated using the same ML surrogate model as the proposed method.

Table IV shows the result for comparison with the baseline methods. Our proposed method is able to achieve more extreme corner case designs with significantly shorter time (~16x) compared to UMC for all cases. Due to the normal distribution nature of GMC, it is expected that GMC would not be able to provide the worst case unless the sample size increases by an order of magnitude or more.

V. CONCLUSIONS

The correlation between the factors impacting loss and impedance is weak. It is found that the worst/best-case loss happens around nominal impedance and vice-versa. The paper presents a methodology for analyzing worst-case impedance and loss models due to HVM and process variations for high-speed designs. The fast and efficient procedure is achieved by adapting the ISOP framework, which utilizes the HPO search algorithm and the ML surrogate model. Experimental results demonstrate that the method can produce corner case design solutions within a few seconds and is significantly efficient compared to brute force uniform distribution Monte Carlo sampling. By employing the proposed approach, we efficiently generate the corner case impedance and loss models. This enable designers to proactively plan for potential worst-case scenarios and take appropriate measures to mitigate the negative effects.

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