A Flexible Neural Network-Based Tool for Package Second Level Interconnect Modeling

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***Abstract*—This paper introduces a neural network (NN)-based practical design tool for quick assessment of package second level interconnects (SLIs) at the earlier design stages. The study addresses the well-known computational cost problem of data generation and training processes of NN implementation by proposing a flexible model approach, where the SLI geometry is divided into several building blocks, for which a separate NN model was trained. The NNs take geometrical parameters as inputs and return the complex S-parameter matrices as outputs. The electrical performance of the entire SLI geometry is obtained by cascading the S-paramaters of the building blocks.**

***Index Terms*—Neural network, high-speed I/O, S-parameters, packaging, second level interconnect**

I. Introduction

Package second level interconnect (SLI) is a limiting factor in the electrical performance of microelectronic packages because of the reflections caused by impedance discontinuities and crosstalk in the plated through hole (PTH) and ball grid array (BGA) field. This has become extremely critical for state-of-the-art package design, particularly for serial input/output (I/O) interfaces where per lane data rates have started to exceed 100 Gbps per lane [1]. Reflections are typically minimized by removing the metal layers beneath or above PTH, BGA and/or microvia pads, which is referred to as shadow voiding [2]. Although this is an effective way of improving the electrical performance, the task is extremely complicated because of the multi-target optimization process with competing performance goals, such as power rails with low loop inductances, and manufacturing constraints, such as maximum void area. Therefore, the optimization of the SLI electrical performance requires multiple iterations, involving different aspects of package design, and requiring significant computational resources because of rigorous full wave analysis. Hence, a fast and accurate surrogate model (SM) to predict SLI electrical performance, especially at the earlier stages of the design cycle, would be extremely useful for rapid prototyping and short time to market.

Neural network (NN)-based SMs have been extensively used in the analysis of electrical components for fast and accurate performance assessment. Several publications in the literature reported successful modeling applications of passive microwave components [3]–[5], high-speed channels [6], linear and non-linear microwave circuits [7], and causal and passive S-parameter prediction [8]. Furthermore, NNs have also been utilized in several package design applications including voltage regulator optimization and power delivery network modeling [9]. This paper builds on the theory explained in [8] to develop a practical tool for fast and accurate S-parameter prediction of a differential pair on packages with different stack-ups, using an NN-based SM.

II. Modeling Approach

In general, supervised learning-based SMs can provide very accurate predictions of the system of interest in a very short amount of time. However, their extrapolation capabilities are limited. Once the input parameter space is defined and samples are generated, the prediction capability of the model remains within that space. A new input parameter space should be defined and a new data set should be generated even if there is a small change in the system of interest.

A classical approach for SLI modeling and data set preparation is to model the entire stack-up in one piece and collect the data samples via full wave simulations. However, because of the above discussion, even a small change in the SLI geometry requires a completely new data set for accurate predictions. For instance, a new data set and training process are required for every package with different layer count, which is computationally extremely expensive. Therefore, in this study, we adopted a divide and conquer approach, where the SLI is divided into several building blocks, as shown in Fig. 1, such as the feed, build-up, PTH, and BGA blocks. An NN model for each block were trained separately and the predicted S-parameters were cascaded to obtain the S-parameter of the entire SLI. All SLI models include one feed, one PTH, and one BGA block, and packages with different number of layers are obtained by adding build-up blocks as required. This approach introduces a significant flexibility and generalization capability, by enabling analysis of packages with different number of layers using only 4 NN models. Moreover, since the input parameter count and problem geometries of each block is much smaller than the entire SLI, the data generation and training processes are also faster.

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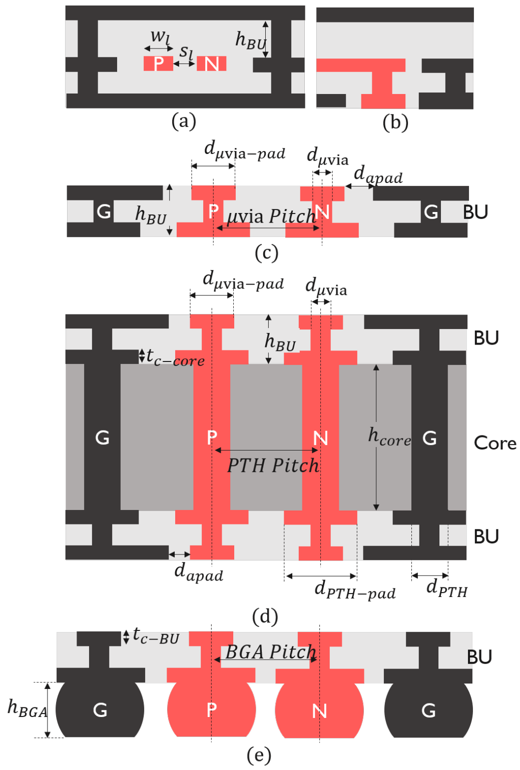

Fig. 1. Building blocks of the SLI geometry. (a) The stripline feed. (b) The stripline feed side view. (c) Build-up layer. (d) PTH. (e) BGA.

Considered interconnect geometry consists of a single differential pair and 8 accompanying ground pins on a rectangular grid. Signal to signal, signal to ground, and ground to ground pitches are assumed to remain constant through the entire stack-up. The feed block consists of 3 metal layers with a stripline feed and microvias whereas, the build-up and BGA blocks include 2 metal layers. The PTH block, however, contains 2 core metal layers in addition to 2 build-up metal layers. Each building block is terminated at the half thickness of the associated metal layer. For a complete list of the input parameters and ranges, the reader is referred to [8].

Port parasitics may have a significant impact on the cascaded S-parameter data and result in erroneous predictions, particularly for high number of layers. Therefore, wave ports were selected for excitation. However, since wave ports support multi mode propagation, as opposed to lumped ports, higher order modes may be excited at the pad/via interfaces, because of the diameter discontinuities. Hence, as illustrated in Fig. 2, the ports were defined on a coaxial cable-like input structure, where the inner and outer conductors have identical diameters to the via pad and antipad. The ports were also defined at a sufficiently long distance to allow effective attenuation of the higher order modes, and then deembedded in accordance with the metal thickness of the model.

III. Neural Network Architecture

The NN architecture used in this study is identical to the one proposed in [8] and is summarized here for completeness.

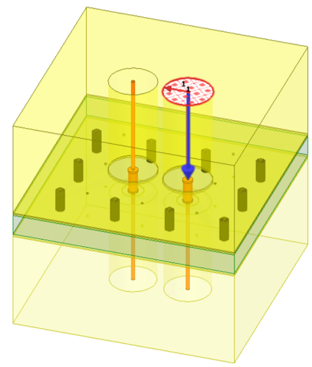

Fig. 2. Coaxial wave port setup for the PTH model.

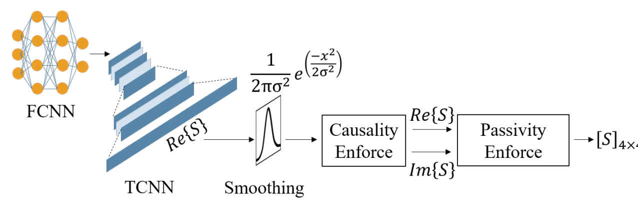

Fig. 3. Neural network architecture.

The NN is composed of fully connected (FCNN), transposed convolutional (TCNN), learnable smoothing, and causality and passivity enforcement layers, as depicted in Fig. 3. The FCNN takes the geometrical parameters as inputs and maps them to a latent space. The TCNN efficiently converts the latent variables to vectors without suffering from scaling issues [9]. This is extremely important when a response over a wide spectrum is predicted. The real part of the S-parameters (TCNN output) is then smoothened via a Gaussian filter, with a learnable standard deviation, and fed into the causality enforcement layer, which computes the imaginary part of the S-parameters using Hilbert transform relations. Finally, the passivity enforcement layer takes the complex S-parameters, computes the upper bounds for the associated eigenvalues, and applies compensation for passivity violations. The output is a 4×4 complex S-parameter matrix for the differential pair.

IV. Numerical Results

The accuracy of the proposed divide and conquer modeling approach was tested using different SLI geometries and comparing them with full wave simulation results. Figs. 4 and 5 compare the single-ended magnitude and phase of the predicted return loss of an SLI of a 5-2-5 package with those of the full wave simulations. In these figures, “Cascade 3D EM” refers to the case where the building blocks were simulated separately and their S-parameters are then cascaded. In contrast, “Full 3D EM” refers to the case where the entire geometry is simulated as a single model from the feed to the BGA. As seen from the figures, even at low magnitude levels, there is a very good agreement between the results, verifying the effectiveness of the NN predictions and the divide and conquer modeling approach.

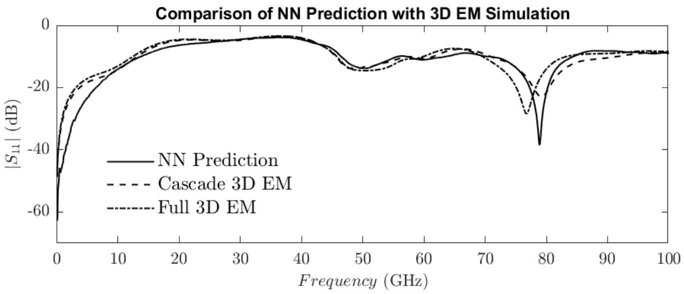

Fig. 4. Return loss magnitude comparison.

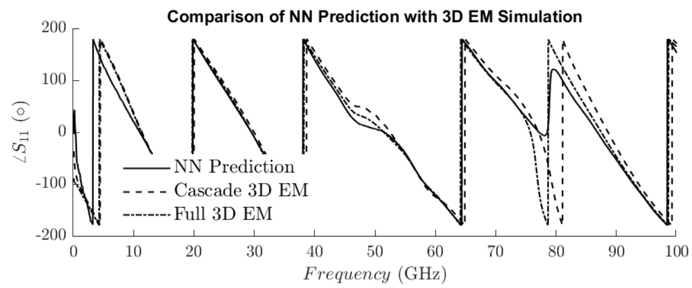

Fig. 5. Return loss phase comparison.

Furthermore, Figs. 6 and 7 show the comparison of the single-ended insertion loss and far end crosstalk, respectively, for two different package stack-ups. The results show that the proposed approach provides sufficiently accurate predictions for packages with different layer counts, by simply changing the number of cascaded build-up layers, with the correct geometry and port settings. Although there are some differences between the NN predictions and simulation results, the accuracy level is acceptable for a quick low-fidelity analysis, which can provide a good initial point for the final optimization.

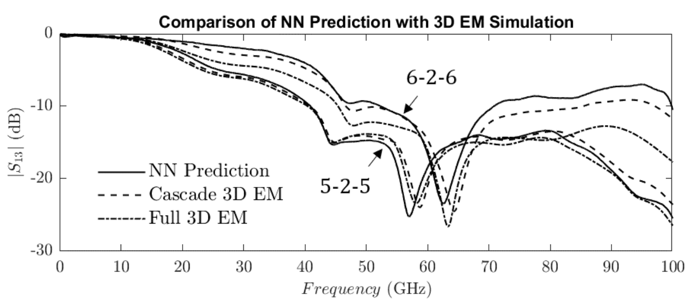

Fig. 6. Insertion loss comparison.

V. Conclusion

This study reports an NN-based modeling tool for the electrical analysis of SLIs and discusses some practical implementation details. To introduce some flexibility, the SLI geometry is divided into 4 building blocks and a separate NN model was trained for each block. The electrical response of the SLI is obtained by cascading the S-parameter matrices of the building blocks. This approach enables modeling of

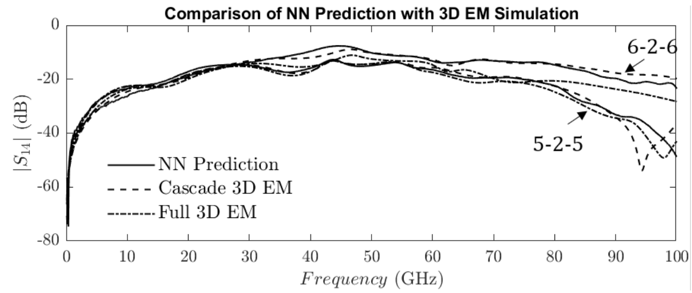

Fig. 7. Far end crosstalk comparison.

packages with different layer counts without generating new data sets and retraining. Special care should be given to excitation to minimize the cumulative impact of port parasitics and higher order mode propagation. When correctly implemented, the proposed model was demonstrated to accurately predict SLI performance over a wide range of frequencies. The results proved that NN-based models combined with flexible modeling approach is an effective tool for fast assessment of SLI geometries, particularly at the early design stages.

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