Thermal Sensitivity of Dielectric Materials in High-Speed Designs

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Abstract—At high-speeds, careful analysis is required at the design stage to ensure robust signal integrity (SI) in high-speed printed circuit boards (PCBs). Signal loss in PCBs is predominantly due to conductor loss, dielectric loss and impedance mismatch.

In this paper, thermal impact on loss and impedance is studied. In that, thermal sensitivity for standard loss, mid-loss, low-loss and ultra-low loss dielectric materials is studied. It is observed that ultra-low loss materials are less sensitive as compared to standard loss materials. Also, thermal impact on impedance and loss in transmission lines, vias and SMT pads is analyzed.

Keywords—Impedance, Thermal sensitivity, PCB

I. INTRODUCTION

Thermal impact on signal integrity (SI) is becoming dominant in high-speed printed circuit boards (PCBs). Heat generated from components can degrade the electrical performance of traces and lead to SI failure [1]. Electrical characteristics of copper traces and dielectric materials vary with temperature, which degrades the performance of signals. In the case of high-speed signals, where the signal-to-noise margin is less, the probability of signal failure is high. Therefore, care should be taken in the modeling phase to account for thermal impact on high-speed signals [2].

Some work is done in the literature on electro-thermal co-simulation of 3D integration system for power delivery networks [3]. This work addressed the importance of electro-thermal co-simulation for on-chip scenario only. Authors in [4] presented the characterization of insertion loss in striplines on various substrate materials as function of temperature. Laboratory measurements for standard, mid-, low- and ultra-low loss materials were performed and it was concluded that temperature sensitivity reduces as the material loss decreases. Authors in [5] discussed experimental thermal sensitivity of dielectric constant and dissipation factor. In [6], thermal sensitivity on PCB cross-section was discussed.

In this paper, the work done in [4]-[6] is extended by taking measured dielectric constant and loss tangent values across various materials and extending them to model insertion loss and impedance for traces, vias and surface mount (SMT) pads. The impact of temperature on impedance and loss is studied across various material classifications through simulations.

This paper is organized as below. Section II explains temperature impact on dielectric constant and loss tangent using vendor measurement data and theoretical postulations. Section III presents thermal sensitivity of impedance and loss for transmission lines, vias and SMT pads. Section IV concludes the paper.

II. TEMPERATURE IMPACT ON MATERIALS

In this section, thermal sensitivity of different PCB materials is discussed. In addition, the theory for thermal sensitivity is also presented.

A. Thermal sensitivity of PCB materials

Dielectric materials are classified based on losses. Major classifications typically include ultra-low loss, low-loss, mid-loss and standard loss. These materials are sensitive to temperature. Table 1 shows that variation of *Dk* and *Df* with respect to temperature [7]. It can be seen that high *Dk* materials exhibit larger temperature variation compared to low *Dk* materials.

TABLE I: THERMAL SENSITIVITY DATA OF DIELECTRIC MATERIALS [7]

Materials		0°C	20°C	60°C	100°C	Delta (20-100)°C
Ultra-Low Loss	*Dk*	3.88	3.88	3.89	3.9	0.52 %
	Df	0.0059	0.0064	0.0068	0.0074	15.63%
Low Loss	*Dk*	3.93	3.94	3.96	3.97	0.76 %
	Df	0.0083	0.0091	0.0102	0.0113	24.18 %
Mid Loss	*Dk*	4.21	4.23	4.26	4.3	1.65 %
	Df	0.0113	0.0124	0.0146	0.0173	39.52 %
Standard Loss	*Dk*	4.23	4.26	4.32	4.4	3.29 %
	Df	0.0164	0.0184	0.0234	0.0279	51.63 %

B. Theory for thermal sensitivity of materials

Dielectric constant of materials is defined by equation (1). Here, $\boldsymbol{E}$ represents the applied electric filed to material and $\boldsymbol{E_{in}}$ is induced electric field [8].

$$Dk = \frac{E}{E - E_{in}} \tag{1}$$

When the molecules are polarized by applying the electric field, $\boldsymbol{E}$, it generates a dipole moment. Due to dipole moment of molecules, induced electric filed, $\boldsymbol{E_{in}}$, is formed inside the dielectric material. The polarization vector per unit volume is given by equation (2), where N represents the number of molecules per unit volume, which contributes to dipole moment. Note that, α_e is polarizability and $\boldsymbol{E}$ is applied electric field [8]. Corresponding to the dipole moment, $\boldsymbol{P}$, the charge density and induced electric field are given by equations (3) and (4) [9], where, ρ represents the charge density and $\hat{\boldsymbol{n}}$ is unit vector in equation (3). In equation (4), ∇ (del) operator represents the divergence of induced electric field.

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$$\boldsymbol{P} = N\alpha_e \boldsymbol{E} \quad (2)$$

$$\rho = \mathbf{P}.\hat{\boldsymbol{n}} \quad (3)$$

$$\nabla.\boldsymbol{E_{in}} = \rho \quad (4)$$

Usually, the dipole moment does not reach the saturation level on applying the electric filed. Few molecules have an orientation such that they could cancel the dipole movement of others. With increase in temperature these molecules get the energy and begin to orient in the direction of electric field. Hence, number of molecules that contribute to the dipole moment are increased. Based on the above explanation, equations (2), (3) and (4) can be modified as equations (5), (6) and (7) as the temperature increases. Here, N' is the number of molecules per unit volume after increase in temperature and N' is greater than N.

$$\boldsymbol{P'} = N'\alpha_e \boldsymbol{E} \quad (5)$$

$$\rho' = \boldsymbol{P'}.\hat{\boldsymbol{n}} \quad (6)$$

$$\nabla.\boldsymbol{E'_{in}} = \rho' \quad (7)$$

Thus, the polarization vector magnitude increases, which results in increased charge density and increase in magnitude of induced electric field as per equations (6) and (7). Induced electric field ($\boldsymbol{E_{in}}$) increases as per equation (1) that results in higher dielectric. Thus, we can conclude that the temperature sensitivity is more dominant on materials with higher dielectric constant.

III. TEMPERATURE IMPACT ON SIGNAL IMPEDANCE AND LOSS

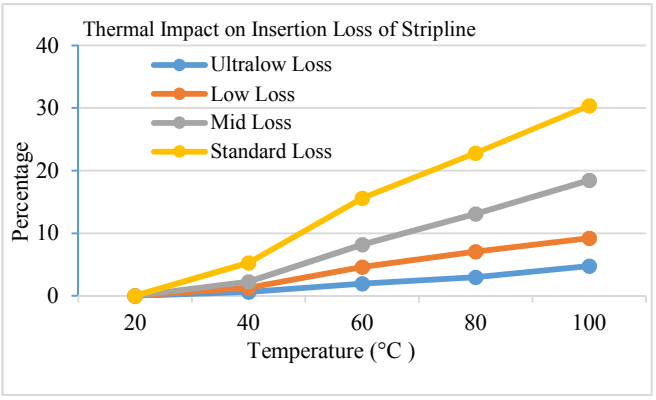
In this section transmission lines, vias, SMT pads are considered to quantify the impact due to thermal variations in a PCB.

a) Transmission Line

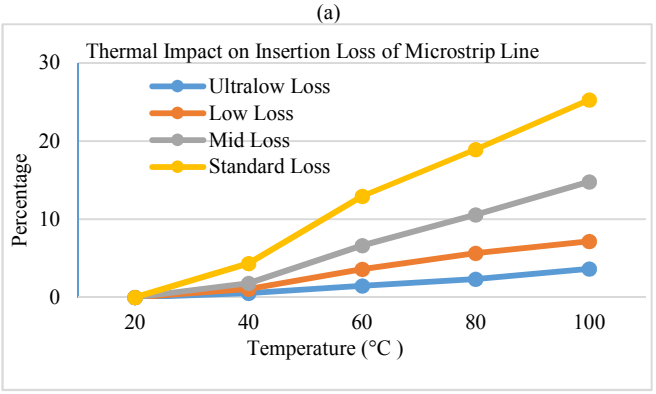
To study the thermal impact on transmission lines, various material classes from standard loss to ultra-low loss are considered. Transmission lines are modeled as per *Dk* and *Df* numbers from Table 1. Geometry for microstrip line includes trace-width of 4.5 mils, spacing of 6 mils, trace thickness of 1.9 mils, prepreg thickness of 3 mils and solder mask of 0.5 mil. The geometry considered for striplines includes trace-width of 4.5 mils, spacing of 6 mils, trace thickness of 1.3 mils, core thickness of 3 mils and prepreg of 6 mils. It is observed that ultra-low loss material is less sensitive to thermal impact as compared to standard loss material. As shown in Fig. 1, ultra-low loss material shows 4.7% and 3.7% change in loss at 16GHz for a temperature change from 20°C to 100°C for stripline and microstrip line, respectively. A standard loss material shows 30.3% and 25.2% change in loss at 16GHz for a temperature change from 20°C to 100°C for stripline and microstrip line, respectively. Thermal sensitivity of impedance is not significant as shown in Fig. 2. As standard loss material is more sensitive to temperature, via and SMT pad are analyzed with standard loss material only for insertion loss and impedance.

b) Via

Vias produce impedance discontinuity when the signal transits from one layer to another. To maintain required impedance different aspects of vias should be considered such as material of the stackup, anti-pad, spacing between the signal vias and signal-to-ground as shown in the Fig. 3. To minimize the impedance discontinuity of vias, designers should clearly understand their thermal sensitivity.

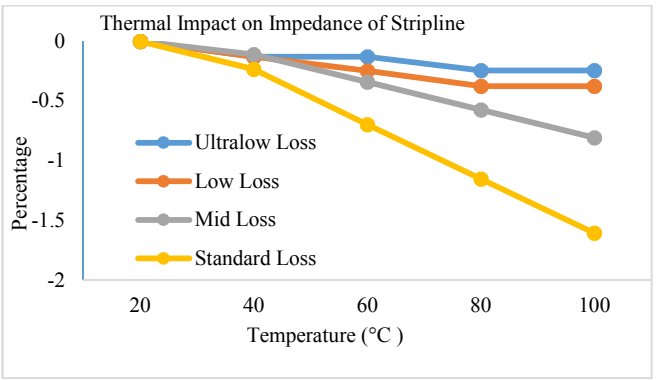


(a)

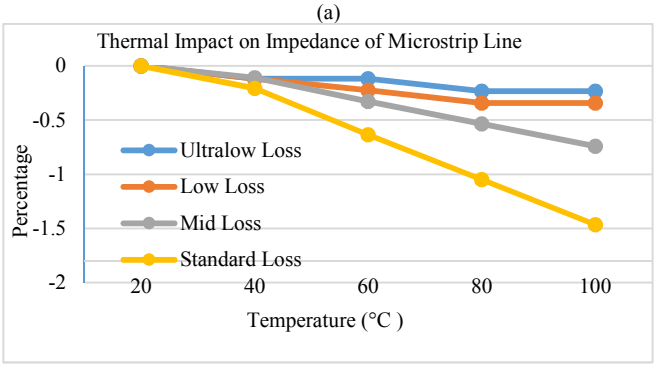


(b)

Fig. 1. Percentage change of insertion loss with temperature (a) Stripline (b) Microstrip line



(a)



(b)

Fig. 2. Percentage change of impedance with temperature (a) Stripline (b) Microstrip line

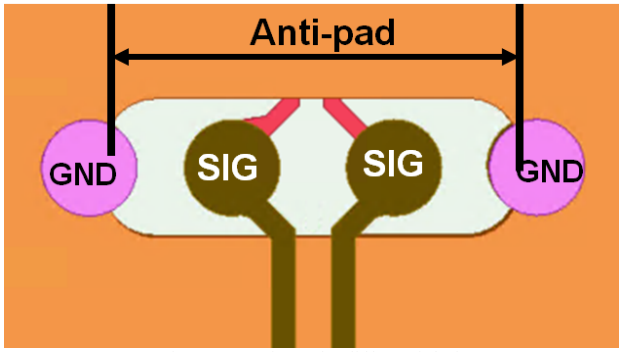


Fig. 3. Top view of a differential via

From Section II, one can observe that the *Dk* of material increases with increasing temperature. Table 2 shows the variation in impedance and insertion loss for a range of *Dk* and *Df* values for a stack-up of 100 mils thickness with signal transiting from top to bottom layer. It is observed that there is 3% variation in impedance and 31% variation in loss at 16 GHz. Thus, thermal sensitivity of vias is similar to that of transmission lines.

TABLE II: VIA IMPEDANCE AND LOSS FOR DIFFERENT DK AND DF

Dk	*Df*	Impedance@ 5ps	% change in impedance	Insertion loss (dB) @16GHz	% change in insertion loss
4.1	0.0075	74-88	--	0.48	--
4.2	0.0142	73.1-87	1.14	0.52	8.34
4.3	0.0217	72.2-85.6	2.72	0.57	18.75
4.4	0.0279	72.1-85.3	3.06	0.63	31.25

c) Surface mount (SMT) pads:

By using SMT pads, electrical components are mounted directly onto the surface of PCB. SMT pads offer higher component density and provide more routing space for inner layers. However, the landing pads in SMT connectors offer large capacitance that can significantly affect their impedance. Table 3 shows the impedance and loss variations for various *Dk* and *Df* for standard loss material. From our analysis, it can be seen that impedance of SMT connector pads varies by 1.5% and insertion loss by ~32%.

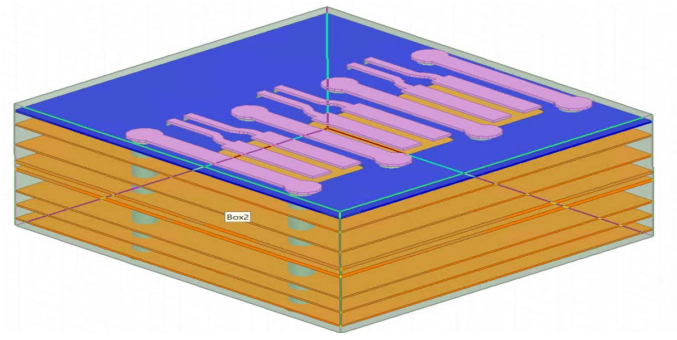


Fig. 4. Surface mount connector pads

TABLE III: SMT IMPEDANCE AND LOSS DIFFERENT DK AND DF

Dk	*Df*	Impedance@ 5ps	% change in impedance	Insertion loss(dB) @16GHz	% change in insertion loss
4.1	0.0075	65.6-91.2	--	0.41	--
4.2	0.0142	65.3-90.7	0.55	0.45	9.75
4.3	0.0217	64.3-90.1	1.2	0.48	17.03
4.4	0.0279	64.1- 89.8	1.53	0.59	31.7

IV. CONCLUSION

In this paper, thermal sensitivity of dielectric materials and its effect on loss and impedance for high-speed PCBs are discussed. The theory behind thermal sensitivity of materials is also discussed, which helps in providing physical insights into this phenomenon. Thermal sensitivity study is done for PCB transmission lines, vias and SMT pads. It is observed that standard loss material is more sensitive to thermal variations as compared with mid-loss, low-loss and ultra-low loss materials. Insertion loss variation of ~30% is observed in transmission lines, vias and SMT pads at 16GHz with standard loss material. Standard loss materials are thermally insensitive for impedance with a ~2-3% variation across transmission lines, vias and SMT pads. Based on our analysis, we conclude that high-speed PCBs need to take thermal sensitivity into account in the early design stages.

V. ACKNOWLEDGEMENTS

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