Analysis of Power Supply Noise Induced Jitter of I/O Subsystems with Multiple Power Domains

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***Abstract*—In high-speed interface designs, multiple power domains are used to improve the performance and minimize noise as well as jitter. Power supply noise induced jitter (PSIJ) is one of major sources of timing uncertainties. To analyze PSIJ, empirical methodologies are often derived in frequency and time domains using the individual DC delay (ps) and sensitivity (ps/mV) of key circuit blocks. In this paper, we examine the validity of PSIJ results from these empirical approaches by comparing those to the results obtained from transistor-based SPICE simulations of complete high-speed data and clock paths such as clock tree, phase interpolator, mux, and buffers under multiple power domains. The accuracy of PSIJ methodology of the overall Input/Output (I/O) subsystem is verified against the combined results of multiple circuit blocks when analyzed separately.**

Keywords— DC delay sensitivity, Input/Output (I/O) subsystem, Multiple power domains Power supply noise induced jitter.

I. INTRODUCTION

Many of the critical circuit blocks of clock and data paths in high-speed serial/parallel interface are sensitive to power supply noise. As such, there may exist several power rails to improve the performance, lower-power consumption and to meet predefined voltage levels in the I/O interface specifications. In this study, three main power rails are considered in the I/O PHY circuits as shown in Figure 1. All the clock circuit blocks use VCCA, I/O registers and pre-drivers use VCC, and the output drivers use VCCIO. These power supplies can be delivered from the same VRM with appropriate filtering at board or package level.

The decision to partition the power supply of an interface often involves power noise and timing impact analyses. The off-chip and/or on-chip power integrity analysis evaluates the self-generated and coupled noises. And, timing analysis assesses the jitter impact due the voltage noises. Figure 2 shows an example of various supply noise generation, noise sensitivity of circuits as well as the jitter sensitivity functions of typical circuit blocks in I/O subsystems.

The power supply noise induced jitter (PSIJ) created by the various circuit blocks can take a significant portion of the total link jitter budget. In order to help circuit/system designers, minimize the PSIJ, efficient empirical simulation methodologies of PSIJ analysis have been widely investigated [1, 2]. In these methods, the PSIJ can be analyzed by equation-based numerical calculations, without time-consuming SPICE simulations of the entire circuit blocks. This paper compares the functional block-based empirical PSIJ analysis and transistor circuit-based SPICE simulation. To verify the jitter transfer function of clock and data paths, the I/O subsystem in an Intel field-programmable gate array (FPGA) is used for transistor-level SPICE simulations. By applying a sinusoidal noise and sweeping the noise frequency, the PSIJ dependency of complete cascaded circuit block on the noise frequency is simulated and compared with the jitter transfer function of the empirical approach of circuit block-based approach.

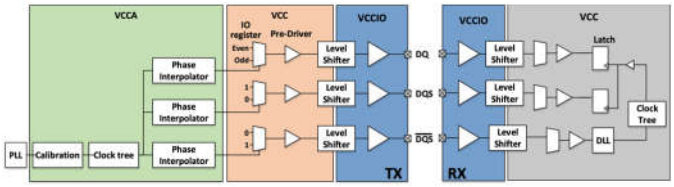

Figure 1: A power supply partition in a typical I/O subsystem for source-synchronous parallel interface.

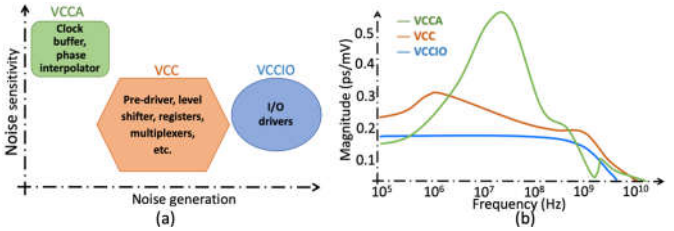

Figure 2: Supply noise partition: (a) noise generation vs. sensitivity, and (b) jitter sensitivity functions for VCCA, VCC, and VCCIO.

The empirical PSIJ analysis consists of deriving a frequency-dependent jitter transfer function (JTF) calculation and modeling of the system-level noise including power distribution network and current noise waveforms as shown in Figure 3. The jitter transfer functions can be calculated with DC delay (ps) and sensitivities (ps/mV) of individual circuit blocks in clock and data paths. As of yet, the jitter transfer function of full-path analysis and comparison have not been accomplished due to the complex design of clock and data paths.

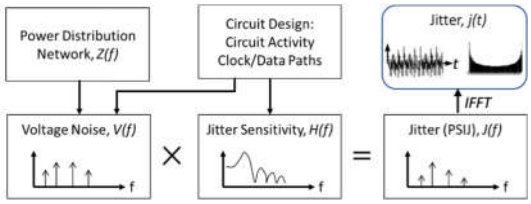

Figure 3: Frequency-domain approach for deriving the power supply noise induced jitter (PSIJ).

II. JITTER TRANSFER FUNCTIONS

1. *Open-loop path jitter*

The jitter transfer function for open-loop paths can be analytically derived by an equation (2) [1, 3]. The DC delay sensitivity (H_0), is defined as the delay change induced by DC voltage changes as described in equation (1). With this DC delay sensitivity and open-loop delay (τ_d) of the circuit block, the frequency-dependent jitter transfer function can be easily calculated as:

$$H_0 = \frac{\tau_{d\,@Vmin} - \tau_{d\,@Vmax}}{Vmax - Vmin}, \quad (1)$$

$$H(f) = \frac{j}{2\pi f \tau_D} H_0 [1 - e^{-j2\pi f \tau_D}]. \quad (2)$$

The magnitude of the jitter sensitivity can be simplified as:

$$|H(f)| = H_0 \left| \frac{\sin(\pi f \tau_d)}{\pi f \tau_d} \right| = H_0 |\mathrm{sinc}(\pi f \tau_d)|. \quad (3)$$

When the path delay is large, the DC sensitivity (H_0) is high, the path is more sensitive to the low-frequency noise. However, the large path delay induces the lower frequency null point in the frequency-dependent jitter transfer function which can make the path less-sensitive to high-frequency noise. Therefore, large path delay does not always induce the worst-case jitter as in static timing analysis (STA) in which longer delay usually means larger timing loss.

2. *Period Jitter of clock signal*

For the clock network analysis, period jitter *(PJ)* is a key parameter because data can be generated and recovered by clock rise and/or fall edges. Period jitter is defined as the deviation of the clock period from its ideal period; thus, the jitter transfer function of *PJ* can be calculated by subtracting the jitter of consecutive edges: rise-to-rise or fall-to-fall edge. From the jitter transfer function of open-loop path in equation (1), the jitter transfer of *PJ* can be expressed by equation (4) and (5) with jitter subtracting term of consecutive edges.

$$H_{period}(f) = H(f)(1 - e^{-j2\pi f T_{clk}}) \quad (4)$$

The magnitude of the jitter sensitivity can be simplified as:

$$|H_{period}(f)| = 2H_0 |\mathrm{sinc}(\pi f \tau_d)| \cdot |\sin(\pi f T_{clk})| . \quad (5)$$

Figure 4 shows the time interval error (TIE), which is the time deviation of rise/fall edge from ideal clock edge position from the open-loop sensitivity equation (4), and period jitter sensitivities by equation (5). With the jitter tracking effect of consecutive edges in PJ, the jitter sensitivity has low value in low frequency region, thus the PSIJ becomes smaller.

In high speed parallel interfaces such as memory and chip-to-chip interfaces, source synchronous clocking, which transmits data and clock (strobe) together, is widely used due to the jitter tracking effect of data and clock at the receivers. In such interfaces, the jitter transfer functions *(JTFs)* of data setup and hold time with source synchronous clocking can be expressed by equations (6) and (7), respectively, considering the phase relation between rising and falling edges:

$$H_{setup}(f) = \frac{j}{2\pi f \tau_D} H_0^D [1 - e^{-j2\pi f \tau_D}] - \frac{j}{2\pi f \tau_C} H_0^C [1 - e^{-j2\pi f \tau_C}] \quad (6)$$

$$H_{hold}(f) = \frac{j}{2\pi f \tau_D} H_0^D [1 - e^{-j2\pi f \tau_D}] - \frac{j}{2\pi f \tau_C} H_0^C [1 - e^{-j2\pi f \tau_C}]\, e^{-j2\pi f T_{Bit}}, \quad (7)$$

where H_0^D and H_0^C is DC sensitivity of data and clock path, τ_D and τ_C are data and clock delays, and T_{Bit} is the unit interval (UI).

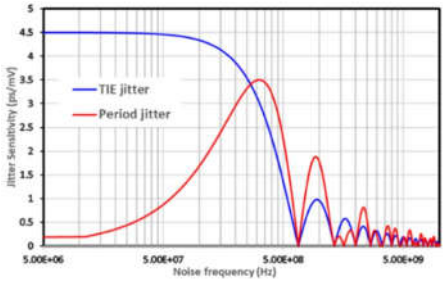

Figure 4: Jitter transfer function of TIE and PJ when the delay (τd) is 1.5ns and clock frequency (1/Tclk) is 1.6GHz.

III. SPICE SIMULATION RESULTS AND CORRELATION

To verify the jitter transfer function of clock and data paths, the I/O subsystem in an Intel FPGA are used for transistor-level SPICE simulations. As shown in Figure 1, the clock is generated from PLL and it goes through calibration circuit, clock tree and phase interpolator for the clock distribution and phase alignment. With the distributed clock, data and strobe signals are generated in IO register blocks. The data and strobe signals are then reshaped in pre-drivers and output buffers to transmit the signals through the channel. Because of the voltage difference between core blocks and output buffers, voltage level shifter is implemented in the design. The data and strobe signals are transmitted together in source synchronous clocking systems with 90-degree phase shift between data and strobe.

1. *SPICE simulation setup*

The full path circuit blocks from PLL out to output buffers are extracted as SPICE post-layout netlist and it is used for transient simulations. To measure the delay, τ_D, and DC sensitivity, H_0, which are required for the jitter transfer function calculation, the delay values of each block are measured at different DC voltages. In our analysis, we only focused on the PSIJ of clock and data paths in the PHY core blocks, and the output buffer power-supply voltage of VCCIO, which is related to simultaneous switching output (SSO) noise, is connected to ideal voltage of 1.2V. In addition, ideal loading capacitors of 1pF are applied to the output buffers to exclude the channel effect. To simulate the jitter transfer function with the SPICE netlist, a sinusoidal noise signal is applied to power supply nodes while sweeping frequency. The PSIJ impacts to the clock period jitter or data eye-opening are measured at the output buffer.

2. *Delay and DC Sensitivity*

Figure 5 shows the measured circuit delays of each block at different voltages. It is seen that the delay decreases as supply voltage increases and the DC sensitivity (H_0) can be calculated using the equation (1).

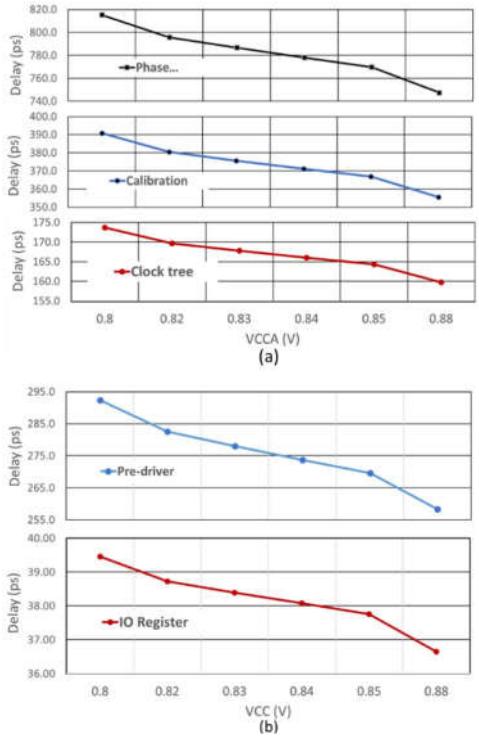

Figure 5: Circuit block delay simulations at different voltages.

3. *Clock period jitter correlation*

In the SPICE simulation, period jitter (PJ) of the strobe signal is measured at the output buffer with varying VCCA or VCC noise frequency. Figure 6 compares the SPICE results and empirical PSIJ values, where sinusoidal noise is applied to the SPICE simulations and equation (4) is used for the empirical jitter transfer function. The frequency-dependent period jitter characteristics are well correlated between the empirical method and SPICE results. However, there are minor mismatches due to the non-linear delay sensitivity and numerical errors in the eye-opening measurements of the simulations.

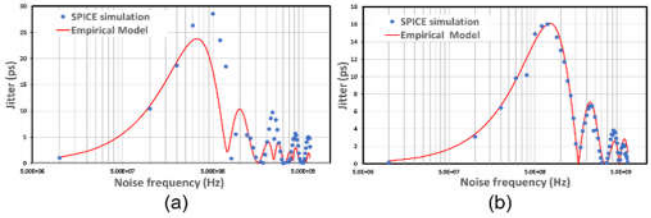

Figure 6: Clock (strobe signal) period jitter as a function of (a) VCCA noise frequency and (b) VCC noise frequency.

4. *Open-path jitter correlation*

With the same SPICE simulations, data signal jitter induced by VCCA or VCC noise is measured and compared with empirical PSIJ analysis results as shown in Figure 7. To analyze open-path jitter characteristics, the data jitter is measured from the eye-diagram with the ideal clock trigger. Jitter transfer function has *sinc* function shape as in equation (3) and frequency-dependent characteristics are well correlated.

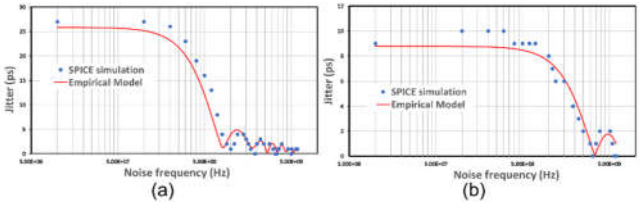

Figure 7: Data jitter without strobe signal triggering as a function of (a) VCCA noise frequency and (b) VCC noise frequency

5. *Data jitter in source-synchronous clocking*

In source synchronous clocking systems, the data and clock jitter can be tracked out when the noise frequency is relatively low, and the specific phase relationship can be met as described in equations (5) and (6). Figure 8 shows SPICE and empirical PSIJ results in source synchronous clocking systems. To consider the jitter tracking, data eye-diagram is triggered by strobe signals in the SPICE simulations. Because the mismatch between SPICE and empirical analysis in data and strobe signals can be accumulated, the jitter magnitude and null points causing low jitter values have discrepancy, however overall frequency-dependent trends are in a relatively good agreement.

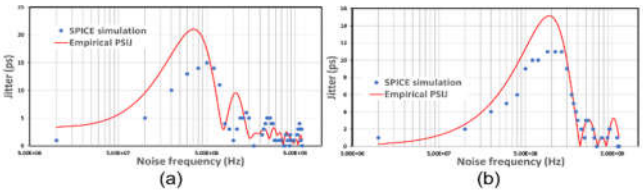

Figure 8: Data jitter with strobe signal triggering as a function of (a) VCCA noise frequency and (b) VCC noise frequency.

IV. Conclusions

In this paper, the correlations of the SPICE simulation and empirical methodology for power supply noise induced jitter (PSIJ) are presented. Using the I/O subsystem circuit blocks in the FPGA, data and strobe jitters are analyzed by applying sinusoidal noise profiles. By sweeping the noise frequency of each power rail, the jitter transfer function of circuit blocks in each power rail can be measured and correlated with the empirical equations. The strobe signal period jitter, open-loop data path jitter, and data jitter in the source-synchronous clocking are examined through both the SPICE simulations and the empirical PSIJ analysis. The frequency dependent jitter characteristics are well correlated; however, the discrepancies of magnitude and null points are observed, which can be due to the inaccurate data and strobe delay modeling. From the results, the empirical PSIJ analysis methodology mainly focusing on jitter transfer functions is verified.

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