SI Model to Hardware Correlation on a 44 Gb/s HLGA Socket Connector

Pavel Roy Paladhi[1*], Yanyan Zhang[1], Junyan Tang[1], Daniel Rodriguez[1], Jose Hejase[2#], Sungjun Chun[1], Wiren Becker[1], Brian Beaman[1], and Daniel Dreps[1]

1. *IBM Corporation,* Austin, TX 78758
2. *Nvidia Corporation*, Austin, TX 78717
 # Contributions to this work completed prior to April 2020 while with IBM Corporation
* Pavel.Roy.Paladhi@ibm.com

***Abstract*— A comprehensive signal integrity model to hardware correlation study on an improved, 44 Gb/s capable, hybrid land grid array (HLGA) socket connector design is presented. The connector only design SI performance is shown through 3D electromagnetic (EM) modelling. Details of the test vehicle designed to carry out the connector hardware evaluation are shown. Simulation modelling and experimental results of the test vehicle inclusive of the connector are presented and compared. The systematic testing ensures that the new component performs up to its required specifications which ensures successful operation at the system level.**

I. Introduction

Over the past few decades, high speed buses in server computers have evolved drastically with increasing speeds of operation and larger data bandwidths. The trend of achieving higher speeds and bandwidth continues to drive innovation in design and technology in its support. With the emergence of new technologies and component designs, carrying out validation testing of their performance remains an essential part of their realization [1].

To maintain the high speed data signaling integrity, the channel carrying the data between the transmitter and receiver has to achieve acceptable signal integrity (SI) requirements in the form of: insertion loss (IL), return loss (RL), impedance profile and crosstalk isolation properties [2]. The high speed channel topologies can vary largely and depend on the architecture of the high speed bus or the system requirements/implementation. They can have any combination of interconnects such as substrate packages, connectors, cables, single or multiple printed circuit boards (PCB), etc. Different types of connectors are used in channel topologies dependent on the need. Some can connect cables to boards, while others can connect boards to substrate packages etc. Connectors can have deleterious effects on the channel performance if not designed or selected properly. At higher speeds, the challenges increase proportionately.

An important type of connectors is the Hybrid Land Grid Array (HLGA) socket connector which connects a chip substrate package to a PCB, commonly: CPU to a server computer motherboard. HLGA connectors are soldered to the motherboard on the bottom side while the package is connected through a spring-loaded assembly on the top side of the HLGA connector. The advantage of the detachable package is that a defective CPU can be removed without changing the whole motherboard as would be the case in a direct attach BGA soldered package to a board. The industry has seen a considerable drive towards improving existing HLGA connectors to function at higher speeds. As an example, in an earlier work, some of the authors in this work had presented an improved HLGA connector design which can support data rates up to 50 Gb/s [3].

Before system integrating new connectors designed to achieve required SI metrics, the component must be validated through design modelling and lab measurement correlation. To assist in doing this, test vehicles are designed to measure performance of the component and validate the design. In this work: (1) connector only SI metrics are shown for a 44 Gb/s capable new connector from 3D EM modelling, (2) details on the design and development of a test vehicle to validate the HLGA connector design are presented and (3) measurements of the HLGA connector as part of this test vehicle are presented along with their correlation with simulation modelling data and discussion validating the design success.

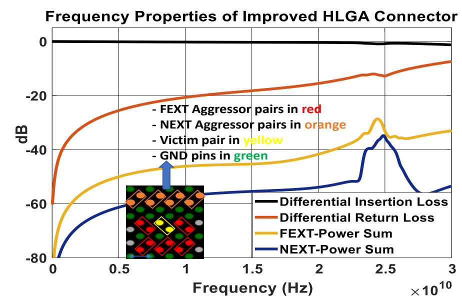

Figure 1. Improved HLGA Frequency properties from 3D modelling.

II. Improved HLGA Design

The frequency response of the improved connector design only model is shown in Fig. 1, assuming a 42.5 Ohm port reference impedance. It is worthy to note that this connector was designed for 85 Ohm differential impedance applications but can support up to 100 Ohm impedance applications. Up to 22 GHz, the differential insertion loss (DIL) is less than 0.4 dB and the differential return loss (DRL) is less than 14 dB. The differential near end crosstalk (NEXT) and far end crosstalk (FEXT) power sums, shown for the signal/ground pin distribution in the inset of Fig. 1, are respectively less than -50

978-1-7281-6161-7/20/$31.00 ©2020 IEEE

dB and -38 dB. The frequency responses show that the connector can operate with good signal integrity up to a frequency of 22 GHz, i.e. 44 Gb/s data rate. Based on this connector design, a test vehicle to carry out measurement to hardware correlation validation of the connector was designed.

III. HLGA Test Vehicle (TV) Planning

An HLGA connector would prevent a direct and isolated measurement of the connector itself on a traditional measurement setup. The TV should be designed in a way so as to be able to measure the properties of the HLGA connector accurately and with minimal interference due to the added traces and connections as part of the TV setup. Furthermore, test points should be efficiently chosen such that all required metrics can be extracted from a minimal set of measurements. With the SI performance evaluation as the primary consideration, the TV is designed to measure IL, RL, impedance and crosstalk metrics of the HLGA connector. A brief description of the TV follows.

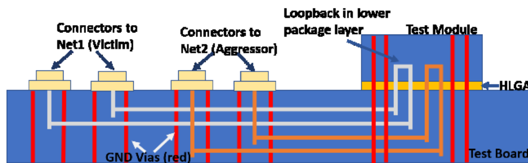

Figure 2. Schematic: HLGA TV showing loopback nets.

The HLGA TV consists of: a PCB board on which the HLGA connector is soldered, the substrate package module which can be mounted on the HLGA connector and the heat sink assembly which provides the mounting capability of the module to the HLGA connector similar to that in a full system.

To measure the frequency domain properties of the HLGA connector, a set of differential-ended loopback nets were designed to be measured with a VNA. An illustrative representation of these test nets in the TV is shown in Fig. 2. The nets originate on the board, outside the HLGA footprint area at SMK connectors where the VNA calibration cable can be directly connected. The general path of the nets is as follows: they breakout from the on-board SMK connectors in the uppermost internal signal layer on the PCB as differential striplines, and then pass through the HLGA connector to the package above. In the package, there is a short trace length in the lower most build up layer which turns back into the HLGA and out into the PCB. The PCB and package wiring layers were chosen to minimize the effect from their respective transition vias from/to the HLGA connector itself. A total of six differential loopback nets were put in the TV. Furthermore, the signal pin locations in the HLGA connector are crucial to get meaningful test data. They were placed in a way to capture representative crosstalk effects which would be observed in an actual system design high speed differential pin distribution. Six differential loopback nets were included in the TV: one victim, two near-end crosstalk aggressors and 3 far-end crosstalk aggressors to evaluate the crosstalk isolation in the HLGA. Fig. 3 shows the top view of the TV. The SMK connectors for the victim net have been circled in the figure. The package (shown in the top right inset) and the heat sink assembly have been removed to show the HLGA connector. The internal wiring for the loopback nets in the pin area of the HLGA connector is shown in the lower inset figure. More details on them are given in the next section. Through the SMK connectors, IL measurement of the six differential pairs and any crosstalk measurement between them can be performed.

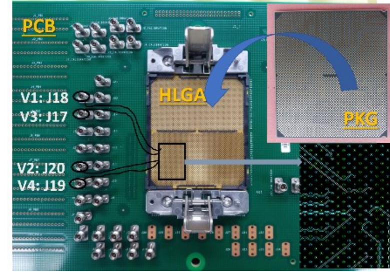

Figure 3. Top view of HLGA TV.

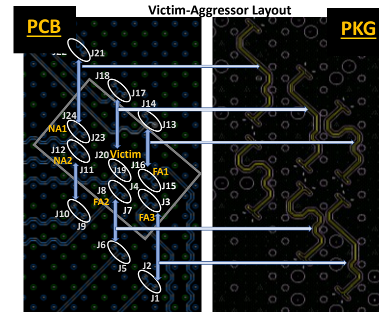

Figure 4: Net layout and grouping for model subdivisions: PCB-HLGA-Package pin transition area subdivided into three sections.

To do a correlation with measurement data, all six loopback nets were needed to be modeled with a 3D EM solver. In order to avoid excessive time and computational complexities, the full structure of the TV was modelled by parts in Ansys HFSS. Then the resulting s-parameters were cascaded to obtain the full channel response. For modelling purposes, the PCB wiring was divided into two zones: open area wiring outside of the HLGA shadow and pin area wiring under the HLGA connector. The other part of the model is the crucial area of the HLGA assembly. In particular, the splitting of the HLGA assembly needed to be done with care to ensure the splitting of the model does not compromise the crosstalk phenomenon in the split models and maintains field continuity. This HLGA assembly contains three main sections: the PCB via, the HLGA connector and the package wiring. It is worthy to note that the HLGA connector model which was used in the modelling of the test nets is the same one for which data was presented for in Section II. This area to be split is shown in Fig. 4 below. The left picture shows the pin area wiring in the PCB section. It shows the transition vias for all the six differential nets. There are six via pairs for going up through the HLGA and six others for coming down (to complete the loopback nets' nature). The upward and downward via pairs for each net have been identified and their connection traces in the package are shown on the right. The rectangular area identified on the left is the key section where the crosstalk phenomena occur. This section is modelled as a single unit to preserve the crosstalk effects. This captures the crosstalk effect from two aggressors separated from the victim with a double-ground isolation (as designed for NEXT in the system) and from three other aggressors with single-ground

separation (as designed for FEXT in the system). Within the box, the NEXT aggressors are marked as NA1 and NA2. The FEXT aggressors are marked as FA1, FA2 and FA3. Outside the rectangular box, the 3 via pairs above and 3 pairs below are modelled as two other separate sections. Beside each via in the left figure, the ‘J#’ number identifies the corresponding connector placed on the PCB, e.g. J17-J18 and J19-J20 are the i/p and o/p connector pairs respectively for the victim net. Measurements were taken in the TV to measure the cross talk between the victim and all the aggressors.

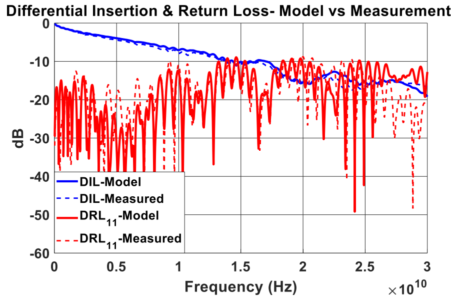

Figure 5. Victim DIL and DRL comparison between measured and modelled data.

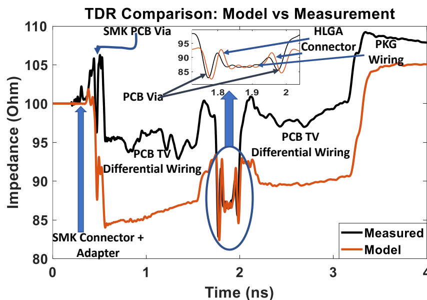

Figure 6. Impedance profile comparison between measured and modeled data of the victim net. TDR is computed from the s-parameters.

IV. Model to Measurement Correlation

S-parameter measurements on the TV were made using Anritsu’s VectorStar VNA. DIL, DRL, impedance profile (calculated from s-parameter), FEXT and NEXT measurements were carried and compared to modelling data. The VNA calibration plane is at the top of the 50 Ohm SMK connectors. The models include the full path for each of the nets starting and ending at the SMK connector tips. Hence, de-embedding of the traces and connectors in the PCB was not needed, in part helping minimize de-embedding inaccuracies, though de-embedding traces existed on the TV PCB. Since the SMK connectors are 50 Ohm and the purpose of this section is solely for comparison, the data is presented for 50 Ohm port reference impedance as opposed to converting to 42.5 Ohm port reference impedance. Fig. 5 shows a comparison of the DIL and DRL in the TV with modelled data for the victim net. A very good correlation is observed for DIL. For DRL, the correlation is good with the peaks and dips matching up well. In Fig. 6, an impedance comparison of the victim channel is shown through TDR plots calculated from the measured and modelled s-parameters using a 25 ps rise time. The different regions of the TV are identified in the figure. The middle section with the two HLGA connector sections connected by package wiring shows very good correlation. The deviation observed in the PCB wiring region can be alluded to fabrication tolerances resulting in deviations in trace dimensions from design values intended to produce 85 ohms differential impedance. Figs. 7 and 8 respectively show FEXT and NEXT comparisons. For FEXT, the nearest and farthest aggressors’ responses are compared and clearly can be distinguished by the difference in their crosstalk energy levels. In both FEXT and NEXT plots, the correlation is good. The deviations in the dB though observable are considerably low taking into consideration the absolute dB levels.

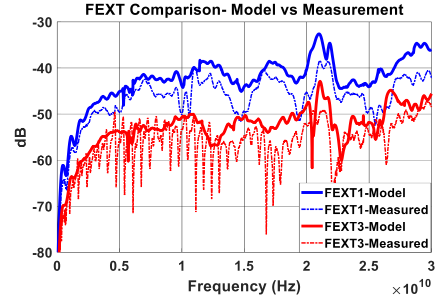

Figure 7. FEXT comparison between measured and modelled data.

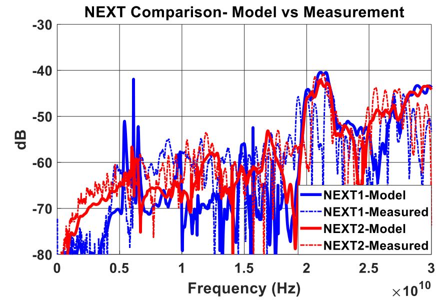

Figure 8. NEXT comparison between measured and modelled data.

V. Conclusion

In this paper, a model to hardware correlation study, including test vehicle design and implementation, to validate the performance of a new and improved 44Gb/s capable HLGA connector design. Modelling studies and measurements showed good correlation for the tested SI parameters, building confidence on the validity of the connector design, for which its good performance in isolation from simulation was shown in the Section II. The comparisons clearly show that the new connector design manufactured are consistent with the good performance in simulation. With the need to perform at higher speeds from one generation to another, studies focusing on validating new and/or improved designs/technologies prior to system implementation are becoming more important.

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