A Shielded-Block Preconditioner for Reduced-Domain Layered-Medium Integral-Equation Methods

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***Abstract*—A shielded-block preconditioner is adopted to reduce the iteration count of layered-medium integral-equation (LMIE) solvers that include dense metallization layers in the Green's functions. Similar to other sparse block preconditioners, the preconditioner is suitable for integration with parallel LMIE solvers to facilitate the analysis of full-size package models. The performance of the preconditioner is demonstrated by analyzing a via array extracted from a full-size package model.**

Key Words—Integral-equation methods; layered media.

I. Introduction

Layered-medium integral-equation (LMIE) methods avoid discretizing and solving for fields in dielectric substrates [1]–[3] and can be enhanced significantly by using parallel iterative solvers, fast matrix-vector multiplication algorithms, and sparse preconditioners [4]. Yet, when used for electromagnetic analysis of full-scale models of modern electronic packages, typical LMIE methods result in large, dense, and poorly conditioned systems of equations; this is in part because they require discretization of currents in/on all conductors.

Reduced-domain LMIE methods, which model contiguous power/ground planes (reference conductors) as highly or perfectly conducting layers in the background medium, reduce the computational domain further and can also yield better conditioned systems of equations; this can be attributed to the fast decay of Green's function components corresponding to horizontal-source to horizontal-observer interactions [3]. When combined with small-aperture modeling methods [5]–[7], reduced-domain LMIE methods can also efficiently analyze complex full-size models by decomposing the package to various subdomains (Fig. 1). For models that include vertical via transitions, however, the Green's function components that correspond to vertical via-to-via interactions (for vias between two highly conductive layers) decay even slower with distance compared to those in the typical LMIE approach [4]. This creates significantly larger off-diagonal matrix entries and can yield rather poorly conditioned matrices that require large number of iterations when iterative solvers are used. This article presents a shielded-block preconditioner [8] that is well-suited for integration into parallel reduced-domain LMIE solvers and demonstrates its effectiveness for a subdomain consisting of a PTH via array at a core dielectric layer.

II. Formulation

Consider a full-size electronic package model that is decomposed into smaller subdomains bounded vertically by one or two highly conductive layers (Fig. 1). The fields in these subdomains are coupled through cutouts in reference conductors; using various small-aperture models to accurately couple the computations for the different subdomains is an important topic of study discussed elsewhere [5]–[7]. The focus of this article is instead on the full-wave analysis in a certain type of subdomain; specifically, consider a subdomain consisting of two contiguous reference conductors, filled by a core dielectric, and connected by a PTH via array (Fig. 2). The structure is modeled as N^{via} vias residing in a planar layered medium background stratified to $K=5$ layers in the *z* direction with infinite extent horizontally. Each layer $k=1,...,K$ is assigned an isotropic material with permittivity ε_k, conductivity σ_k, and permeability μ_k, where $k=2,4$ are two highly conductive layers to approximate the reference conductors and $k=3$ is the core dielectric layer embedding the PTH vias.

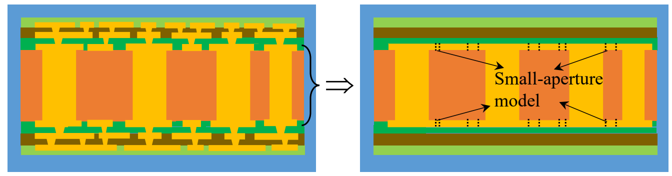

Fig. 1. A subdomain problem consisting of a plated-through-hole (PTH) via array is extracted from a full-size electronic package using small-aperture models to account for coupling through cutouts at the reference conductors.

Consider the extraction of 2-port network parameters for a signal via in the presence of all other structures. Enforcing the standard Leontovich impedance boundary condition on all via surfaces S^{via} to account for finite conductivity and surface roughness effects, yields the LMIE for this subdomain problem:

$$\hat{\mathbf{n}}\times\hat{\mathbf{n}}\times\mathcal{L}^{\text{EJ}}(\mathbf{J},\mathbf{r})+Z_S(\mathbf{r})\mathbf{J}(\mathbf{r})=0 \quad \forall\mathbf{r}\in S^{\text{via}} \tag{1}$$

Here, $\mathbf{J}$ is the surface current density, $\mathcal{L}^{\text{EJ}}$ is the layered-medium electric-field integral-equation operator, and Z_S is the local surface impedance term [3][4]. To extract the network parameters, the delta-gap port model is used: ports 1 and 2 are defined as the circular edges at the top and bottom surface of the signal via and all ports are terminated at 50-Ω loads. The signal via is driven by two different excitations; for the *p*-th excitation (*p*=1 or 2), a 1 V time-harmonic voltage source is placed at port p; i.e., $\mathcal{L}^{\text{EJ}}(\mathbf{J},\mathbf{r})=\delta(\mathbf{r}-\mathbf{r}_p)\hat{\mathbf{h}}_p$ is enforced, where $\mathbf{r}_p$ are points on the circular edges of port p and $\hat{\mathbf{h}}_p$ is the unit normal vector pointing from the port into one of the reference planes.

To solve the LMIE in (1), $\mathbf{J}$ is expanded with a total of N Rao-Wilton-Glisson (RWG) [9] functions on the vias and half-RWG functions on the circular edges touching the highly conductive layers. Galerkin testing of the LMIE in (1) yields the linear system of equations: $\mathbf{Z}_{N\times N}\mathbf{I}_{N\times 1}=\mathbf{V}_{N\times 1}$, where $\mathbf{Z}$, $\mathbf{I}$, and $\mathbf{V}$ are the impedance matrix, unknown coefficient vector, and right-hand-side vector. As there are N^{via} disconnected structures (vias), $\mathbf{Z}$ can be organized into $N^{\text{via}}\times N^{\text{via}}$ blocks

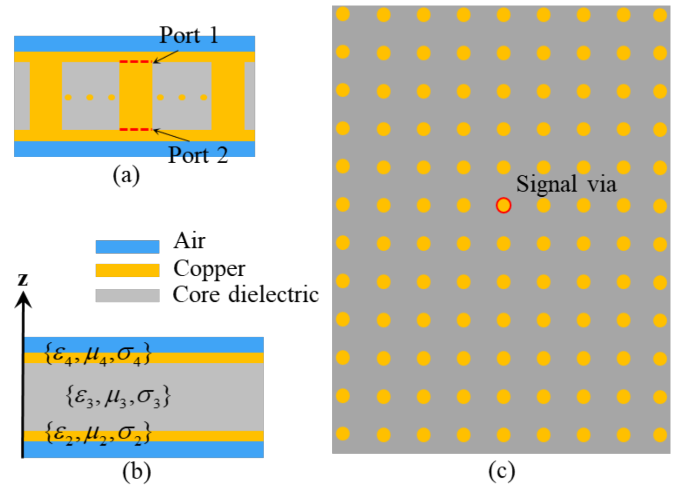

Fig. 2. A PTH via array with N^{via} vias embedded in a core dielectric layer: (a) cross-section view of the array and the port configuration. (b) The *K*=5-layer background model used by the reduced-domain LMIE method. (c) Top-down view of the via array with the boundary edges of the signal via marked in red.

$$\mathbf{Z}=\begin{bmatrix} \mathbf{Z}_{11} & \cdots & \mathbf{Z}_{1a} & \cdots & \mathbf{Z}_{1N^{\text{via}}} \\ \vdots & \ddots & & & \vdots \\ \mathbf{Z}_{a1} & \cdots & \mathbf{Z}_{ab} & \cdots & \mathbf{Z}_{aN^{\text{via}}} \\ \vdots & & & \ddots & \vdots \\ \mathbf{Z}_{N^{\text{via}}1} & \cdots & \mathbf{Z}_{N^{\text{via}}a} & \cdots & \mathbf{Z}_{N^{\text{via}}N^{\text{via}}} \end{bmatrix} \quad (2)$$

Here, each $N_a \times N_b$ sized block $\mathbf{Z}_{ab}$ stands for the interaction between the observer via *b* (with N_b testing functions on it) and the source via *a* (with N_a basis functions on it). To reduce the iteration count and improve solution accuracy, the system of equations can be preconditioned from the left as:

$$\mathbf{Z}^{\text{precon}}\mathbf{Z}\cdot\mathbf{I}=\mathbf{Z}^{\text{precon}}\cdot\mathbf{V} \quad (3)$$

The proposed preconditioner is constructed by assigning each via a "shielding region" by identifying a group of neighboring vias as its "shield" [8]. These regions are dictated by a predefined parameter ρ^{s}: the axial distance between a via and other vias in its shield is less than ρ^{s} (Fig. 3). Let N_a^{via} and N_a^{SB} denote the total number of vias and basis functions enclosed in the *a*-th via's shielding region, and $\mathbf{Z}_a^{\text{SB}}$ denote the $N_a^{\text{SB}} \times N_a^{\text{SB}}$ impedance submatrix that stores all the interactions within the shield; this submatrix can be formulated using the via-to-via interaction blocks in (3):

$$\mathbf{Z}_a^{\text{SB}}=\begin{bmatrix} \mathbf{Z}_{\mathbf{S}_a[1]\mathbf{S}_a[1]} & \cdots & \mathbf{Z}_{\mathbf{S}_a[1]\mathbf{S}_a[N_a^{\text{via}}]} \\ \vdots & \ddots & \vdots \\ \mathbf{Z}_{\mathbf{S}_a[N_a^{\text{via}}]\mathbf{S}_a[1]} & \cdots & \mathbf{Z}_{\mathbf{S}_a[N_a^{\text{via}}]\mathbf{S}_a[N_a^{\text{via}}]} \end{bmatrix}_{N_a^{\text{SB}}\times N_a^{\text{SB}}} \quad (4)$$

Here, the selection array $\mathbf{S}_a$ stores the indexes of the N_a^{via} vias enclosed in the shield of the *a*-th via; the first via in each shielding region is set to the shielded via itself, i.e., $\mathbf{S}_a[1]=a$. Then, $\mathbf{Z}_a^{\text{SB}}$ for each via *a* is inverted (capturing the self and mutual via interactions in the shielding region of the via). Next, the first N_a rows of each inverted shielded-block submatrix is collected and these rows are arranged into rectangular-block-diagonal form (Fig. 3). Specifically, $\mathbf{Z}^{\text{precon}}$ is filled as:

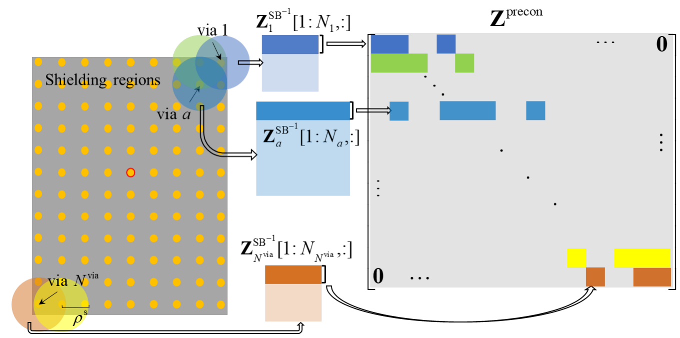

Fig. 3. Shielding regions for the via array and the corresponding matrix pattern for the shielded-block preconditioner.

$$\mathbf{Z}^{\text{precon}}\left[\mathbf{C}_a[1:N_a],\,\mathbf{C}_a[1:N_a^{\text{SB}}]\right]=\mathbf{Z}_a^{\text{SB}^{-1}}[1:N_a,1:N_a^{\text{SB}}] \quad (5)$$

where $\mathbf{C}_a$ simply maps the (local) indexes of the submatrix $\mathbf{Z}_a^{\text{SB}}$ to the (global) indexes of the impedance matrix $\mathbf{Z}$.

Like other sparse preconditioners, using $\mathbf{Z}^{\text{precon}}$ requires two major computational steps: (i) inverting all shielded-block submatrices to setup the preconditioner, which requires $\mathcal{O}(\sum_a [N_a^{\text{SB}}]^3)$ operations and $\mathcal{O}(\sum_a N_a N_a^{\text{SB}})$ memory space; (ii) multiplying the inverted matrices at each iteration, which requires $\mathcal{O}(\sum_a N_a N_a^{\text{SB}})$ operations per iteration. Therefore, the preconditioner is well-suited for problems with many small disconnected geometries ($N_a \ll N$), e.g., PTH via or stitching via arrays in full-size package models.

III. Numerical Results

To demonstrate the performance of the shielded-block preconditioner, four increasingly larger PTH via arrays are analyzed with a parallel iterative LMIE solver [4] and the resulting number of iterations are compared to those from the element-diagonal [4] and block-diagonal preconditioner. Here, the block-diagonal preconditioner is implemented by setting ρ^{s} to a very small number such that $\mathbf{Z}_a^{\text{SB}}=\mathbf{Z}_{aa}$. In these examples, the number of vias N^{via} is increased from 25 to 1681, with a uniform spacing of 1 mm in the *x* and *y* directions. Every via is a circular cylinder with 750-μm height, 250-μm diameter cylinder, and $\sigma_c=4.5\times10^7$ S/m conductivity. The signal via is always assigned to the center via within these arrays. All vias are embedded in a (core) dielectric layer with relative permittivity $\varepsilon_r=3.5$, loss tangent $\tan\delta=0.2$, and relative permeability $\mu_r=1$. The two reference conductors are modeled as 30μm- thick metal layers and the same conductivity as the vias (Fig. 4). Surface-roughness of the conductors is not modeled. After triangularization, the circular cylinder vias are meshed to 12-edge polygon cylinder vias resulting in 228 unknowns for each via ($N=228N^{\text{via}}$); thus, the number of unknowns increases from $N=5700$ to 383 268 as the number of vias increases. An FFT-accelerated TFQMR solver combined with different preconditioners is used, and the relative residual error is enforced to be smaller than 10^{-4}. The shielding region parameter ρ^{s} is set to 1.1 mm for all vias, i.e., $N_a^{\text{via}}=5$ for all non-boundary vias (Fig. 3).

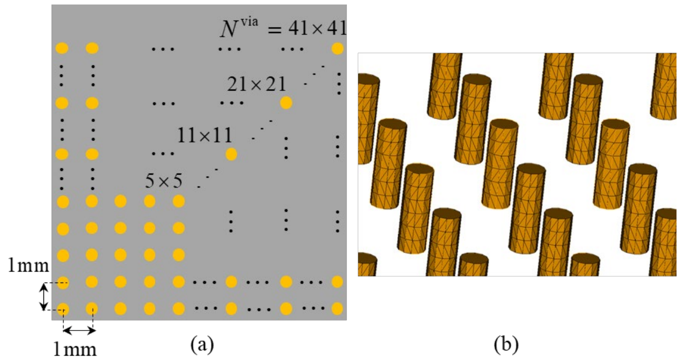

Fig. 4. Four via arrays: (a) top-down view of the 5×5, 11×11, 21×21, and 41×41 element arrays with 1 mm uniform spacing, (b) cross-section view of the PTH via arrays embedded in a 5-layer background, and (c) the mesh view of the vias with the reduced-domain LMIE method.

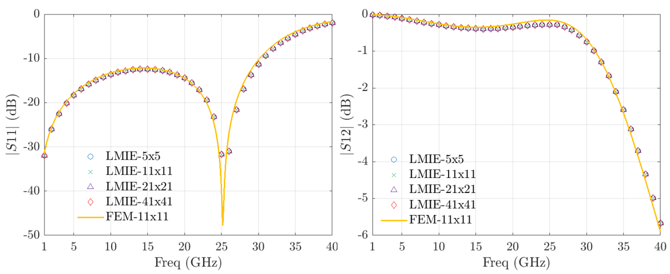

Fig. 5. $|S_{11}|$ and $|S_{12}|$ parameter for the four PTH via array problems obtained from the reduced-domain LMIE method and an FEM solver.

First, the *S*-parameters of the signal via for these four problems are extracted in the 1 to 40 GHz range in Fig. 5. Both $|S_{11}|$ and $|S_{12}|$ parameters are visually identical in all problems, which indicates the effect of the nearby vias on the signal via remains unchanged beyond 25 (5×5) vias. As the frequency increases, less energy can be coupled through the signal via ($|S_{12}|$ drops significantly), while stronger reflection is observed above 30 GHz. Fig. 5 also shows the 11×11 via array's parameters found by a commercial finite-element-method solver, whose results for $|S_{12}|$ and $|S_{11}|$ parameters are within 0.25 dB and 1.5 dB of the LMIE ones at all sampled frequencies, respectively (except at 25 GHz for $|S_{11}|$).

Next, the performance of the three different preconditioners is studied by contrasting the number of iterations they require. As the number of vias increases, the shielded-block preconditioner's iteration count grows the slowest and the method requires much smaller number of iterations (Fig. 6). The iteration counts are also reported at all sampled frequencies in Fig. 6 and the shielded-block preconditioner is found to require <25 iterations for all cases. The computational costs of the shielded-block preconditioner are sensitive to the shielding parameter ρ^{s} and mesh density on the vias, i.e., N_a. For the above examples, the shielded-block diagonal preconditioner requires $\sim10\times$ operations for setting up the preconditioner and $\sim2\times$ operations to apply it at each iteration compared to the block-diagonal preconditioner. Overall, when the mesh edge lengths on the vias are $\approx\lambda/20$ (λ: the wavelength at the core layer at 40 GHz), the preconditioner setup and multiplication costs are comparable to the impedance-matrix fill and matrix-vector multiplication costs, respectively.

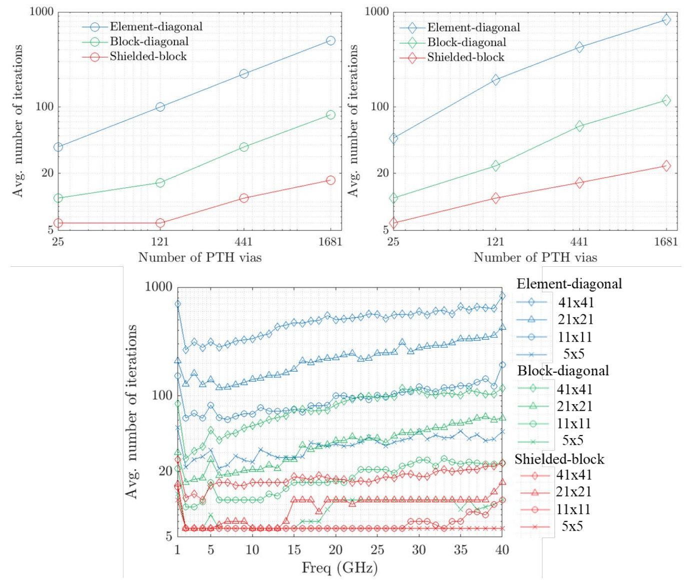

Fig. 6. Comparison of the iteration counts among three preconditioners: Top: average number of iterations vs. problem size at 20GHz (left) and 40 GHz (right); Bottom: average number of iterations for the entire frequency band.

IV. Conclusion

A shielded-block preconditioner was adopted and shown to improve the performance of reduced-domain LMIE solvers when applied to subdomains that contain many vertical-source to vertical-observer interactions. The preconditioner can be efficiently parallelized and easily integrated into the parallel reduced-domain LMIE solvers.

References

[1] S. Sharma, U. R. Patel, and P. Triverio, "Accelerated electromagnetic analysis of interconnects in layered media using a near-field series expansion of the Green's function," in *Proc. IEEE 27th Conf. Elect. Perform. of Electron. Packag. Syst. (EPEPS*), Oct. 2018.

[2] G. Bianconi and S. Chakraborty, "Efficient and robust dyadic Green's function evaluation algorithm for the analysis of IC packages and printed circuit board," in *Proc. IEEE 25th Conf. Elect. Perform. of Electron. Packag. Syst. (EPEPS*), Oct. 2016.

[3] C. Liu, and A. E. Yılmaz, "A reduced-domain layered-medium integral-equation method for electronic packages," in *Proc. IEEE 28th Conf. Elect. Perform. of Electron. Packag. Syst. (EPEPS*), Oct. 2019.

[4] C. Liu, K. Aygün, and A. E. Yılmaz, "A parallel FFT-accelerated layered-medium integral-equation solver for electronic packages" *Int. J. Num. Model.: Electron. Networks, Dev., Fields,* vol. 33, no. 2, Mar. 2020.

[5] S. Bai *et al.*, "The accuracy of port connections between layers in printed circuit board," in *Proc. IEEE 26th Conf. Elect. Perform. of Electron. Packag. Syst. (EPEPS*), Oct. 2017.

[6] M. R. Abdul-Gaffoor *et al.*, "Simple and efficient full-wave modeling of electromagnetic coupling in realistic RF multilayer PCB layouts," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 6, pp. 1445–1457, 2002.

[7] C-J. Ong *et al.*, "Full-wave solver for microstrip trace and through-hole via in layered media," *IEEE Trans. Adv. Packag.,* vol. 31, no. 2, pp. 292–302, May. 2008.

[8] D. Pissoort *et al.*, "A rank-revealing preconditioner for the fast integral-equation based characterization of EM crystal device," *Microw. Opt. Technol. Lett.,* vol. 48, no. 4, pp. 783–789, Apr. 2006.

[9] S. M. Rao, D. R. Wilton, and A. W. Glisson, "Electromagnetic scattering by surfaces of arbitrary shapes," *IEEE Trans. Antennas Propag.*, vol. 30, no. 3, pp. 409–418, May 1982.

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