Post-FEC BER Performance Analysis for Multi-stage PAM4 Systems

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***Abstract*— In a multi-stage link system where forward error correction (FEC) encoding/decoding is only used in the end devices of the end-to-end link, mixed mode errors (random and burst errors) from each sub-link stage collectively impact the end-to-end link performance. This paper introduces an analytical method for evaluating RS-FEC performance in multi-stage PAM4 systems. Typical application scenarios include links with retimer(s), and electrical-optical-electrical (E-O-E) links such as 200GAUI-n/400GAUI-n systems. Simulations are performed to study the impact of sub-link stages on the overall system post-FEC BER performance.**

Keywords*— *RS-FEC, multi-stage link, burst error, BER, SER, end-to-end performance

I. INTRODUCTION

Forward error correction (FEC) has been widely used in high speed 4-level PAM signaling (PAM4) system links. Both the 56G and 112G PAM4 standards adopt Reed-Solomon codes for error correction in long reach (LR), middle reach (MR) and very short reach (VSR) applications [1]. Unlike in single-stage links where FEC error correction is performed within single-stage closed systems, a multi-stage link system usually consists of multiple active components along the signal path, FEC encoding/decoding is only performed by the devices on both ends of the end-to-end link, the middle active components do not terminate errors in each sub-link stage for power and latency reasons.

For end-to-end FEC performance evaluation for such multi-stage systems, two aspects need to be considered: (1) the active components such as SerDes, the system level impairments such as insertion loss (related to inter symbol interference) or crosstalk (related to noise), are usually quite different in each sub-link stage, this leads to different error distribution signatures seen by the final stage FEC and largely determines error correction performances; (2) Coding techniques such as Reed-Solomon (RS) symbol distribution, FEC codewords interleaving and PMA bit-level multiplexing as defined in 200Gb/s and 400Gb/s Ethernet [1], play an important role in such multi-stage link systems and have great impact on the post-FEC BER performances.

Combining the two aspects, part II starts with the basic process of a FEC performance simulation methodology that takes into consideration of all possible error patterns from DFE burst effect, followed by the introduction of an analytical model for typical multi-stage FEC applications. FEC codewords interleaving, RS symbol distribution and bit-level multiplexing which are typically applied in multi-lane, multi-stage Ethernet systems are modeled. The algorithmic model is also scalable to handle the cases where correlated errors triggered in very short time periods are averaged out in a longer time window and yields an averaged raw BER, thus the commonly seen FEC simulations could be on the optimistic side.

II. SIMULATION MODEL FOR MULTI-STAGE FEC LINK

A. Analytical FEC performance simulation method

High speed links are typically mixed error systems: randomly occurred errors triggered by impairments such as inter symbol interference (ISI), random noise, jitter, etc., and burst errors that have dependencies on the previously occurred errors, both exist. In the scenarios where decision feedback equalizer (DFE) is used, once a wrong decision has occurred at the slicer, the error affects the voltage level of the next NRZ bit/PAM4 symbol with certain probability through the feedback loop and resulting in error propagation. For NRZ the maximum error propagation probability is 0.5 and for PAM4, it is 0.75.

For one-tap DFE architecture, there are only two error patterns in the DFE register. Probabilities of single burst error with different lengths can be calculated using error propagation probability *Pb*, through equation (1), where *Pr* represents the raw BER, and *i* is burst length:

$$P_{burst\ error}(i) = Pr \cdot Pb^{i-1} \cdot (1 - Pb) \quad (1)$$

In general, for an *M*–tap DFE (*M*≥1), single burst error propagation probabilities of the 2^*M* error patterns can be calculated using detection SNR or vertical bathtub curves.

For RS FEC, as error correction is performed in units of RS symbols, burst errors of different lengths shall translate into the corresponding numbers of RS symbol errors, and the corresponding symbol error ratio (SER) is calculated. Post-FEC Frame Error Ratio (FER) and BER are then calculated according to the maximum correctable number of RS symbols of the RS code. Let *i* be the number of RS symbol errors in a FEC frame. For RS (*n*,*k*,*t*):

$$FER = \sum_{i=t+1}^{n} SER(i) \quad (2)$$

B. Analytical model for multi-stage and multi-lane systems

A multi-stage FEC system usually consists of multiple cascaded sub-link stages and for one or more of the sub-link stages, there could be multiple lanes in parallel carrying RS symbols. FEC encoding/decoding is only performed at both ends of the system. Figure 1 (a) illustrates a 3-stage, 4-lane system, where the middle stage active components can be retimer(s) or optical modules in practical scenarios; figure 1 (b) shows how the RS symbols are distributed across multiple PMA lanes in 100Gb/s Ethernet application. The number of PMA lanes is 2, 4, 8 and 16 for 50GbE, 100GbE, 200 and 400GbE applications respectively.

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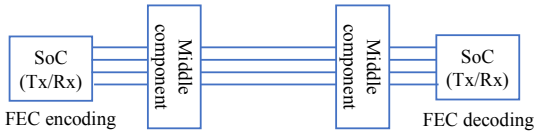
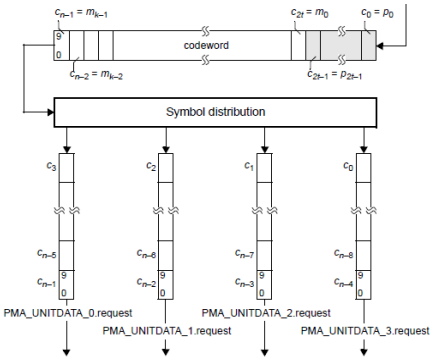


(a). Illustrative topology of a 3-stage, 4-lane FEC system



(b). RS symbol distribution across 4-lane in 100GBASE-R [1]

Fig.1. Multi-stage, multi-lane system illustration

For a cascaded stage system, RS symbol errors in a received RS(*n*,*k*,*t*) codeword are introduced independently by each stage. When *j* RS symbol errors occur in the first stage, there are *n*-*j* possible locations for the next stage to introduce RS symbol errors. Therefore, SER of a 2-stage link can be calculated through convolution of the probabilities of different numbers of RS symbol errors in each stage, as in (3). The same method can be extended to 3 or more stages.

$$SER(i) = \sum_{j=0}^{i} SER_{stg1}(j) \cdot \frac{C_{n-j}^{i-j}}{C_n^{i-j}} SER_{stg2}(i-j) \qquad (3)$$

For a multi-lane system where RS symbols are distributed across lanes, there is no overlap of RS symbol errors between lanes in a received RS codeword. The same convolution approach applies. Take 4-lane system for example, SER with *i* RS symbol errors in a complete RS(*n*,*k*,*t*) codeword is the convolution of SER probabilities of each single lane:

$$SER_{0-1}(i) = \sum_{j=0}^{i} SER0(j) \cdot SER1(i-j) \qquad (4)$$

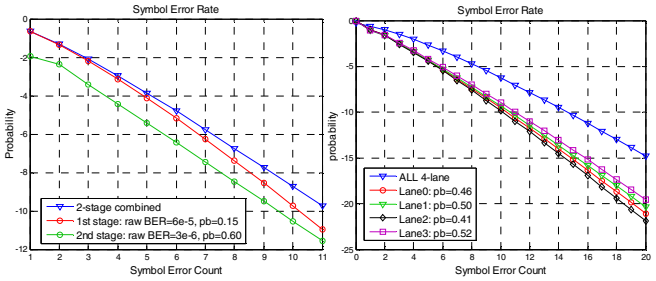
$$SER_{2-3}(i) = \sum_{j=0}^{i} SER2(j) \cdot SER3(i-j) \qquad (5)$$

$$SER(i) = \sum_{j=0}^{i} SER_{0-1}(j) \cdot SER_{2-3}(i-j) \qquad (6)$$

In (4) to (6), subscripts 0-1, 2-3 represent lane 0 and 1, lane 2 and 3, respectively. The same idea applies to 2, 8 and 16-lane applications. The "aggregated" SER is obtained through SER probability convolution of 2, 8 and 16 lanes.

Note that in some insertion loss dominated links, concentrated ISI patterns in PRBS sequences are more likely to produce concentrated pattern correlated errors. The initial randomly occurred errors (as opposed to burst errors) in such links are no longer evenly distributed. FEC model discussed in this section as in (3) applies for such cases [6], with the exception that that C_{n-j}^{i-j}/C_n^{i-j} is set to 1. SER_{stg1} deals with evenly distributed initial error input, while SER_{stg2} handles the ISI pattern input.

Figure 2 (a) shows the SER simulation result of a cascaded 2-stage, single-lane system, and figure 2 (b) shows the SER simulation result of a single-stage, 4-lane system. In both simulations, DFE error propagation strength of each single lane is denoted by *pb*. From the analysis, SER of the received RS codeword of a cascaded multi-stage system, or a multi-lane system, has a noticeable degradation compared with any single stage or single lane, and the degradation increases as the number of RS symbol errors increases. This draws attention to post-FEC BER analysis in such multi-stage and multi-lane systems, as the KP4 FEC, i.e., RS(544,514,15) in the 56G and 112G era, is affected by SER with RS symbol error number increasing to more than 15.



(a). 2-stage, 1-lane system (b). 1-stage, 4-lane system

Fig.2. SER Simulation for multi-stage and multi-lane systems

C. *Analytical model for FEC codewords interleaving effect*

FEC codewords interleaving/de-interleaving helps break long burst errors occurred in physical channels and scatter the long bursts induced consecutive RS symbol errors across 2 or more received FEC codewords. For 2:1 FEC codewords interleaving (as defined in 400GBASE-R), pairs of FEC codewords are interleaved/de-interleaved on a 10-bit basis.

With 2:1 interleaving, the probabilities of *i* consecutive RS symbol errors in a FEC codeword are calculated:

$$P\ with\ interleaving(i) = 0.5 \cdot P(2 \cdot i - 1) + P(2 \cdot i) + 0.5 \cdot P(2 \cdot i + 1) \qquad (7)$$

Where, *P* on the right side of the equation represents the RS symbol error probabilities without interleaving effect.

D. *Analytical model for PMA bit-level multiplexing effect*

In 50GbE, 100GbE, 200GbE and 400GbE PMA, 2:1 bit-level multiplexing is defined for PAM4 applications. De-multiplexing in the receiving direction converts the PAM4 symbols to pairs of bits in two PMA lanes (MSB and LSB). Thus, one Gray-coded PAM4 symbol error maps into one bit error either in LSB (2/3 chance) or in MSB (1/3 chance). For general analysis, define the burst error length as (*i*-1)·5+*j*, where *i* is an odd integer (*i* =1, 3, 5…), *j* ranges from 1 to 10.

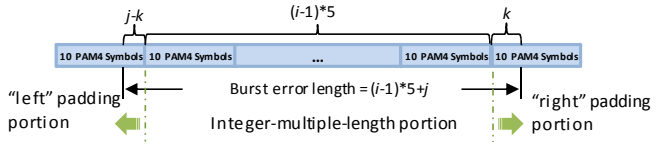


Fig.3. Single burst length definition for 2:1 bit-mux analysis

For the burst error defined in Figure 3, RS symbol error probabilities from the "left" padding portion plus the integer-multiple portion of the burst error are calculated as follows:

$$\forall k \in [0,9],\ M = \begin{cases} 0, & k \geq 1 \\ 1, & k = 0 \end{cases}$$

$$P_{consecutive\ \ symbol\ errors\ left}(k,\ 1) = \sum_{j=k+1}^{10} (11-j)^M \cdot P_{burst}\left((i-1)\cdot 5+j\right)\cdot\left(\left(\frac{1}{3}\right)^{j-k}+\left(\frac{2}{3}\right)^{j-k}\right) \quad (8)$$

$$P_{consecutive\ \ symbol\ errors\ left}(k,\ 2) = \sum_{j=k+1}^{10} (11-j)^M \cdot P_{burst}\left((i-1)\cdot 5+j\right)\cdot\left(1-\left(\frac{1}{3}\right)^{j-k}-\left(\frac{2}{3}\right)^{j-k}\right) \quad (9)$$

RS symbol error probabilities of the "right" part padding:

$$\text{For } k=0: \quad P_{consecutive\ symbol\ errors\ right}(k,0:2) = [1\ 0\ 0]$$

$$\text{For } k\geq 1: \quad P_{consecutive\ symbol\ errors\ right}(k,0) = 0$$

$$P_{consecutive\ symbol\ errors\ right}(k,1) = \left(\frac{1}{3}\right)^k+\left(\frac{2}{3}\right)^k$$

$$P_{consecutive\ symbol\ errors\ right}(k,2) = 1-\left(\frac{1}{3}\right)^k-\left(\frac{2}{3}\right)^k \quad (10)$$

The RS symbol error probabilities of the burst error of length $(i-1)\cdot 5+j$ can then be calculated through convolution:

$$P_{consecutive\ symbol\ erros}(i:i+3) = \sum_{k=0}^{9}\left(P_{consecutive\ symbol\ errors\ left}(k,1:2) * P_{consecutive\ symbol\ errors\ right}(k,0:2)\right) \quad (11)$$

With bit-level multiplexing, post-FEC BER performance degrades, which can also be found in discussions in [2, 3, 4].

III. PERFORMANCE STUDY FOR MULTI-STAGE FEC LINK

A. *Two-stage FEC link with retimer(s)*

A two-stage, single-lane backplane link with a retimer is investigated. RS (544,514,15) error correction is applied at the end stage of the link. The transceivers are based on an IBIS-AMI model for a 56Gbps PAM4 ADC-based receiver architecture. Receiver equalization consists of CTLE/AGC, 24-tap FFE, and 1-tap DFE. The end-to-end link insertion loss keeps the same (about 40dB bump to bump); the lengths (and loss) of the sub-links are different, depending on the location adjustment of the retimer under practical engineering constrains. 0.36mVrms crosstalk noise is applied in AMI simulations for sub-link 2.

Table 1 summarizes the simulated raw BER for each sub-link stage and the post-FEC BER of the end-to-end link:

TABLE I. FEC SIMULATION SUMMARY OF A 2-STAGE LINK

Insertion Loss (dB)			Raw BER		End-to-end
Sublink1	*Sublink2*	*End-to-end*	*Sublink1*	*Sublink2*	Post-FEC BER
24.7	15.4	40.1	4.38E-05	1.01E-05	5.57E-27
25.5	14.7	40.2	2.50E-05	7.12E-06	2.60E-28
26.4	19.9	40.3	2.20E-04	9.48E-06	5.43E-16
28.0	12.1	40.1	1.01E-04	9.78E-07	5.20E-17
30.0	10.1	40.2	2.42E-04	6.29E-06	1.33E-15
31.5	8.7	40.2	3.79E-04	7.02E-06	2.11E-17
33	8.0	41	7.14E-04	5.11E-05	2.14E-15

From the results, post-FEC BER varies about 10 orders while adjusting the location of the retimer in the end-to-end link; the raw BER of the two sub-links hardly changes by 1 order. Case-by-case post-FEC BER analysis helps to evaluate such multi-stage link systems for margin budgeting.

B. *Three-stage FEC link of E-O-E System*

A three-stage E-O-E system is investigated. In this simulation, optical link SER from a reported 400GBASE-LR8 field data for 27km SMF [5] is used as an example, the measured raw BER is 8.71e-5. One-tap DFE receiver model is used for 400GAUI-8 host chips on both ends of the three-stage link. 2:1 FEC codewords interleaving and 2:1 PMA bit-level multiplexing are enabled.

The DFE error propagation probability factor *Pb* for the 8 individual lanes in VSR sub-link stages 1 and 3 is swept. From the simulation results in Figure 4, reducing DFE error propagation strength, which means to reduce the DFE tap weight, helps to enhance post-FEC BER performance of the end-to-end link; however, the gain is reducing as *Pb* reduces incrementally from 0.5 to 0.2 for this system.

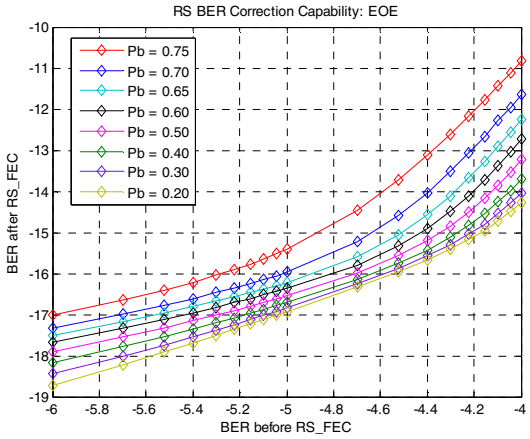


Fig.4.End-to-end FEC performance simulation for E-O-E link

IV. CONCLUSIONS

A simulation method for analyzing end-to-end RS FEC performance for multi-stage link systems is discussed. Examples with a retimer link system and a 400GAUI-8 E-O-E system show that post-FEC BER performance for multi-stage systems largely depends on link configuration, SerDes equalization architecture as well as system link impairments. Accurate post-FEC performance evaluation for such multi-stage systems relies on case-by-case analysis.

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