Signal Integrity Characterization of Channels With Asymmetric Via Stubs

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Abstract—**The characterization of the signal integrity (SI) performance of differential high-speed channels that have an imbalance due to mismatched via stub length is investigated. The impact of the asymmetric stubs are characterized with regards to impedance matching, differential-to-common mode conversion and intra-pair skew computation. Simulations for the short and long differential vias are carried out in both the frequency-domain and the time-domain with a back-drilling tolerance of ±10 mils for the residual stubs. It is shown that there is a 9 Ω differential impedance variation, over -40 dB mode conversion loss above 5GHz and 2~3 ps of intra-pair skew is introduced. An example is illustrated to show the impact of the stub asymmetry for the high-speed channel with a time-domain eye simulation at 40 Gbps data rate. It is shown that the short imbalanced differential via with a 20 mil stub asymmetry has the eye diagram degradation in the peak-peak jitter that doubles the jitter for the channel with vias with equal-length residual stubs.**

I. Introduction

As high-speed serial link channel data rates increase, any asymmetry or imbalance in the differential signal routing significantly degrades the signal integrity of multi-gigabit interconnects [1-3]. A plated through hole (PTH) in the printed circuit board (PCB) is referred to as a via for this study. This PTH via has a current carrying part from the surface connection to an internal wiring layer that is called the active via length. The portion of the via after the internal wiring layer is removed, typically by a back-drilling process that leaves a residual via stub [4]. The via stub lengths are greater than zero due to tolerances in PCB fabrication. For the class of PCBs considered for this study, we assume that a via stub tolerance of +/- 10 mils around a so-called do-not-cut line is achieved. This 20mil stub length variation causes a mismatch of the via stub loading on the differential signaling which impacts the impedance matching and induces an intra-pair skew. Skew mitigation is very important for maintaining the signal integrity. Even picosecond skews can impact the performance of the channel and induce undesirable differential-to-common (DTC) mode noise and cause electromagnetic radiation (EMI). This study characterizes the impedance variation and the skews introduced by the asymmetric via stub. For this study, we are assuming a data rate of 25 Gbps or more.

The paper is organized as follows. Section II presents the 3D full-wave differential via modeling with asymmetrical stubs in both short and long active via lengths, respectively. Through simulation, the differential via impedance, the differential insertion loss and the DTC mode conversion are determined. The intra-pair skew as a function of frequency is computed with a method using the modified mixed-mode S parameter [5]. Section III provides an eye simulation example at a data rate of 40 Gbps comparing the imbalanced via stub response with the balanced via stub. Finally, the conclusion is given in Section IV.

II. Modeling of Imbalanced Differential Via with Asymmetric Stubs

A pair of differential vias with the via stubs is shown in Fig. 1. The active via length, *h,* is from the surface differential microstrip trace to the differential stripline traces on an internal wiring layer. The via stub lengths, b_1 and b_2, extend below the internal wiring layer. In order to compare the SI impact of the stub asymmetry, two active via lengths are chosen as shown in Fig.1(a) with h=52mils (~1.32mm) and Fig. 1(b) with h=102.7mils (~2.61mm). The stub asymmetry is studied as the stub length b_2 varies with the center at b_1=15mils with a variation of +/- 10 mils. A stubless via model is simulated as the reference for comparison. The S-parameter models are extracted using a 3D full-wave solver.

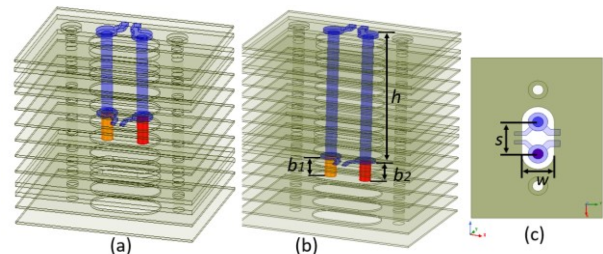

Fig. 1. Modeling with a pair of differential via with via stubs: (a) and (b) front views for short and long vias; (c) top view.

Both the microstrip and stripline traces are designed to have an 85 Ω differential impedance. The via pad is 18 mils, the drill dimeter is 10 mils, the via spacing, *S*, is 31.5 mils, the oblong antipad width, *W*, is 30 mil, and the antipad length, (*W*+*S*), is 61.5mil. The board cross-section is of a hybrid construction [4] having an effective relative dielectric constant of ε_r=3.26 and a loss tangent tanδ=0.003 at 10GHz for the low-loss internal wiring layers with the breakout wiring, and a relative dielectric constant of ε_r=4.15 and a loss tangent tanδ=0.021 at 10GHz for the layers without internal high-speed signal traces.

Figs. 2a and 2b shows the simulated differential time-domain reflectometry (TDR) results for the short h=52 mils and long h=102.7 mils differential vias, respectively. A 0-100% rise time of 20 ps is launched at the breakout stripline on the internal

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wiring layer. One via stub is fixed at the length b_1=15 mils, and the other via stub b_2 varies the length from 5 mils to 25 mils in light of the back-drilling tolerance of ±10 mils. Both the short and long differential vias show the capacitive impedance with the aforementioned board stackup, and the via impedance dip increases as via stub b_2 gets shorter by approximately 2.5 Ω per 5 mils change in b_2. For the stubless case, the short and long differential vias are around 80 Ω. As b_2 changes from 5mils to 25mils, the impedance of the short differential via varies by 9.1 Ω decreasing from 73.8 Ω to 64.7 Ω . For the long differential via, the impedance decreases from 71.0 Ω to 62.4 Ω, an 8.6 Ω change. Therefore, the back-drilling tolerance of ±10 mils results in a differential impedance uncertainty of approximately 9 Ω for the vias in this PCB.

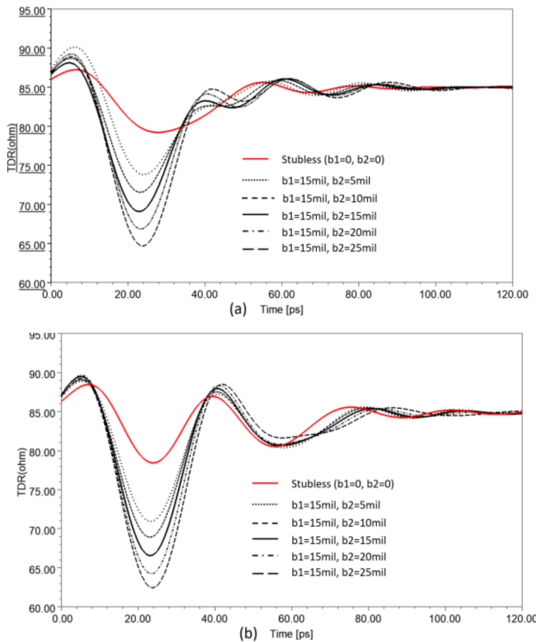


Fig. 2. Simulated differential TDR impedance of the differential via from the breakout stripline to the top microstrip with rise time of 20 ps and source reference impedance at 85 Ω: (a) active via length h=52mils and (b) active via length h=102.7mils.

The simulated differential-to-common mode conversion as denoted by Scd21 with varied stub lengths for both the short and long differential vias are shown in Fig. 3. It is clearly seen that the asymmetry of the via stubs causes the DTC loss to increase with the frequency. Scd21 rises over -40dB above 5 GHz. However, the equal-stub case (b_1=15mils, b_2=15mils) shows that Scd21 is less than -50 dB over the 35 GHz frequency range and nearly follows the ideal stubless case. The induced mode conversion increases with more asymmetry as shown in Table 1. In addition, there is nearly a 10dB variation in mode conversion over the back-drilling tolerance of ±10mils. Note that the Scd21 curves are very similar for the short and long active vias showing that it is the stub asymmetry that increases the mode conversion. Meanwhile, the Scd21 curves start to drop near 30GHz as is caused by the poor impedance matching and the worse return loss.

Also note that the differential insertion loss Sdd21 mirrors the aforementioned impedance variation by the via stubs in TDR plots. The differential via with the longest stub b_2=25 mils has the biggest insertion loss. For instance, Sdd21 of the imbalanced short differential via drops 0.5 dB at 20 GHz and 1.4dB at 30GHz as compared with the stubless via model; while for the long differential via, it drops 0.8 dB at 20 GHz and 2.2 dB at 30 GHz.

$b2$ (mils)	5	10	15	20	25
$\Delta(=b2-b1)$ (mils)	-10	-5	0	5	10
Scd21(dB)	-23.5	-28.8	-70.8	-27.2	-19.9

Table 1. Simulated differential-to-common mode conversion Scd21 at 16GHz for the active via length h=52mils with one stub length $b1$ at 15mils.

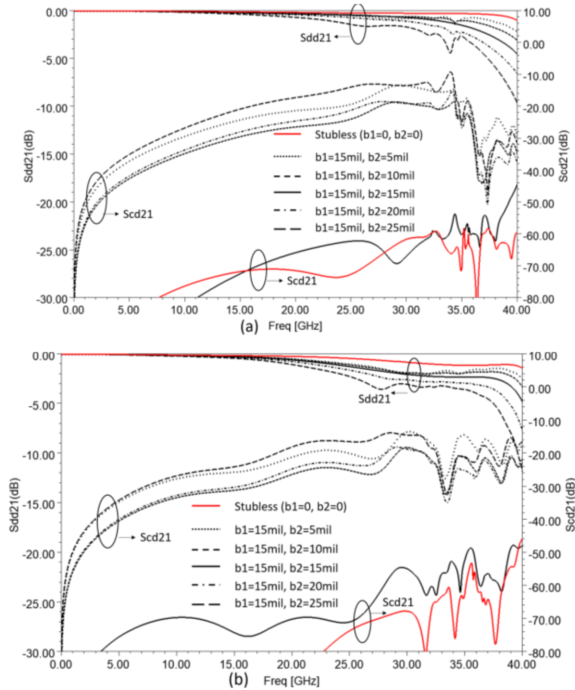


Fig. 3. Simulated differential insertion loss Sdd21and differential-to-common mode conversion Scd21 at the reference impedance 85 Ω: (a) active via length h=52mils and (b) active via length h=102.7mils.

The modified mixed-mode S parameter as proposed by the computational method in [5], takes differential-mode and common-mode into account simultaneously. Based on this method, the intra-pair skew is calculated as the function of the frequency with different stub lengths for the short and long differential vias. Fig.4 shows the calculated results of unwrapped phases and the resulting time delays for the P-side via with the stub b_1=5 mils and N-side via with the stub b_2=25 mils of the long differential via (h=102.7 mils).

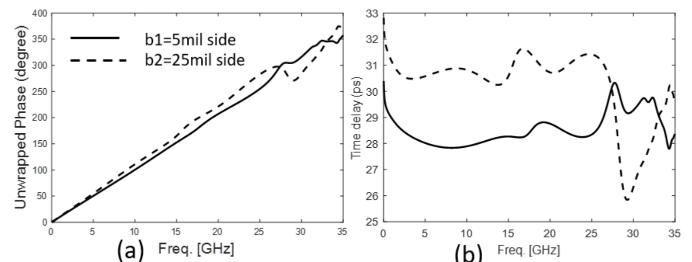


Fig. 4. Calculated unwrapped phase (a) and time delay (b) for the long differential via (h=102.7mils) with the asymmetric stubs (b_1=5mils, b_2=25mils).

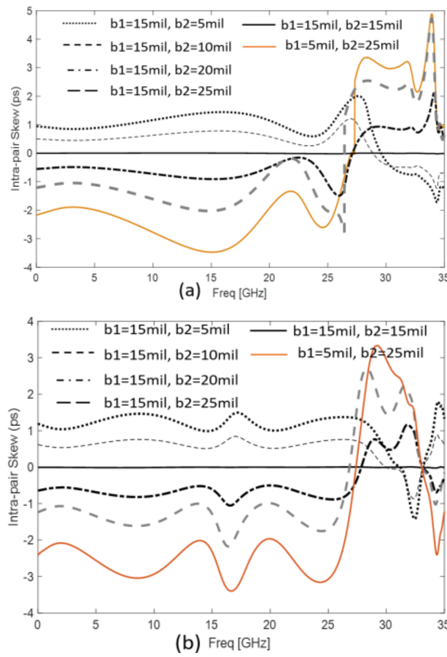
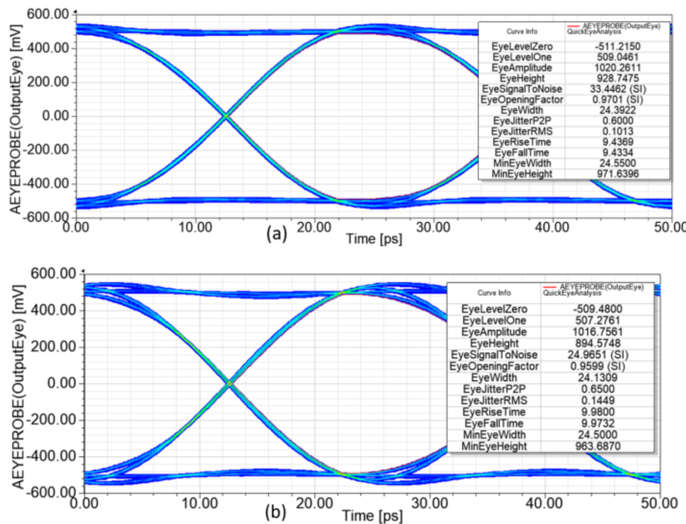


Fig. 5. Calculated intra-pair skew: (a) active via length h=52mils and (b) active via length h=102.7mils.

The intra-pair skew is defined by the difference between the time delays of P-side and N-side vias, as is derived in the following Fig. 5. As expected, the equal-stub case (b_1=15 mils, b_2=15 mils) has zero skew in the entire frequency band. At the lower frequencies less than 10 GHz, the skew changes very slowly with the frequency, and there is around a 0.5 ps step size for the skew as the stub asymmetry changes in 5 mils length steps. The case (b_1=5 mils, b_2=25 mils) has the biggest stub difference and shows the biggest skew as a result. For the short and long differential vias, the intra-pair skews are very close at a certain stub asymmetry, which agrees well with the Scd21 plots for the mode conversion.

III. TIME-DOMAIN EYE SIMULATION



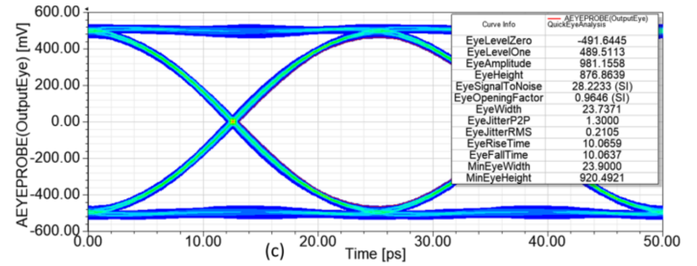


Fig. 6. Eye diagrams for the short (h=52 mils) differential via at 40 Gbps: (a) stubless (b_1=0 mil, b_2=0 mil), (b) equal stubs (b_1=15 mils, b_2=15 mils) and (c) unequal stubs (b_1=5 mils, b_2=25 mils).

The short (h=52 mils) differential via is simulated in the time domain at 40 Gbps date rate. The 85 Ω Tx setting uses the peak voltage of 1 V, the bit pattern of PRBS23 and the rise time of 15 ps. No equalization is used in Tx and the eye probe in Rx. The eye width and the jitter match closely in both the ideal stubless case in Fig.6(a) and the equal 15 mils stub case in Fig. 6(b). Fig. 6(c) has the multiple traces in the eye which indicates the degraded impedance matching. In comparison with the equal stub case in Fig. 6(b), the 20 mils stub asymmetry (b_1=5 mils, b_2=25 mils) in Fig. 6(c) results in the peak-to-peak jitter doubling from 0.65 ps to 1.30 ps, and the RMS jitter increasing by a factor of 1.45 from 0.145 ps to 0.21 ps.

IV. CONCLUSION

The degradation of signal integrity properties introduced by stub asymmetry in the back-drilling process of differential vias is investigated and simulated with regards to differential impedance, the insertion loss, the differential-to-common conversion, and the intra-pair skew. The SI characterization for the imbalanced differential via with asymmetric stubs provides useful insights into the differential via designs for high-speed channel applications. At 25 Gb/s and above, the impact is significant, and steps must be taken to avoid or minimize the stub length differences between PTH vias in a differential pair by proper PCB design and fabrication process control. If sufficient control is not available, the impact of the via stub asymmetry on the signal integrity of the high-speed signal needs to be factored into the channel specifications.

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