Via Design Optimization for High Speed Differential Interconnects on Circuit Boards

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***Abstract*— The unprecedented demand for high bandwidth applications boosts the data rates of major high speed differential interconnect protocols such as PCIe and Thunderbolt/USB. Transmission lines and via transitions form most of the interconnect path between a transmitter and a receiver. To get maximum performance of the system at high signaling rates, the impedance of the interconnect path has to be as uniform as possible to cause minimal signal reflections. While the impedance of transmission lines can be easily controlled, the impedance of vias are much harder to control. In this paper, we use time-domain impedance waveforms in conjunction with channel simulations to optimize the impedance profiles of 3 types of differential vias: through-hole vias, blind vias and buried vias. We do this by varying the via diameter, pad diameter, antipad diameter and via pitch (center-to-center distance). We then show a quick method to optimize the vias for faster turnaround time, depending on whether the via impedance is too capacitive or too inductive. The board designer can use the quick method to try to achieve approximately the impedance profiles we show.**

Keywords— bandwidth, high-speed electronics, impedance matching, printed circuit boards

I. Introduction

One of the key challenges of signal integrity engineers is the understanding of how to maximize the electrical performance of high speed differential I/O, which can run at data rates of tens of gigabits per second. It is critical to identify significant factors which can be optimized to stretch the electrical performance of electronic systems in an increasingly competitive business environment.

On circuit boards and packages, vias are impedance discontinuities that are unavoidable as routing needs to change layers. Up to data rates of several gigabits per second, these vias are electrically short, so they do not interfere too much with signal integrity performance. Board designers focus mainly on the maximum length allowable for via stubs to prevent resonance effects. When the data rate goes into tens of gigabits per second as in PCIe Gen. 5, USB 3.2 Gen. 2 and Thunderbolt, the vias could contribute to significant degradations to the signal quality.

The investigation into single ended via modeling and via impedance control has been undertaken by Andreas Hardock et al. [1]. In this paper, the focus will be on differential vias as high speed input-output (HSIO) signaling at high data rates takes place on differential interconnects. In particular, we will focus on PCIe Gen. 5. The methodology is general and applies to high speed differential vias for any signaling protocol.

A lot of researchers have worked on optimizing via electrical performance. Some have tried to optimize ground via placement and patterns [2] [3]. Others have tried to redesign the via structure [4]. In this paper, we will optimize via parameters such as via diameter, pad diameter, anti-pad diameter and via pitch to get optimum signal-to-noise ratio (SNR). (The anti-pads for the differential vias are assumed to be merged.) This involves generating differential via models and performing channel simulations. The optimum impedance profile for 3 types of vias will be shown: the plated through hole (PTH) via, the blind via and the buried via. The blind and buried vias are all assumed to be backdrilled and hence have no stubs. These 3 via types are shown in Fig. 1. We will also show a quick method of optimizing vias, depending on whether the impedance profile is too capacitive or too inductive. The board designer can use the optimized impedance profile as a guide to optimize the via impedance.

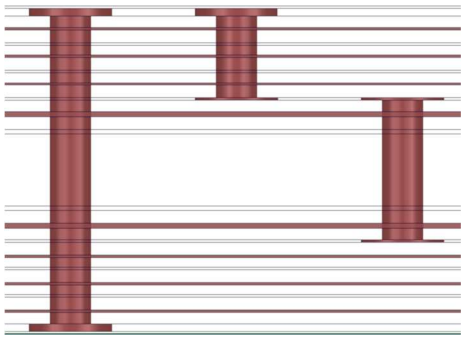

Fig. 1 Three types of vias. From left: through-hole via, blind via and buried via. The stackup is drawn to scale.

II. Methodology for Full Factorial Via Parameter Optimization

The S-parameters and time domain impedance profiles of the PTH vias, blind vias and buried vias were generated. For each via type, the following via parameters were swept: via diameter, pad diameter, antipad diameter and via pitch. Table I shows the via parameter values swept. The minimum values of these parameters were chosen such that the boards can be mass manufactured at reasonable cost.

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TABLE I. RANGE OF VIA PARAMETERS

Via parameter	Min. Value (mils)	Max. Value (mils)
via diameter	8	12
pad diameter	18	22
antipad diameter	28	32
via pitch	28	36

Each via of the differential pair had a ground via placed 40 mils away (center-to-center). Each ground via had a 10 mil via diameter. The board in total had 18 layers. The through hole via went from the top layer to the bottom layer. The blind via went from the top layer to layer 7. The buried via went from layer 7 to layer 12. See Fig. 1. The ground plane and substrate dimensions for the via model was 150 mils by 150 mils. The total feed length was about 150 mils. Fig. 2 shows the modeled structure for the blind via. The buried and through-hole via were modeled similarly.

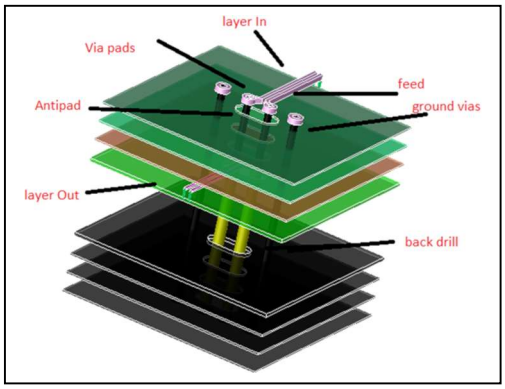

Fig. 2 Via structure for blind via.

Each model for a single set of parameters took about 15 to 20 min. to generate for a frequency range from 1 MHz to 32 GHz. About 240 models were generated for each via type. The machine used to generate the models (and perform the channel simulations) was a 64 bit Windows server with 384 GB of RAM and dual Intel Xeon Gold 6142 CPU's clocked at 2.6 GHz.

The via models were incorporated into channel simulations to generate the eye patterns at the receiver end of a PCIe Gen 5 channel, which had a 32 GT/s data rate. The channel included 2.5 inch long differential transmission lines both before and after the via models. The channel simulation for the blind vias had 2 sets of vias to so that transmitter and receiver were both on the top layer. The channel simulation for the buried vias had 2 sets of buried vias as well as blind vias so that the transmitter and receiver was on the top layer. The channel simulation for the PTH via had only 1 via from top to bottom layer. The transmitter had feed forward equalization (FFE) enabled in the IBIS AMI model. The receiver had decision feedback equalization (DFE) enabled in the IBIS AMI model. No continuous time linear (CTLE) equalization was used. The optimized via parameters were not expected to be heavily influenced by the equalization, as having a better channel should result in better receiver eye parameters irrespective of the equalization scheme.

III. RESULTS

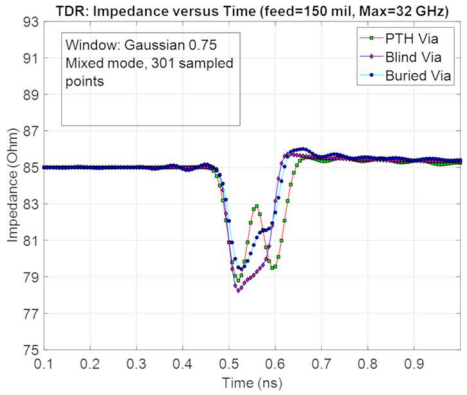

Fig. 3 Impedance profiles of vias with largest SNR for the 3 via types.

Fig. 3 shows the impedance profiles of the vias with the largest SNR for each of the 3 via types. (The differential impedance of the transmission lines was 85 Ω.) These are impedance profiles of the vias with the via parameters optimized such that the channel simulations would give the largest SNR. In general, the via gives optimal SNR when there are minimal impedance changes. This is because reflections will be minimized. Multiple reflections will cause distortions to received waveform. Thus, if the via is capacitive, an inductance 'spike' in the middle of the via is undesirable. We see that for the PTH via, the inductance 'spike' in the center is unavoidable as the via goes through the core where there are no closely spaced ground planes. The buried via goes through the core too but has no inductance spike as the pad capacitance and via pitch can compensate for the inductance due to the via barrel. It also helps that the buried via is less capacitive than the through-hole via. The blind via does not go through the core and is strictly capacitive for maximum SNR.

Table II shows the via parameters corresponding to the impedance profiles shown in Fig. 3.

TABLE II. VIA PARAMETER VALUES FOR VIAS WITH OPTIMIZED SNR

Via Type	Via Diameter (mils)	Pad Diameter (mils)	Antipad Diameter (mils)	Via Pitch (mils)	SNR (dB)
PTH	11	22	28	34	9.05
Blind Via	8	20	32	28	8.50
Buried Via	8	22	30	28	8.98

To illustrate how the optimized via impedance profile differs from a via impedance profile that is not optimized, we show the case of the buried via that was not optimized in Fig. 4, along with the case of the optimized via.

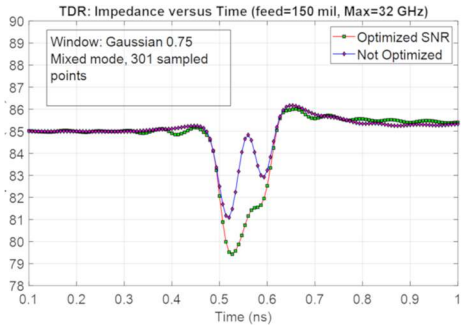

Fig. 4 Impedance profile of buried via that is optimized for SNR and one that has not been optimized. For the latter case, the via diameter is 11 mils, pad diameter is 18 mils, antipad diameter is 28 mils and via pitch is 33 mils. The SNR of the receiver signal was 8.48 dB.

Comparing the buried via impedance profile in Fig. 3 and Fig. 4, it can be seen that maximizing pad diameter and minimizing the via pitch helps to shape the impedance profile to minimize the impedance change for the via optimized for maximum SNR. Fig. 5 shows the receiver eye of the channel with the optimized buried via.

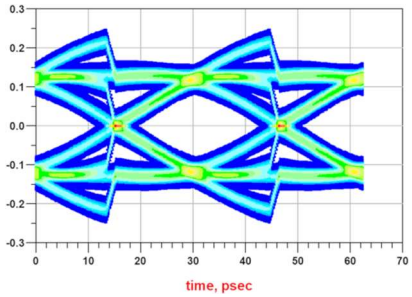

Fig. 5 Receiver eye for channel with optimized buried via. The y-axis has units of volts. The impedance profile of the via is shown in Fig. 3 and the via parameters are shown in table II.

IV. Quick Methodology for Via Parameter Optimization

The results in Fig. 3 were generated using a full factorial parameter sweep and this may take days to accomplish. If such a time period is too prohibitive, an arbitrary via design can be simulated and a sub optimization method can be achieved using tables III and IV.

TABLE III. Quick Via Optimization if Via is too Capacitive

Action	Rel. Mag. of Impact	Constraints
Decrease via diameter	Highest	Via diameter ≥ 6 mils
Decrease pad diameter	High	Pad diameter – hole diameter ≥ 6 mils
Increase antipad diameter	High	Antipad diameter – via diameter ≥ 16 mils
Increase via pitch	Medium	Via pitch – via diameter ≥ 15 mils

Other methods to lower the capacitance include lowering the dielectric constant of the substrate, increasing dielectric thicknesses and removing non-functional pads.

TABLE IV. Quick Via Optimization if Via is too Inductive

Action	Rel. Mag. of Impact	Constraints
Increase via diameter	Highest	Via diameter ≥ 6 mils
Increase pad diameter	High	Pad diameter – hole diameter ≥ 6 mils
Decrease antipad diameter	High	Antipad diameter – via diameter ≥ 16 mils
Decrease via pitch	Medium	Via pitch – via diameter ≥ 15 mils

Other methods for lowering inductance are increasing dielectric constant of the substrate, decreasing dielectric thickness, adding non-functional pads and adding ground vias.

A constraint not in tables III and IV is the maximum aspect ratio. For mechanically drilled vias, it is 10:1 for filled vias and 15:1 for unfilled vias. All the constraints may vary depending on the board manufacturer. The process in tables III and IV is repeated until the via impedance profile approximates the corresponding profile in Fig. 3.

V. Conclusion

We have presented a method to optimize differential vias for maximum SNR. We showed a full factorial method with the optimum impedance profiles of 3 types of vias: through hole vias, blind vias and buried vias. We also showed a quick method of optimizing the vias, depending on whether the vias are too capacitive or inductive. The goal for the quick optimization is to achieve an impedance profile that approximates the profiles shown in this paper for the full factorial optimization.

Acknowledgment

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