Determine Socket's Inductance and Contact Resistance by Using PRF Method

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***Abstract*—In this paper, an accurate socket modeling methodology is proposed for signal integrity and power integrity applications using a quasi-static EM solver and considering the contact resistance of the socket which is a non-negligible component in socket modeling. The contact resistance characterization of a specific pogo-pin socket has been conducted by measuring the socket mounted on a specially designed test vehicle. A Parallel Resonance Frequency (PRF) method [1] is used to validate the EM model and to extract the contact resistance accurately.**

***Index Terms*—pogo pin socket, contact resistance, signal integrity, power integrity, quasi-static, PRF methodology.**

I. Introduction

Nowadays, a test socket is often used to electrically link the testing PCB and semiconductor chips and to eliminate the soldering process as shown in Fig.1.

To accurately evaluate the performance of high-speed interfaces and power delivery networks (PDN), high-quality electromagnetic (EM) socket models are needed in system level simulation for both signal integrity (SI) and power integrity (PI) applications to capture crosstalk and Vdroop. Socket were characterized by using a first order equivalent circuit model or building socket model with H type of equivalent circuit. Unfortunately, direct micro probe landing is still used to measure the socket which will introduce unavoidable errors.

The resistance behavior of the socket is a function of the force applied to the socket by the socket clamp. The contact design, material, and mechanical assembly will impact the contact resistance range. In this study, a socket fixture with a force-control clamp is designed and used so the compression is kept constant with a mechanical stop. In applications where the socket can be treated as electrically small, it is adequate to add a series contact resistance component to model all the contact resistances that may exist at several points along the socket pin. Sockets with contact resistance included are characterized using the PRF method that utilizes a parallel LC resonance to characterize the socket's loop resistance and inductance over a broad frequency range. Through further analysis, the socket pin's contact resistance can be extracted. The measurements were done with a specially designed test-vehicle that enables the creation of accurate models by avoiding probe-to-socket pin contact and instead utilizing the PRF methodology.

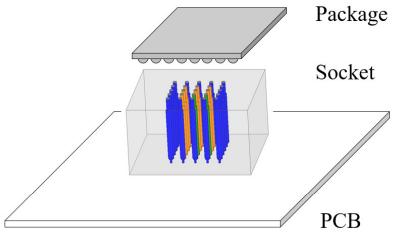

Fig. 1: Diagram of a pogo pin socket with PKG and PCB.

II. Socket Modeling Methodology

A. Socket Modeling Flow

This paper provides insights into extracting EM socket models for SI and PI applications using a quasi-static EM solver by extracting RLGC parameters of socket pins and export an equivalent circuit model that can be used in system level simulations to characterize channel or PDN performance. As shown in Fig. 2, a complete socket modeling flow is established to extract a socket model that includes contact resistance. In this flow, the first step is to create a pin model. After the individual pin model is completed, a socket pin array is created using the pin pattern of interest.

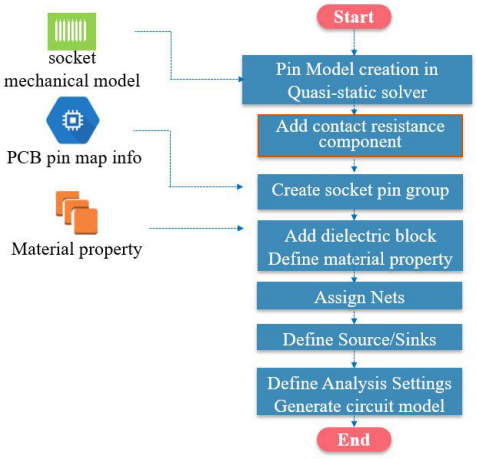

Fig. 2: Socket modeling flow

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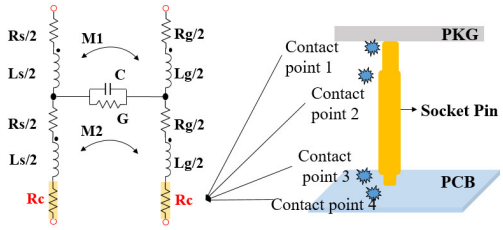

Fig. 3: Schematic diagram of a two pin socket with contact resistance

B. Contact Resistance

In a pogo-pin socket there may be several metal-to-metal contact points along the pin that contribute to the contact resistance as shown in Fig.3. The contact resistance also includes the locations where the socket pin touches the PKG and PCB in addition to the metal to metal contact points along the socket pin. In most cases, a socket pin is electrically small, so it is valid to sum the contact resistances at different points into a total contact resistance element as shown in the equivalent circuit in Fig. 3

Contact resistance of single socket pin ranges from 10 mOhm to 100 mOhm for commonly used sockets, with a representative average of contact resistance of 40 mOhm. In PI applications, such resistances can cause specification compliance failure so the contact resistance should be carefully evaluated. The PRF method captures contact resistance as will be discussed in the following section.

III. Socket Modeling Validation

A. PRF Methodology

In validating the representative socket EM model, good correlation between the simulation and measurements have been achieved using the PRF method. A frequency domain measurement utilizing a vector network analyzer was performed to measure the impedance of a fixtured socket. The PRF technique is applied by designing a fixture that has a well characterized, fixed capacitance which interacts with the socket inductance to form a parallel resonance. The parallel resonance peak offers insight into the DUT and fixture since the Q factor of the peak is a function of the resistance, inductance, and capacitance of the DUT. The parallel resonance peak is an eigenvalue function of the fixture, thus, it is robust and not prone to parasitic inductance error that can be introduced from traditional de-embedding techniques. With the PRF method, the fixture inductance and resistance can be separated from the socket inductance and resistance, effectively de-embedding the fixture.

The DUT impedance in relation to the 2-port S-parameter is defined in (1). Since the two ports at the probing pads in Fig. 5 provide an input wave from one port while the second port senses the received wave, what is really measured is a transfer-impedance between the two ports, which is related to the DUT S-parameters as:

$$Z_{DUT} = \frac{Z_0 S_{21}}{2(1 - S_{21})} \tag{1}$$

where Z_0 is the port reference impedance (50 Ω).

B. Fixture Design

The fixtures designed for mounting the DUT socket are intended for de-embedding utilizing the parallel resonance peak. The fixture provides an accurate and easily measured capacitance source while loop inductance comprises the socket pins and the metal shorting mechanism. The PCB plane capacitance and the mounted socket pin inductance form the parallel resonance. The PCB dielectric material relative permittivity and plane dimensions and probe location are designed to have the capacitance resonate at a frequency where it is distinguishable from the cavity resonances [1].

Key parameters to the fixture are the amount of fixture capacitance and inductance needed to achieve a desired peak resonance at the desired frequency. Once the desired frequency is known, the following equation can help determine the fixture key electrical parameters.

The PRFs from the Fixture Short measurement and Socket Mounted from Fig. 4 can be used to calculate L_{DUT} to yield $L_{fixture}$ and $L_{fixture+socket}$ by subtracting the two extracted inductance values, effectively de-embedding the fixture, so that the inductance of the socket can be derived as L_{Socket}. The socket resistance, R_{DC} can be derived from subtracting the fixture resistance from the fixture and socket resistance.
As a first step, $L_{fixture}$ can be derived from (2):

$$f_{PRF_{fixture}} = \frac{1}{2\pi\sqrt{L_{fixture}C_{fixture}}} \tag{2}$$

$C_{fixture}$ can be calculated from impedance curve obtained in the Fixture Open scenario as shown in Fig. 6. After mounting the socket on top of test fixture, PRF becomes:

$$\begin{aligned} f_{PRF_{fixture+socket}} &= \frac{1}{2\pi\sqrt{L_{loop}C_{loop}}} \\ &= \frac{1}{2\pi\sqrt{L_{fixture+socket} \cdot \frac{1}{\frac{1}{C_{socket}} + \frac{1}{C_{fixture}}}}} \end{aligned} \tag{3}$$

where:

$$L_{loop} = L_{fixture+socket} \tag{4}$$

$$C_{loop} = \frac{1}{\frac{1}{C_{socket}} + \frac{1}{C_{fixture}}} \tag{5}$$

Since C_{socket} is very small compared to $C_{fixture}$, the C_{socket} term can be ignored. $L_{fixture+socket}$ then can be derived from (3)

The fixture on the PCB comprises parallel planes with probe contact pads and the socket mounting footprint. Fig. 4 shows the 2D cross-section representation of the fixture. The same fixture design is used for the Fixture Open, Fixture Short, and Socket Mounted cases. A shorting metal is utilized to allow

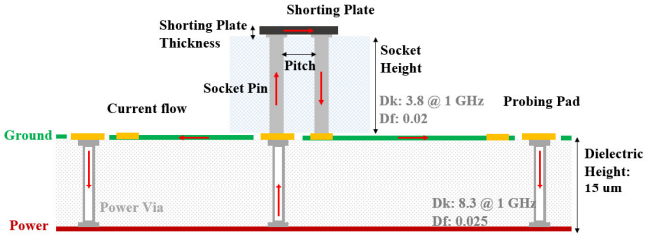

Fig. 4: Fixture + Socket 2D Cross-section diagram. (Dimension not to scale)

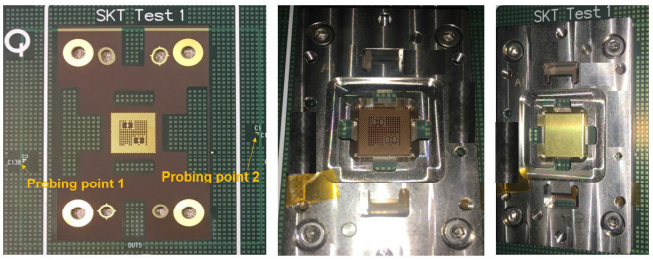

Fig. 5: Fixture design. left: top view of fixture design with two probing points located at edge of the ficture. middle: PCB fixture with socket mounted on top. right: PCB fixture with socket mounted on top and shorting plate is added on top of socket to make a short.

for a loop impedance measurement for the Fixture Short and Socket Mounted. A real fixture design is shown in Fig. 5

In order to correlate measured data to EM simulation results and be able to de-embed the fixture from the socket, three measurements must be made.

1) Fixture Open circuit. The fixture is referred as Open due to the open circuit at the socket footprint when the DUT socket is not mounted. The key design parameters for the Open fixture are governing the size of the planes, finding the minimum thickness, and finding the suitable dielectric with a permittivity value that achieves right amount of capacitance to generate a desired PRF.

2) Fixture Short. The socket footprint will now have a metal short between the positive and negative pins. With the size, thickness, and dielectric material fixed from the Open Fixture design, determining the location of the port landing pad will affect the effectiveness of the PRF. By determining the desired probe landing location, the PRF peak should be at a lower frequency than the cavity mode resonances.

3) Fixture with socket (Socket Mounted). The DUT fixture is essentially the exact copy of the Open fixture. Measurement is done while the socket is mounted and the shorting plate on the top of the socket is applied. The PRF formed by this measurement will include the fixture and the DUT.

Fig. 6 shows the measured impedance of the fixture in the open and short configurations. The impedance measurement of the open fixture allows characterization of the fixture's capacitance. Impedance measurement of the Socket Mounted captures the combined loop inductance and resistance of the fixture and the socket. DC resistance increase dramatically in the presence of the socket pins. The contact resistance of the socket pins dominates the resistance at low frequencies and dampens the Q of the resonance at higher frequencies.

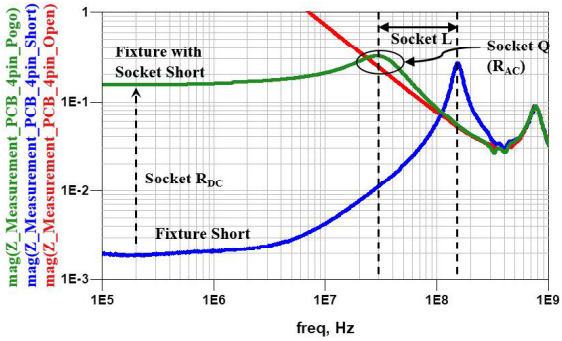

Fig. 6: Measured impedance of the Socket Mounted comparing with fixture.

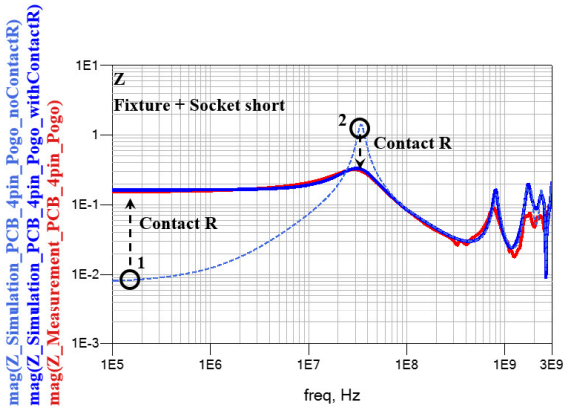

Fig. 7: Fixture Open EM model well correlated with measured data after PCB cross-section. PCB cross-section is used to get the real layer thickness of fixture PCB.

C. Pogo-pin Socket Model Correlation

There are no concerns of port prasitic elements during correlation as the socket was mounted directly on top of the fixture and a shorting plate was used to form the current loop. The solid blue curve in Fig. 7 shows the impedance of the mounted socket model with contact resistance added from simulation and it is well correlated to the measurement. By achieving this close correlation, the socket model is concluded to be a good representation of the socket's electrical performance.

Fig. 7 highlights the importance of contact resistance in the socket. The dashed curve shows the simulation model of the mounted socket pin without modeling additional contact resistance. After tuning the additional representative contact resistance, the simulation model correlates well with measured data at both low and high frequencies. The parallel resonance peak correlates well, which indicates that the AC loop inductance and resistance are modeled accurately. The Q factor is much dampened due to the contact resistance.

REFERENCES

[1] V. Sriboonlue, J. Shin and T. Michalka, "Novel Parallel Resonance Peak Measurement and Lossy Transmission Line Modeling of 2-T and 3-T MLLC Capacitors for PDN Application," *IEEE 67th Electronic Components and Technology Conference*, Lake Buena Vista, 2017.