Extracting the Dynamic Current of a Power Delivery Network

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***Abstract*—Measuring dynamic current at a multi-pin load, such as an FPGA, creates significant challenges. There is no practical way of installing current loop probes, or sense resistors in every power and ground pin pair that connect to the load. This paper demonstrates a practical approach for extracting the dynamic current going into a multipin load component on a PCB. The method uses the creation of an accurate EM model with components of the distributed power delivery network (PDN) in combination with measured voltages at the VRM input to the PDN and at the load on the output of the PDN. This method enables power integrity engineers to see the hidden impact of dynamic current on the power rail noise.**

Keywords—Power Integrity, Power Distribution Network, Dynamic Current, Power Rail Noise, Target Impedance

I. Introduction

Power integrity simulations should be able to predict the dynamic time domain ripple on the power rail. However, this prediction is limited if one does not know the actual dynamic load current. The model in Fig. 1 shows the key elements for a simple power integrity simulation. A voltage regulator module (VRM) supplies the voltage on one side of a PCB power delivery network (PDN), and on the other side is the load represented by the package/die impedance with a dynamic current sink. The challenge is the lack of a good model for the FPGA di/dt dynamic current sink. It is not possible for the consumer of an FPGA component to measure the dynamic current at the die, and even direct measurements of the current going into the FPGA package is problematic with so many power and ground pin connections.

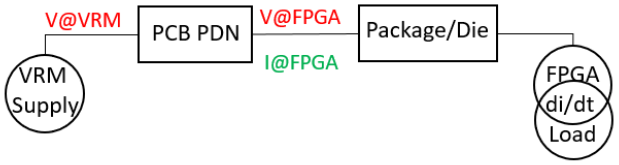

Fig. 1. Key elements of a power integrity simulation: Supply + PCB PDN + Package/Die + Dynamic Load Current.

This paper proposes the use of the easily measured dynamic voltage at the VRM and at the FPGA package pins to synthesize the actual dynamic current at the FPGA pins.

Dynamic voltage measurements can be made with high impedance probes to capture the high frequency transient behavior of the power rail voltage noise ripple [1]. This method of synthesizing dynamic current is shown in Fig. 2 and relies on an accurate model of the PCB PDN and simultaneous measurements of the dynamic voltage at the input and output of the PCB PDN.

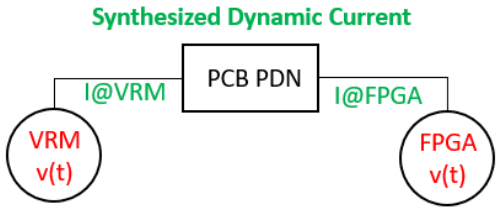

Fig. 2. Dynamic load current at the FPGA is synthesized by simulating the PCB PDN model with measured dynamic voltages at the input VRM side and at the output going to the FPGA load.

The PCB PDN can be modeled as a z-parameter impedance matrix behavioral model. Mathematically this system can be defined by two state equations [2]:

$$I_{VRM} = \frac{V_{VRM}}{Z_{11}} + \frac{V_{VRM}}{Z_{21}}$$

$$I_{FPGA} = \frac{V_{FPGA}}{Z_{21}} + \frac{V_{FPGA}}{Z_{22}} \quad (1)$$

This method of synthesizing dynamic current is demonstrated using the Xilinx Zynq™ ZCU104 FPGA characterization board [3]. The success of the method enables correlation between simulation and measurement to predict worst case noise. The result also highlights that the dynamic voltage ripple is not an accurate predictor of the dynamic noise power and that both dynamic current and voltage are needed.

II. PDN Model

The power delivery network consists of three key parts, the power supply, the PCB power delivery network, and the

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packaged FPGA load. Practical models are needed for each element to predict the time and frequency domain behavior.

A bench top supply with a remote VICOR™ current multiplier module was used as the power supply. This provided a stable low impedance delivery of power to the VCCINT power rail on the ZCU104 board. The output impedance of the power supply was measured and to first order can be represented by a simple series R – L model where R is 3 mOhms measured at low frequency, and the L is 3.33 nH measured in the inductive region at higher frequencies.

The PCB PDN was simulated using Keysight PathWave PIPro FEM simulator to create an EM model of the bare PCB in the form of a multiport s-parameter. This net-based FEM simulator places ports at the pins of the components attached to the VCCINT power rail and then solves for the multiport s-parameter over the frequency of interest. The model of the bare PCB PDN without capacitors was verified with measurements, and then PDN capacitor models attached. It is worth noting that each capacitor value was measured and in every case the vendor model included too much of the mounting inductance that is already a part of the EM model. For this reason, measurements under bias were used to create user models with the mounting inductance removed.

The package/die model can also be represented by an S-parameter supplied by the vendor. To simplify the initial test case and minimize the port count the power pins are grouped together and the ground pins are grouped together to look at the total dynamic current going into the FPGA. The dynamic current load at the die is also grouped to a single output pin to allow a total dynamic load to be applied at the die location. Connecting the package/die s-parameter to an open, short, and matched 5 milliohm load on the PCB input side shows how the PCB impedance can impact the impedance that the die sees, Fig. 3. Matched impedance provides the lowest overall impedance profile, while extremely low impedance increases the impedance peak of the package/die inductance resonating with the die capacitance. It is the frequency of this impedance peak that will be shown to be the worst case noise [4].

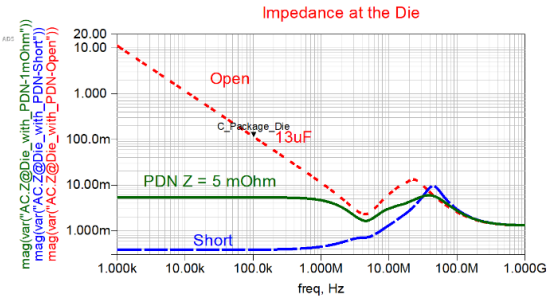

Fig. 3. Connecting the package die model to a PCB open, short, and matched 5 mOhm load shows how the impedance seen by the die is influenced by attaching the PCB PDN. There is no influence above 100MHz.

Connecting these three parts of the power integrity ecosystem together, power supply, PCB PDN, and package/die, shows an impedance profile in Fig. 4 that has an impedance peak at 30 MHz. Measurements actually miss seeing this impedance peak since it is internal to the package/die and measurement locations suffer from the inductance of vias and interconnects.

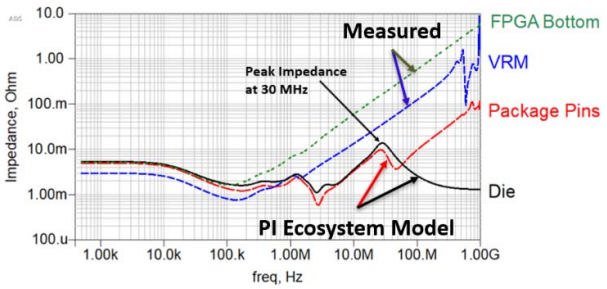

Fig. 4. The PI Ecosystem Model uncovers the impedance peak at 30 MHz that was not seen with measurement. The impedance peak indicates the potential for worst case noise.

This full model of the VCCINT PDN highlights the potential for worst case noise when the impedance peak at 30 MHz is excited with a forcing function at that frequency. The Zynq FPGA has the ability to be programmed to switch all 400,000 flipflops on and off at various clock rates to create a dynamic current load. Two specific clock rates were compared 30 MHz with an average current of 2.5 Amps, and 200 MHz with an average current of 13.5 Amps.

III. Validation with Simulation

To validate the method of synthesizing dynamic current, the method was simulated by attaching a simulated 30 MHz, 2.5 Amp load at the die. The simulation schematic test bench is shown in Fig. 5. This full model of the VCCINT PDN with input 0.87 volts and dynamic current load then generated the dynamic voltages at the input and output of the PCB PDN EM model.

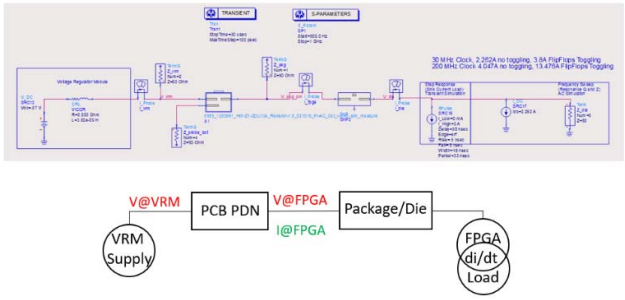

Fig. 5. Test bench for validating the methodology for synthesizing current. A simulated dynamic load is used to simulate the dynamic voltages across the PCB PDN.

The dynamic voltages were then used in a simulation to excite the PCB PDN EM model without the power supply and package/die model. The dynamic current at the input to the FPGA was synthesized from this simulation and then compared with the simulated currents from initial full VCCINT PDN model with dynamic load. The results in Fig. 6 show excellent correlation, even capturing the start-up behavior as the load starts switching.

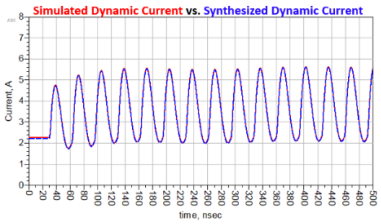

Fig. 6. Simulated currents using the test bench with known simulated currents in red matches well with the synthesized currents in blue.

IV. Measurement Results

After validating the method with simulated dynamic voltages, the next step is to apply the methodology using measured dynamic voltages. Although it is not possible to measure the dynamic current at the FPGA, it is possible to measure dynamic current coming from the power supply. Measuring the current at the VRM can be used as an additional cross check with the synthesized currents. An AC coupled Rogowski current loop was chosen with its small size and minimal impact on the inductance of the power supply connection.

The results in Fig. 7 of the cross check with measured total current at the VRM supply with that of the synthesized total current at the VRM are limited by the performance of the Rogowski probe [5]. However, to first order it shows the similarity of measured current to synthesized current for the step load response when turning on 400,000 flip flops with a 200 MHz toggling rate.

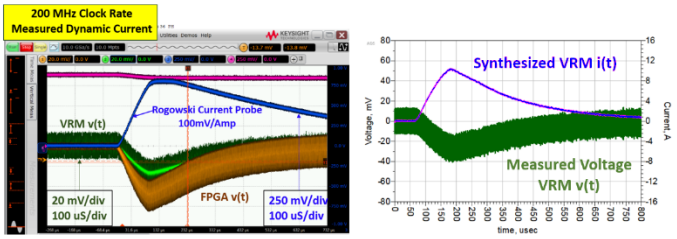

Fig. 7. Total current from the VRM supply was measured with an AC coupled Rogowski probe and compared with the synthesized current from the measured voltages across the PCB PDN.

The VRM current isn't nearly as interesting as what is going on at the FPGA pins. To highlight the benefit of being able to synthesize the dynamic current at the FPGA pins, two toggling rates for the load are used, 200 MHz with 13.5 Amps, and 30 MHz with 2.5 Amps. The results shown in Fig. 8 confirm the predicted worst-case measured voltage ripple is at 30 MHz, not 200 MHz even though the average current is 5 times less.

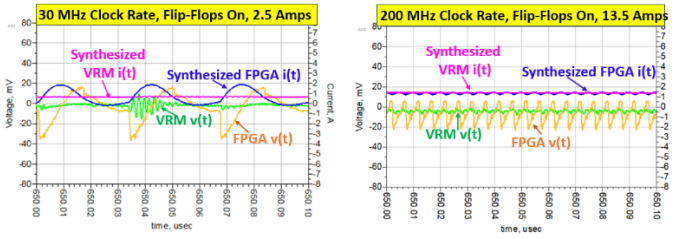

Fig. 8. Results showing synthesized dynamic current at the FPGA in blue for 30 MHz and 200 MHz. The impedance peak at 30 MHz correctly predicts worst case noise for both dynamic current and voltage.

Looking closely at the delta change in noise ripple going from 200 MHz to 30 MHz, as shown in Fig. 9, reveals that the measured voltage ripple is on the order of 2 times worse, but the synthesized current ripple is more than a factor of 10. This means that the AC noise power increased by a larger percentage then what the voltage ripple alone would indicate. Designers worried about EMI/EMC compatibility will benefit from this technique of looking at the noise power and not just step load voltage ripple.

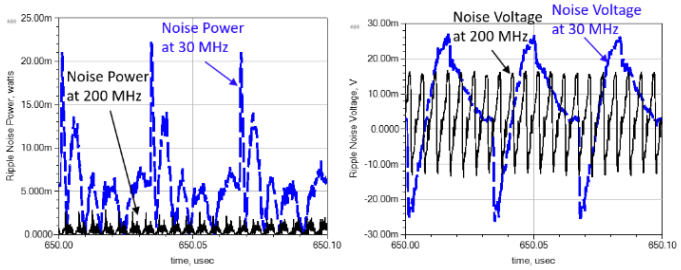

Fig. 9. Multiplying the voltage ripple times the current ripple to get AC noise power shows a factor of 10 increase at 30 MHz compared to 200 MHz, while the voltage is only twice as large.

V. Conclusion

The method of synthesizing the total dynamic current going into the FPGA from two dynamic voltage measurements across the PCB PDN works. The method relies on an accurate model of the full PDN which includes an EM model of the PCB and measured models of the capacitors. This full model has the additional benefit of making it easy to identify the frequency of impedance peaks with the potential for worst case noise. Comparing dynamic voltage ripple and dynamic current ripple at two different load frequencies shows that dynamic voltage alone does not indicate the full magnitude of the noise power.

Acknowledgment

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