Accurate BGA Package Solder Joint Modeling for High Speed SerDes Interfaces

Jiwei Sun
Assembly and Test Technology Development
Intel Corporation
Chandler, USA
jiwei.sun@intel.com

Zhiguo Qian
Assembly and Test Technology Development
Intel Corporation
Chandler, USA
zhiguo.qian@intel.com

Cemil S. Geyik
Assembly and Test Technology Development
Intel Corporation
Chandler, USA
cemil.s.geyik@intel.com

Kemal Aygün
Assembly and Test Technology Development
Intel Corporation
Chandler, USA
kemal.aygun@intel.com

***Abstract*— The solder joint of the ball grid array (BGA) package becomes a performance bottleneck as the serializer/deserializer (SerDes) speeds increase beyond 112 Gbps. This paper presents a comprehensive methodology to correctly model the volume and shape variations of solder joints for both nominal and worst-case electrical models. It is found that it is indispensable to accurately predict the performance of vertical transitions from package to board beyond 30 GHz. Construction of a worst-case solder joint model is also critical to ensure adequate electrical performance for a high-volume manufacturing solution.**

Keywords—BGA package, SerDes, solder joint modeling

I. Introduction

High speed digital standards are evolving towards terabit Ethernet speeds to keep pace with emerging technologies such as 5G, Internet of Things, artificial intelligence, and autonomous vehicles [1]. Over the past ten years, SerDes speeds have dramatically increased from 10 Gbps to 112+ Gbps. Such an aggressive speed scaling has demanded corresponding improvements in channel bandwidth, as the signaling is approaching the Shannon limit [2].

As a key component in input/output channels, BGA packages have been widely used in SerDes solutions. Besides the lateral routing loss in package substrates [3], the vertical transition from package to board also plays an important role [4]-[5]. As SerDes speeds scale beyond 112 Gbps, the solder joint connecting the package substrate to the board creates a big discontinuity in the signaling path and becomes a major bandwidth limiter. Consequently, the assumptions used for past designs that either overlook or oversimplify solder joint modeling are also no longer valid.

This paper focuses on the characteristics of the solder joint formed after the package is mounted to the board. Section II explains the challenging bandwidth demand for the SerDes speed scaling. Section III highlights the importance of shape and volume modeling of solder joints. Section IV introduces an accurate solder joint model for full-wave electromagnetic field solvers. Finally, section V outlines a method to construct a worst-case ball model which is used to investigate the impact of solder joint manufacturing variations on electrical performance.

II. Solder Joint Impact on Speed Scaling

As seen in Fig. 1 (a), the solder joint that connects the package substrate to the board is a major portion of the overall vertical transition in a typical package. It has a substantial impact on multiple electrical performance metrics including impedance, return loss, insertion loss, and crosstalk. This paper focuses on the insertion loss as one of the key performance metrics. Fig. 1 (b) shows the modeled differential insertion loss of a typical vertical transition of a SerDes package designed for 112 Gbps, including micro- vias, plated through holes (PTHs) and solder joints. This result demonstrates that the insertion loss up to 28 GHz, the Nyquist frequency of the Pulse-Amplitude Modulation 4-Level (PAM-4) coding scheme, is less than ~0.5 dB. This accounts for a small portion of the total package loss budget. However, as the speed scales beyond 112 Gbps, the corresponding Nyquist frequency is above 28 GHz with the PAM-4 coding scheme. It can be observed in Fig. 1(b) that the significant roll-off beyond 30 GHz has the slope of ~0.083 dB/GHz, much higher than 0.017 dB/GHz below 30 GHz, resulting in the rapid insertion loss increase. That is too high to meet the package loss budget, and the strong dispersion makes the performance worse. Hence, a higher bandwidth solder joint solution is required to reduce the loss of the vertical transition with low dispersion. In addition, the insertion loss above 30 GHz with a rapid roll-off is more susceptible to solder joint shape variations.

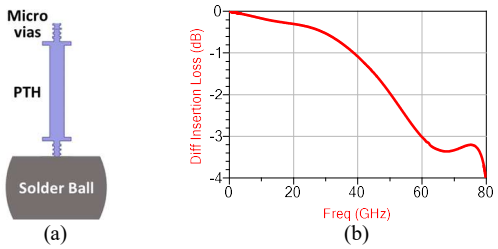


Fig. 1. An example of a typical BGA package vertical transition (a) geometry illustration (b) insertion loss for 112 Gbps SerDes.

III. Solder Joint Modeling Challenges

Full-wave electromagnetic field solvers are widely used to predict the electrical performance of packages. In the past, solder joints of BGA packages are usually approximated as cylinders or spheres with the volume of the incoming solder ball [5]-[6]. This assumption underestimates the loss, especially at frequencies beyond 30 GHz for two reasons. First reason is that the amount of solder volume coming from the solder paste on the package and the board is not considered in this approach. The real solder joint is bigger than what is modeled and therefore has higher parasitics. The total solder volume needs to be correctly calculated to avoid underestimation.

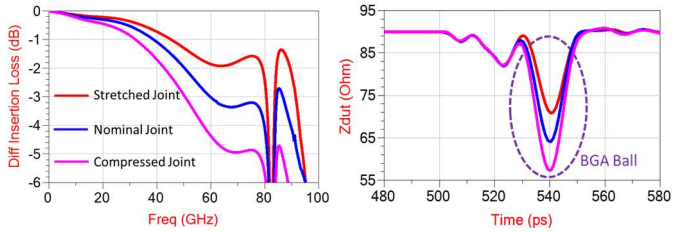
The second reason is that the shape variation after the surface mount process is ignored. As an example, the cross

978-1-7281-6161-7/20/$31.00 ©2020 IEEE

sections of solder joints at different locations of an assembled BGA package are shown in Fig. 2. Despite having similar solder volume, the shape varies significantly due to warpage and board stencil design. Some joints are close to a spherical shape (Fig. 2 (a)), some are stretched to be cylindrical (Fig. 2 (b)), and others are compressed to be elliptical (Fig. 2 (c)). The stretched cylindrical solder joints have the largest height and the smallest width, while the compressed elliptical ones have the smallest height and the largest width. These 3 different shapes are all modeled and compared in Fig. 3. The spherical one is referred to as the nominal case. The stretched cylinder one increases the standoff height by 110 um and achieves better performance than the nominal case. The compressed elliptical one reduces the standoff height by 75 um and results in dramatically worse performance, as shown in Fig. 3 (a). The impedance result based on the time domain reflectometry (TDR) simulations in Fig. 3 (b) show that the compressed solder joint causes the largest capacitance leading to the biggest impedance discontinuity, which is detrimental to the overall performance. Hence, it is critical to have a solder joint model that represents its shape accurately after the surface mount process.

(a) (b) (c)

Fig. 2. (a) Spherical (b) cylindrical and (c) elliptical shape of solder joints at different locations of the same BGA package.



(a) (b)

Fig. 3. Impact of solder joint shape on (a) insertion loss and (b) impedance.

IV. Accurate Solder Joint Modeling

Both the volume and the shape of the solder joint need to be correct to accurately predict the performance. For the solder volume, the solder pastes on both the package and the board also need to be included. There may be non-negligible solder paste on package substrate for the ball attachment. The solder paste on the board for surface mount often has much larger volume, which can be 30-40% of the incoming ball volume, depending on the stencil design. It is imperative to consolidate all the information into the total volume of the solder joints.

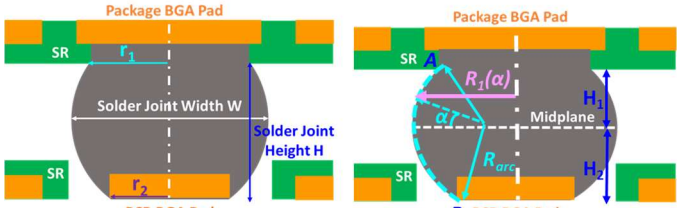
The shape of the solder joint depends on quite a few factors, such as the package-to-board assembly warpage, the package form factor, the stencil design, the location of the joint, etc. This drives the need of two models: One is the nominal model needed for typical performance estimation before the package design starts. The other is the worst-case model required for the electrical performance verification after the package design is completed.

The nominal model is constructed with a truncated sphere [7], as illustrated in Fig. 4 (a). The geometry follows two assumptions: First, the solder joint shape is spherical. Second, for a solder mask defined (SMD) pad, the ball landing radius is equal to the solder resist opening (SRO) radius. While for a metal defined (MD) pad, the ball landing radius is equal to the pad radius. Given the solder joint volume V and ball landing radius of package side r_1 and PCB side r_2, (1) and (2) can be used to calculate the solder joint height H and width W [7] as

$$V = \frac{\pi}{3}\left[\sqrt{R^2 - r_1^2}(2R^2 + r_1^2) + \sqrt{R^2 - r_2^2}(2R^2 + r_2^2)\right] \quad (1)$$

$$H = \sqrt{R^2 - r_1^2} + \sqrt{R^2 - r_2^2} \quad (2)$$

where $R=W/2$ is the spherical solder joint radius. The nominal model can guide the BGA ball size selection and be used in package design studies.



(a) (b)

Fig. 4. (a) Nominal model and (b) worst-case model.

Once the design is completed, a two-step approach can be applied to develop the worst-case BGA ball model. The first step is to extract the solder ball geometries of high-speed SerDes signals. For the balls selected, the compressed ball with the minimum solder joint height and maximum solder joint width is identified as the worst case, since it implies the largest capacitance at BGA ball transition. The second step is to determine the surface profile of the worst-case BGA ball from any two known parameters among solder joint height (H), width (W) and volume (V), based on the following three assumptions. The first is that the solder completely covers a metal defined pad and does not flow beyond the pad. The second is that no solder paste flows out of SRO for a solder mask defined pad. The third is that the meridian defining the surface profile of the solder joint in Fig. 4 (b) is approximated by a circular arc, although the solder ball shape is no longer spherical. In addition, defining the exact worst-case solder joint model requires the midplane, as shown in Fig. 4 (b). With reference to this midplane, the worst-case model can be split into two regions, the upper half and lower half. The key to find the midplane is the arc radius determination, which can be obtained from (3) and (4) below

$$H = H_1 + H_2 = \sqrt{2d_1R_{arc} - d_1^2} + \sqrt{2d_2R_{arc} - d_2^2} \quad (3)$$

$$V = V_1 + V_2 = \int_0^{\theta_1} \pi[R_1(\alpha)]^2 R_{arc}\cos\alpha d\alpha + \int_0^{\theta_2} \pi[R_1(\alpha)]^2 R_{arc}\cos\alpha d\alpha \quad (4)$$

where $d_1 = W/2\text{-}r_1$, $d_2 = W/2\text{-}r_2$, R_{arc} is the arc radius, H_1 and V_1 are the upper half height and volume, H_2 and V_2 are the lower half height and volume, respectively. $R_1(\alpha)$ shown in Fig. 4 (b) is given by

$$R_1(\alpha) = W/2 - R_{arc}(1 - \cos\ \alpha) \quad (5)$$

where α is the angle between R_{arc} and the midplane. Equation (4) can be solved for the integration variable α using the boundary conditions, where, at position A, $\alpha = \theta_1 = arctan(H_1/(R_{arc} - d_1))$, and at position B, $\alpha = \theta_2 = arctan(H_2/(R_{arc} - d_2))$. When $d_1 = d_2$ and $\theta_1 = \theta_2$, the worst-case solder joint is symmetric about the midplane. Generally, the smallest solder joint height or the largest solder joint width leads to the worst-case model.

V. Application of The Worst-Case Solder Joint Model

The worst-case solder joint model results in a larger capacitance, so it creates a low impedance discontinuity and consequently causes insertion loss increase. Primary parameters considered for the worst-case model demonstrated above include solder joint width, height, volume and shape. For SerDes speeds beyond 112 Gbps, the impact of the parameters on solder joint capacitance and insertion loss of the vertical transition becomes more notable. As a result, the utilization of the worst-case model is critical for high-volume manufacturing solutions targeting these speeds. Such models can help determine the impact of the solder joint variation on the electrical performance and optimize the assembly process accordingly.

In Fig. 5, the impact of solder joint width and height variation on solder joint capacitance is shown as an example. The capacitance increase is relative to a baseline, i.e., nominal solder joint model, which is the lower-right corner in the plot. Clearly, solder joint width is the dominant parameter in ball capacitance increase. When the width variation is less than 40 um, the capacitance increase is not sensitive to the height reduction. Also, for large width variations (> 40 um), every 10 um increase in width can increase the capacitance by ~6 fF, which is about two times than the capacitance increase for small width variations (< 30 um).

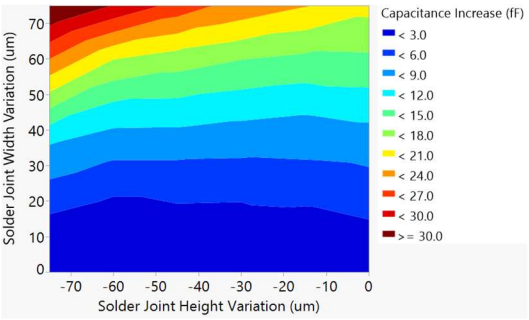


Fig. 5. Impact of solder joint width and height variation on ball capacitance.

Similarly, an example of the solder joint variation impact on insertion loss of the vertical transition beyond 30 GHz is shown in Fig. 6. The contour plot shows how the insertion loss increases as the solder joint width increases and the solder joint height decreases. A 40 um increase in joint width from the baseline causes more than 0.5 dB extra loss, corresponding to about 12 fF solder joint capacitance increase. When the width is well controlled to less than 20 um increase, the ball capacitance and loss increase are less than 6 fF and 0.3 dB, respectively. It's evident that a 0.2 dB insertion loss is attributed to every 6 fF solder joint capacitance increase. As illustrated in Fig. 6, the joint width also shows much bigger impact on the insertion loss increase than the solder joint height. Therefore, to meet the loss target, the most important parameter to control is the solder joint width. For instance, the white dash line indicates the variation limit of 0.1 dB loss increase. This sets the requirement of the maximum joint width and the minimum joint height for an example product implementation. Advancements in assembly technology may be required to achieve such a variation control.

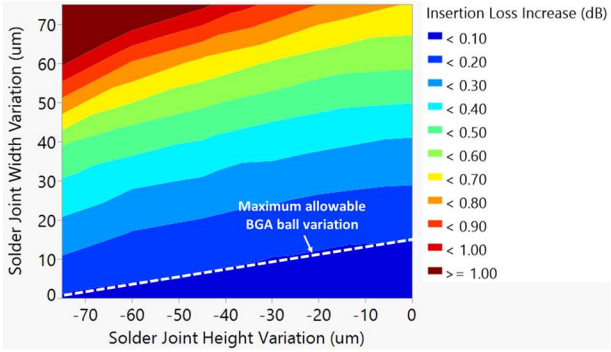


Fig. 6. Insertion loss dependence on solder joint width and height.

VI. Conclusions

Solder joints of BGA packages become a major bandwidth limiter as SerDes speed scales beyond 112 Gbps. This paper introduces a solder joint modeling methodology to accurately capture the impact of the volume and shape variation of the solder ball for electrical performance analysis. Based on this methodology, the worst-case solder joint models are used to determine the key parameters for solder joint assembly that can meet the product electrical performance requirements of future high speed SerDes interfaces.

Acknowledgment

The authors would like to acknowledge the following colleagues for their technical supports: Patrick Nardi, John Harper, and Hemanth Dhavaleswarapu.

References

[1] "2020 Ethernet roadmap: the past, present and future of Ethernet." [Online]. Available: https://ethernetalliance.org/technology/2020-roadmap/

[2] C. E. Shannon, "A mathematical theory of communication," *Bell Syst. Tech. J.*, vol. 27, no. 4, pp. 623-656, July 1948.

[3] C. S. Geyik *et al.*, "Impact of Use Conditions on Dielectric and Conductor Material Models for High-Speed Package Interconnects," *IEEE Trans on Compon., Packag., Manuf. Technol.*, vol. 9, no. 10, pp. 1942-1951, Oct. 2019.

[4] Q. Zhu *et al.*, "Package Design Optimization for Intel SoC Xeon-D," *IEEE Trans on Compon., Packag., Manuf. Technol.*, vol. 8, no. 4, pp. 531-537, April 2018.

[5] J. Lim *et al.*, "ASIC package to board BGA discontinuity characterizationin >10 Gbps SerDes Links," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Denver, CO, USA, Aug. 5–9, 2013, pp. 569–574.

[6] S. Jin *et al.*, "Analytical equivalent circuit modeling for BGA in high speed package," *IEEE Trans. Electromagn. Compat.*, vol. 60, no. 1, pp. 68–76.

[7] K. Chiang and C. Yuan, "An overview of solder bump shape prediction algorithms with validation," *IEEE Trans. Adv. Packag.*, vol. 24, no. 2, pp. 158–162, May 2001.