An Inspection Based Method to Analyse Deterministic Noise in N-port Circuits

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***Abstract*— This paper proposes the estimation by inspection method to analyse the impact of deterministic supply noise on the design specifications of the analog and mixed signal (AMS) systems. The method is based on the indefinite admittance matrix (IAM) method. The voltage gain, phase and input-output impedance have been considered as the design specifications. To validate the method, two examples of output stages for analog and digital blocks have been simulated in standard 0.18 μm technology with 1.8 V of supply and same geometric area. The proposed models using the inspection method and the SPICE based simulations shows maximum mean percentage error (MPE) of 3% for all the examples.**

***Index Terms*— Two-port network, indefinite admittance matrix (IAM), deterministic supply noise, signal integrity.**

I. Introduction

Power supply noise is one of the dominant factors which degrades the performance of any high-speed AMS system [1]. The common causes of power supply noise are simultaneous switching noise, insertion-loss, reflection, electromagnetic interference, etc. [2]. The variations in the supply voltage, known as power supply noise (PSN), may affect the signal integrity (SI) of the system. The SI of analog and digital blocks of the AMS system depends on the primary design parameters such as gain, phase and input-output (I/O) impedance. In case of noisy power supply, deviations in these parameters may occur and hence the performance of the system will be degraded. Therefore, the causes and impacts of these quantities under supply/bulk fluctuations need to be investigated for deep sub-micron technologies.

For the estimation of the aforementioned-design parameters, a two port network analysis is widely used to describe the I/O behavior of a system [3]. In the recent years, the two-port network theory was used in many complex systems to analyse the input-output behavior of the systems [4], [5]. In the literature, the modeling of two-port network parameters including the effects of PSN, ground supply noise (GSN) and bulk-supply noise (BSN) has not been reported yet.

In this paper, the standard two-port network analysis using the IAM is extended and a new method, estimation-by-inspection for multi-input port is proposed to understand the effects in the presence of supply noise. The initial results of this work are presented in [6]. The inspection method derives crucial SI metrics such as gain, phase, I/O impedance and output transient response in the closed-form expressions. These expressions are derived to form a generalised two-port network for an active circuit having N-terminals.

II. Proposed Analysis for an N-port Network

A. Estimation by Inspection Method

The IAM, is a zero sum matrix ($n \times n$ singular matrix), the reference terminal of which is at an arbitrary potential which lies outside the network. The procedure to write IAM and design parameters for two-port networks are discussed in [7]. However, the standard IAM method is not valid for the estimation of design parameters in case of multiple terminals.

Algorithm 1 Proposed algorithm to calculate two-port parameters for the generalised multi-port system.

Input: v_{na}, v_{in}, v_b, v_{bn}, v_{bp} and angular frequency (ω)
Output: A_{v_i}, $\tilde{A}_v$, Z_i, $\tilde{\phi}$

1: Initialise : p = Number of input terminals, o = output terminal (v_{out}), i_m = main input terminal of a circuit.
2: Draw the small-signal model and assign the node numbers.
3: Compute the required IAM elements for a circuit with all the deterministic noise sources.
4: **for** $i = 1$ to p **do**
4: $A_{v_i} = \frac{-|Y_{o,i}|}{|Y_{o,o}|}$
4: $Z_i = \frac{Y_{o,o}}{\begin{vmatrix} Y_{i,i} & Y_{i,o} \\ Y_{o,i} & Y_{o,o} \end{vmatrix}}$; $Z_{out} = \frac{|Y_{i_m,i_m}|}{\begin{vmatrix} Y_{i_m,i_m} & Y_{i_m,o} \\ Y_{o,i_m} & Y_{o,o} \end{vmatrix}}$
4: $i = i + 1$
5: **end for**
6: $\tilde{A}_v = \sum_{i=1}^{p} A_{v_i}$
7: $\tilde{\phi} = \pi - \angle \tilde{A}_v(j\omega)$
8: **return** Two port parameters

For multi-input terminals, the estimation-by-inspection method, based on the IAM approach is used to compute the two-port parameters. Here, multiple inputs refer to the different deterministic supply noise sources. The abbreviations used for the PSN, p-bulk, n-bulk, ground, common-mode noise and input voltage sources are v_{na}, v_{bp}, v_{bn}, GND, v_b and v_{in}, respectively. The first step of the method is to draw the small-signal model of the circuit with all the deterministic supply noise sources. In the next step, the node numbers need to be assigned in the small-signal model. After that, the required IAM ($Y_{i,i}$, $Y_{o,o}$, $Y_{o,i}$, $Y_{i,o}$) elements are extracted for the circuit including all the nodes. The $Y_{i,i}$ and $Y_{o,o}$ refer to the self admittance parameters of input and output nodes, respectively. $Y_{o,i}$ and $Y_{i,o}$ are the negative signed mutual admittance parameters between output-to-input and input-to-

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output nodes, respectively. Next, to determine the closed-form equations of the required parameters, the superposition theorem has been applied on the circuit by selecting one excited input node at a time. Finally, the transfer function (TF), impedance, overall gain and the overall phase expressions can be calculated using the Algorithm 1. The derivations of these formulae are skipped for the interest of readers.

B. Validation of the Proposed Method

The proposed method of multi-port analysis by inspection is validated using two examples viz. a CMOS inverter and a chain of inverters, in the presence of PSN and BSN. For the sake of simplicity and a proof of concept, the GSN has not been considered. In this method, the circuits are analysed with respect to the lowest potential i.e. GND.

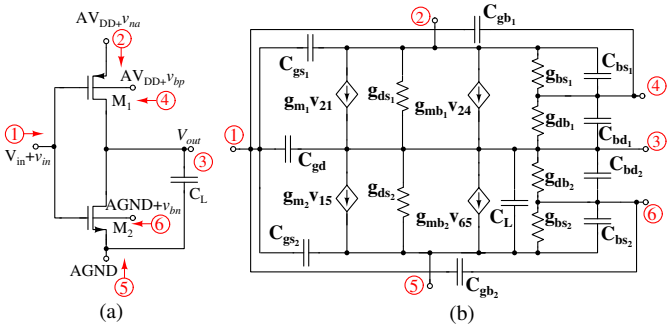


Fig. 1: The CMOS inverter (a) schematic diagram and (b) equivalent small-signal model.

Example-I: CMOS inverter

The CMOS inverters have diverse applications in AMS system as a class-AB push-pull amplifier, high-speed buffer, output driver and a transmission gate. The schematic and the small-signal diagram of an inverter is depicted in Fig. 1. The possible paths of supply noise in the circuit are denoted by red circled arrows in the Fig. 1(a). The required IAM parameters to estimate the TFs and I/O impedance are mentioned in Table I.

TABLE I: The required IAM parameters for the inverter.

Y_{ij}	Expressions	Y_{ij}	Expressions
Y_{11}	$s(C_{gd}+C_{gs}+C_{gb})$	Y_{13}	$-sC_{gd}$
Y_{22}	$s(C_{gs_1}+C_{bs_1})+\gamma_3$	Y_{23}	$-g_{ds_1}$
Y_{31}	$g_{m_1}+g_{m_2}-sC_{gd}$	Y_{32}	$-g_{m_1}-g_{mb_1}-g_{ds_1}$
Y_{33}	$g_{ds}+g_{bd}+sC_1$	Y_{34}	$g_{mb_1}-g_{bd_1}-sC_{bd_1}$
Y_{35}	$-g_{ds_2}-g_{mb_2}-sC_L$	Y_{36}	$g_{mb_2}-g_{bd_2}-sC_{bd_2}$
Y_{43}	$-g_{bd_1}-sC_{bd_1}$	Y_{44}	$g_{bs_1}+g_{bd_1}+s(C_{bd_1}+C_{bs_1}+C_{gb_1})$
Y_{63}	$-g_{bd_2}-sC_{bd_2}$	Y_{66}	$g_{bs_2}+g_{bd_2}+s(C_{bd_2}+C_{bs_2}+C_{gb_2})$

The voltage gain, phase and the impedance expressions for the inverter can be formulated as:

$$A_{v1_{inv}} = \frac{-g_{m_1}-g_{m_2}+sC_{gd}}{\gamma_1+sC_1}, \quad A_{v2_{inv}} = \frac{g_{m_1}+g_{mb_1}+g_{ds_1}}{\gamma_1+sC_1}, \tag{1}$$

$$A_{v4_{inv}} = \frac{-g_{mb_1}+g_{bd_1}+sC_{bd_1}}{\gamma_1+sC_1}, \quad A_{v6_{inv}} = \frac{-g_{mb_2}+g_{bd_2}+sC_{bd_2}}{\gamma_1+sC_1} \tag{2}$$

$$Z_{1_{inv}} = \frac{\gamma_1+sC_1}{s^2(C_2C_1-C_{gd}^2)+s(C_2\gamma_1+g_mC_{gd})}, \tag{3}$$

$$Z_{2_{inv}} = \frac{\gamma_1+sC_1}{\alpha_1 s^2+\alpha_2 s+\alpha_3}, \tag{4}$$

$$Z_{3_{inv}} = Z_{out_{inv}} = \frac{sC_2}{s^2(C_1C_2-C_{gd}^2)+s(g_mC_{gd}+C_2\gamma_1)}, \tag{5}$$

$$Z_{4_{inv}} = \frac{\gamma_1+sC_1}{\alpha_4 s^2+\alpha_5 s+\alpha_6}, \quad Z_{6_{inv}} = \frac{\gamma_1+sC_1}{\alpha_7 s^2+\alpha_8 s+\alpha_9}, \tag{6}$$

where, $C_{gs} = C_{gs_1}+C_{gs_2}$, $C_{gd} = C_{gd_1}+C_{gd_2}$, $C_{db} = C_{db1}+C_{db2}$, $C_1 = C_{gd}+C_{db}+C_L$, $C_2 = C_{gd}+C_{gs}+C_{gb}$, $\gamma_1 = g_{ds}+g_{db}$, $g_{ds} = g_{ds_1}+g_{ds_2}$, $g_m = g_{m_1}+g_{m_2}$, $\gamma_2 = g_{ds_1}+g_{bs_1}+g_{m_1}+g_{mb_1}$, $\alpha_1 = C_1(C_{gs_1}+C_{bs_1})$, $\alpha_2 = C_1\gamma_2+\gamma_1(C_{gs_1}+C_{bs_1})$, $\alpha_3 = \gamma_1\gamma_2-g_{ds_1}(g_{m_1}+g_{mb_1}+g_{ds_1})$, $\alpha_4 = C_1(C_{bd_1}+C_{bs_1})-C_{bd_1}^2$, $\alpha_5 = C_1(g_{bs_1}+g_{bd_1})+\gamma_1(C_{bd_1}+C_{bs_1})-C_{bd_1}(2g_{bd_1}-g_{mb_1})$, $\alpha_6 = \gamma_1(g_{bs_1}+g_{bd_1})-(g_{bd_1}-g_{mb_1})g_{bd_1}$, $\alpha_7 = C_1(C_{bd_2}+C_{bs_2})-C_{bd_2}^2$, $\alpha_8 = C_1(g_{bs_2}+g_{bd_2})+\gamma_1(C_{bd_2}+C_{bs_2})-C_{bd_2}(2g_{bd_2}-g_{mb_2})$, $\alpha_9 = \gamma_1(g_{bs_2}+g_{bd_2})-(g_{bd_2}-g_{mb_2})g_{bd_2}$.

Here, the subscript in the gain (A) and the impedance (Z) expressions refer to the input terminal. For example, $A_{v1_{inv}}$ is the input-output voltage gain and $Z_{1_{inv}}$ is impedance at terminal ① of an inverter circuit. The overall voltage gain ($\tilde{A}_{v_{inv}}$) of the inverter is:

$$\tilde{A}_{v_{inv}} = G_{m_{inv}}Z_{out_{inv}}, \tag{7}$$

$$G_{m_{inv}} = \frac{A_{v1_{inv}}(1+\zeta)[s^2(C_1C_2-C_{gd}^2)+s(g_mC_{gd}+C_2\gamma_1)]}{s(C_{gd}+C_{gs}+C_{gb})}, \tag{8}$$

$$\zeta = \frac{g_{mb_2}-g_{m_1}-g_{ds_1}-g_{bd}-sC_{bd}}{g_m-sC_{gd}}. \tag{9}$$

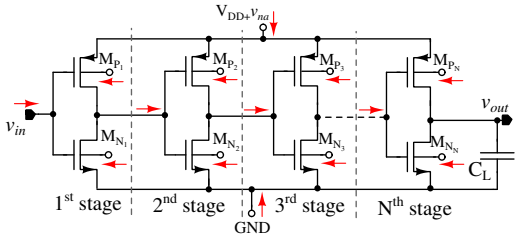


Fig. 2: Schematic diagram of a chain of CMOS inverters.

The overall output response ($\tilde{V}_{o_{inv}}$) of CMOS inverter due to deterministic noise fluctuations is as follows:

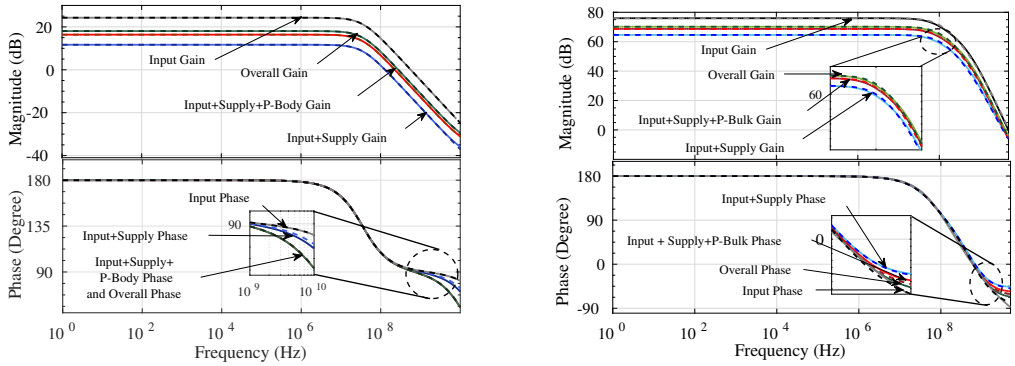
$$\tilde{V}_{o_{inv}} = A_{v1_{inv}}(v_{in}+\frac{Y_{32}}{Y_{31}}v_{na}+\frac{Y_{34}}{Y_{31}}v_{bp}+\frac{Y_{36}}{Y_{31}}v_{bn}). \tag{10}$$

Example-II: N-stages Inverter Chain

Fig. 2 shows such N-stages of chain considering the supply/bulk/common-mode noise (denoted by red colored arrows). The required two-port model expressions for the chain can be written in a similar way as discussed in the previous example. The impedance and phase expressions for the respective terminals are the same as derived for the inverter. The overall gain ($A'_{v_{ch}}$) with all the supply noise sources for an N-stages of inverter chain is:

$$A'_{v_{ch}} = \sum_{n=2}^{N}\left(\prod_{k=n}^{N}\left(\frac{Y_{o1}}{Y_{oo}}\right)_k\left(\frac{\sum_{i=1}^{p-1}(Y_{oi})}{(Y_{oo})}\right)_{n-1}\right) + \prod_{n=1}^{N}\left(\frac{Y_{o1}}{Y_{oo}}\right)_n + \left(\frac{\sum_{i=1}^{p-1}(Y_{oi})}{(Y_{oo})}\right)_N \tag{11}$$

where, N is total number of stages in an inverter chain and p refers to the input noise sources in a single stage. The derivation of the $A'_{v_{ch}}$ and the other details of two-parameters for the inverter chain are omitted due to space constraints.



(a) (b)

Fig. 3: Frequency and phase response due to the combination of noise sources for: (a) the CMOS inverter and; (b) the cascaded three stage CMOS inverter.

III. Results and Discussions

In order to verify the proposed approach, two example circuits are designed in a standard 180 nm CMOS technology with supply voltage of 1.8 V and a load capacitor of 100 fF. The DC model parameters have been calculated using the SPICE based simulations and BSIM model.

Fig. 3(a) and (b) compare the analytical and simulation results of the single inverter and three-stage inverter, respectively. The analytical results are shown by dashed line whereas, the solid lines are for the simulation results. The impact of combination of different noise sources on the I/O gain and the phase behavior for the CMOS inverter and the three stage inverter are shown in Fig. 3(a) and (b), respectively. These different combinations of noise sources include the effect of supply, common-mode and bulk noises. The combined response of pull-up transistor due to supply and input node is the difference of the individual gain of these two node. This composite response in the presence of the PSN and input node noise is lowest among the other combinations as they are out-of-phase from each other. The analytical plot matches accurately with the simulation results with MPE of 3%.

IV. Insights and Usage of the Proposed Analysis

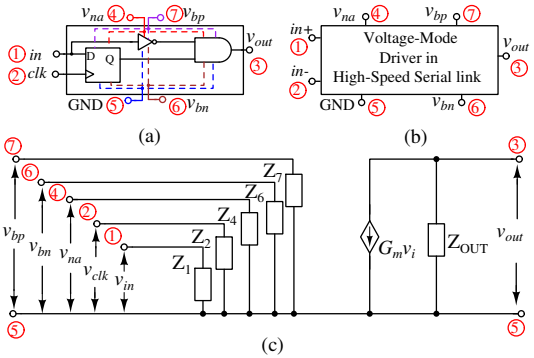


Fig. 4: (a) Edge detector circuit and, (b) voltage-mode driver circuit [8] with its (c) equivalent N-port network.

Fig. 4 shows the generalised two-port network for high-speed AMS block when the excited signals are applied at gate, supply and bulk nodes. Here, the word *generalised* means that Fig. 4(a) and (b) or any other system can be realised in the form of a two-port network as shown in Fig. 4(c). Consider an example of an edge detector circuit, depicted in Fig. 4(a) which has multiple-terminals viz. in, clk, v_{na}, GND, v_{bn}, v_{bp} and v_{out}. The deterministic noise may disturb the DC voltage at these terminals and may degrade the SI of the system. Therefore, the SI effects due to supply noise can be analysed using the modified two-port network, shown in Fig. 4(c). Note that, the outputs of an AMS circuits are generally taken from drain to drain abutted output of nMOS and pMOS. This makes the circuit with high output impedance and hence, the circuits are modeled as transconductance amplifier with the PSN, GSN and the BSN. Here, Z_i is the impedance at the node ⓘ. The G_m depends on number of input ports and it can be changed by varying the input sources (v_i). These metrics are estimated using the proposed method. Moreover, the other circuits can be modelled using the proposed method in the similar fashion.

V. Conclusions

A method, estimation-by-inspection, is proposed to model the design parameters for a multi-port AMS system in the presence of noisy supplies. The mathematical model of the performance metrics viz. A_v, Z_i and ϕ, under the influence of PSN, GSN, BSN and common-mode noises are derived. On the basis of derived TFs, the gain cross over frequency, gain margin, phase margin and, subsequently, stability can be predicted. The method is not only limited to simple two transistors based circuits, but, can be extended for the system level blocks such as op-amp, flip-flops, data converters, etc.

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