Gauss-Newton Method for Performance Evaluation of Decoupling Capacitors on Resonant Parallel Plates

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***Abstract*—A Gauss-Newton (G-N) based method is proposed for optimal placement and performance evaluation of local decoupling capacitors on resonant parallel-plates. Multiple power pins are used as a leverage for simultaneous placement optimization of multiple capacitors by utilizing matrix calculus methods. The algorithm converges in a few iterations, which is a big improvement against the competing evolutionary methods. The proposed method is tested on a sample case and the results are observed to be valid across a practically wide frequency range.**

***Index Terms*—decoupling capacitors, gauss-newton, newton-raphson, power delivery network, power integrity.**

I. Introduction

With design concerns like limited space resources and manufacturing yield issues of printed circuit boards (PCB), the selection and placement of decoupling capacitors have always been among the major priorities of power integrity (PI) analysis. The complexity of a PCB structure makes model generation for PI analysis very challenging especially at high frequencies. While some design parameters like the capacitance value, type, parasitics, etc. could be relatively easy to address, calculations for the optimum placement configuration could be extremely challenging especially for design techniques that rely on numerical EM methods.

Optimal placement and value of decoupling capacitors have long been researched in the literature and industrial circles [1]-[8]. Due to the large number of optimization parameters involved, evolutionary algorithms have become prominent and some of these techniques were implemented in commercial PI analysis tools. Despite their success, the large number of iterations and lack of convergence to a unique solution even for the same initial conditions stand out as the two major drawbacks of evolutionary algorithms. It's possible to address both of these issues by using gradient methods which can converge to a unique solution in a few iterations under favorable initial conditions.

From a practical point, the implementation of evolutionary algorithms is fairly straightforward, provided that a suitable objective function can be found. On the other hand, considerable preliminary work is needed for gradient algorithms. Especially, the calculation of derivatives could be quite involved in the case of multiple capacitors and power pins.

In the past, some research efforts have been devoted with the application of Newton-Raphson (N-R) method to basic cases involving a single capacitor and a power pin port [9]. Although the complexity of the problem impeded the immediate application of the technique to practical cases, the theoretical advancements laid out the groundwork to improve the gradient-based algorithms.

In this paper, N-R method is advanced to the case involving multiple power pins and decoupling capacitors, which represent a more realistic and practical design scenario. The previously developed scalar expressions for the impedance of a power pin and its partial derivative for N-R iterations are extended to multiple pins and capacitors using matrix calculus techniques. The proposed G-N based method allows the *simultaneous* optimization and performance evaluation of *multiple* decoupling capacitors in a few iteration steps.

This document is organized as follows. In Section II, the theoretical analysis is presented. This is followed by Section III, which the proposed model is validated on a numerical example and conclusions are provided in Section IV.

II. Theory of the Proposed Model

In a system involving P number of power pins and M number of capacitors, the pin impedance matrix $\boldsymbol{Z}_{in}$ can be expressed as follows:

$$\boldsymbol{Z}_{in} = \boldsymbol{Z}_{PP} - \boldsymbol{Z}_{PM} \left[\boldsymbol{Z}_{MM} + \boldsymbol{Z}_c\right]^{-1} \boldsymbol{Z}_{MP} \tag{1}$$

where the impedance matrices, $\boldsymbol{Z}_{PP}$ and $\boldsymbol{Z}_{MM}$ with entries $Z_{ij}(s)$ $(i,\ j \in \{1, ..., P+M\})$ represent distributed circuit parameters of power pins and capacitor ports, respectively. The parameter s is the complex angular frequency. The matrix $\boldsymbol{Z}_{PM}$ and its transpose relate the pin and capacitor ports. $\boldsymbol{Z}_c$ is a diagonal matrix of size M, whose elements $Z_c(s)$ are defined by the impedance of decoupling capacitors at the corresponding port locations. The variable $Z_c(s)$ can be represented by its the lead-length parasitic resistance, R, and inductance, L as follows.

$$Z_c(s) = R + sL + \frac{1}{sC} \tag{2}$$

with C being the capacitance.

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For rectangular parallel plates of size a and b which are separated by a gap of d, $Z_{ij}(s)$ is given by the following compact relation [10]:

$$Z_{ij}(s) = \frac{\mu d}{ab} \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{\chi_n \chi_m \sigma_{nmij} \psi_{nmij}}{\beta_n^2 + \beta_m^2 - \beta^2} \quad (3)$$

where μ is permittivity of the medium; $\beta_n = \frac{n\pi}{a}$ and $\beta_m = \frac{m\pi}{b}$ are the eigenvalues of standing waves inside the parallel plates. β is the wavenumber and $\chi_{nm} = \left\{ \begin{array}{c} 1,\ n,\ m=0 \\ \sqrt{2},\ otherwise \end{array} \right\}$ The remaining variables in (3) are expressed as follows:

$$\begin{aligned} \psi_{nmij} =& \cos(\beta_m x_i)\cos(\beta_n y_i) \times \\ & \cos(\beta_m(x_i + r\cos\phi))\cos(\beta_n(y_i + r\sin\phi)) \end{aligned} \quad (4)$$

where x_i and y_i represent the associated port coordinates, r and ϕ are the distance and angle between the ports, respectively. Here,

$$\begin{aligned} \sigma_{nmij} =& \operatorname{sinc}(\beta_m w_{xi})\operatorname{sinc}(\beta_n w_{yi}) \times \\ & \operatorname{sinc}(\beta_m w_{xj})\operatorname{sinc}(\beta_n w_{yj}) \end{aligned} \quad (5)$$

where w_{xi} and w_{yi} represent the associated port sizes.

Let the Ψ represent the set of coordinates on the plane pair for decoupling capacitors:

$$\Psi = \{r, \phi | r, \phi \in \mathbb{R}^{2M}; r_1, \phi_1, ..., r_M, \phi_M\} \quad (6)$$

Assuming there's a set of coordinates Ψ_0 for which $Z_{in}(s, \Psi_0)$ becomes minimum, one can define the impedance compromise parameter, q as follows:

$$q = \left| \frac{Z_{in}(s, \Psi_q)}{Z_{in}(s, \Psi_0)} \right| \quad (7)$$

.

It has been established that the elements of Ψ_0 are those closest to the observed pin location [9]. In order to evaluate the performance of decoupling capacitors with respect to the specified pin location, the vector function $\boldsymbol{f}(s, \Psi)$ is defined as follows:

$$\boldsymbol{f}(s, \Psi) = |\boldsymbol{Z}_{in}(s, \Psi)| - q\,|\boldsymbol{Z}_{in}(s, \Psi_0)| \quad (8)$$

The analytical nature of (3) makes the gradient-based algorithms a prime candidate for the solution of Ψ_q. The Newton-Raphson (N-R) method is a suitable choice for the iterative solution to the vector function $\boldsymbol{f}(s, \Psi)$ as follows:

$$\Psi_{k+1} = \Psi_k - \nabla \boldsymbol{f}_k^{-1}(s, \Psi)\boldsymbol{f}_k(s, \Psi) \quad (9)$$

From (9), it is clear that $P \geq 2M$ is required. If $P > 2M$ $\nabla \boldsymbol{f}_k(s, \Psi)$ becomes overdetermined and (9) needs to be modified as follows:

$$\Psi_{k+1} = \Psi_k - \nabla \boldsymbol{f}_k^{+}(s, \Psi)\boldsymbol{f}_k(s, \Psi) \quad (10)$$

where $\nabla \boldsymbol{f}_k^{+}(s, \Psi)$ is the pseudo-inverse of $\nabla \boldsymbol{f}_k(s, \Psi)$ which is defined as

$$\nabla \boldsymbol{f}_k^{+}(s, \Psi) = [\nabla \boldsymbol{f}_k^{T}(s, \Psi) \nabla \boldsymbol{f}_k(s, \Psi)]^{-1} \nabla \boldsymbol{f}_k^{T}(s, \Psi) \quad (11)$$

The relation (10) is also referred to as Gauss-Newton iteration [11]. Regardless of the deterministic nature of $\nabla \boldsymbol{f}_k(s, \Psi)$, calculation of its entries requires the partial derivatives of $\boldsymbol{Z}_{in}(s, \Psi)$ which can be expressed as follows by using the chain rule in matrix calculus [12]:

$$\begin{aligned} \boldsymbol{Z'}_{in}(s, \Psi) =& 2\boldsymbol{Z}_{MP}\left[\boldsymbol{Z}_{MM} + \boldsymbol{Z}_c\right]^{-1} \boldsymbol{Z}'_{PM} - \boldsymbol{Z}_{MP} \\ & \times \left[\boldsymbol{Z}_{MM} + \boldsymbol{Z}_c\right]^{-1} \boldsymbol{Z'}_{MM} \left[\boldsymbol{Z}_{MM} + \boldsymbol{Z}_c\right]^{-1} \\ & \times \boldsymbol{Z}_{PM} \end{aligned} \quad (12)$$

The parameters Z_{ij} constitute the building blocks of (9), (10) and (12) as the key elements of Newton's algorithm whose convergence depends on the precise evaluation of $\nabla \boldsymbol{f}_k(s, \Psi)$. In the evaluation of the derivatives, the analytical expression of the parameters Z'_{ij} were derived in [9].

III. Numerical Example

The validity of the proposed method will be demonstrated on a pair of rectangular parallel-plates which represent power and ground plane conductors. The two planes are sized on x-y coordinates as 125 mm by 75 mm with a dielectric thickness of 0.127 mm which separates them in the z-dimension. The effective permittivity and the loss tangent of the dielectric slab are 4.5 and 0.02, respectively. Sixteen power pins with a 1 mm pitch spacing are shown with the cluster of circular pegs in Fig. 1. Three decoupling capacitors are initially placed within 0.8 mm distance of a power pin which is selected as the observation port for the proposed calculation method. The placement of capacitors is marked with the three grey square pegs in Fig. 1. All capacitors are modeled as 100 nF with lead length parasitics of R_p = 58 mΩ and L_p = 200 pH.

The pin impedance for this initial configuration is calculated as $30m\Omega$ and taken as a reference for values pertaining to other placement configurations. As the 3 capacitors are moved away from the observation pin, its impedance tends to increase. In order to find the placement configuration for which the pin impedance increases by a specified amount q, the capacitors can be gradually moved away from the observation location as the impedance is checked at incremental distances. While this could be regarded as a viable method for the assessment of a single capacitor, the number of radial and angular possibilities for the simultaneous displacement of all 3 capacitors are overwhelmingly large even for the simple case discussed in this example.

A practical solution comes with the proposed G-N iterations. In this example $q = 2$ is assumed. The required placement of capacitors is then calculated with the proposed method after only three iterations at the selected 60 MHz and shown in Fig. 1 with 3 black square pegs. The analysis takes into account the mutual interaction among the capacitors as well as with the power pins while evaluating their placement. The placement configuration can be interpreted as the region within which the effectiveness of capacitors will not be reduced more than half with respect to the power pin cluster.

The resulting pin impedance curve is plotted in Fig. 2 as a function of frequency in comparison to the reference case. The impedance values at 60 MHz are indicated with circular marks ($30m\Omega$ for the reference and $60m\Omega$ for the final case). Although the frequency is set to 60 MHz in the G-N iterations, a similar $q = 2$ ratio can be observed for the pin impedance magnitude up to 250 MHz between the two configurations. Besides that, calculations are also conducted at other frequencies and similarly fast convergence is observed for the G-N iterations as summarized in Table I.

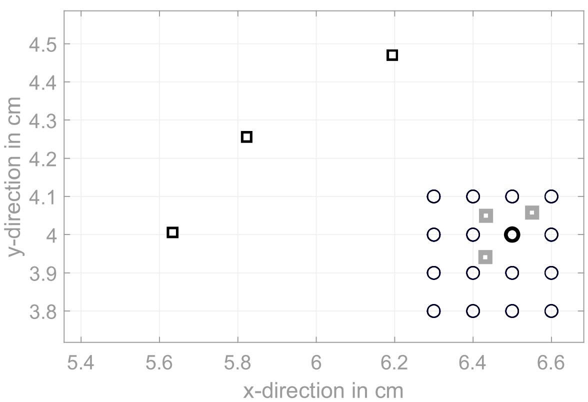

Fig. 1. The assumed configuration for the numerical example with the power pin cluster of circular pegs and decoupling capacitors (square pegs). The initial placement of the capacitors are marked with thick grey square pegs inside the BGA area close to the reference pin (marked with the bold circle) among the others. The calculated final positions of the capacitors are marked with black square pegs outside the BGA area.

The simulations are conducted in an *Intel i7* platform using *MATLAB R2019b*. With the selected initial placement of the 3 capacitors, the proposed algorithm takes a few iterations as summarized in Table I. It should be noted that the proposed G-N method for the optimal placement of multipin/multicapacitor problem can also be applied to other impedance criteria like the specification of a target impedance instead of the impedance increasing to a certain value.

TABLE I
NUMERICAL DATA FOR G-N ITERATIONS AT SELECTED FREQUENCIES

Frequency (MHz)	$\lvert Z_{in}(r_q)\rvert$ $(m\Omega)$	$\lvert Z_{in}(r_{q0})\rvert$ $(m\Omega)$	# G-N iterations	time (sec)
60	60.0	30.0	3	32.9
120	131.0	65.0	6	69.6
180	240.0	120.0	5	59.9
240	585.0	262.0	2	22.6

IV. CONCLUSION

In this work, the G-N method is developed for the analysis of PDNs involving multiple power pins and decoupling capacitors. By utilizing matrix calculus techniques, G-N method is tailored for PI optimization and shown as a viable alternative to the evolutionary algorithms. The proposed method allows the simultaneous optimization and performance evaluation of multiple decoupling capacitors in a few iteration steps.

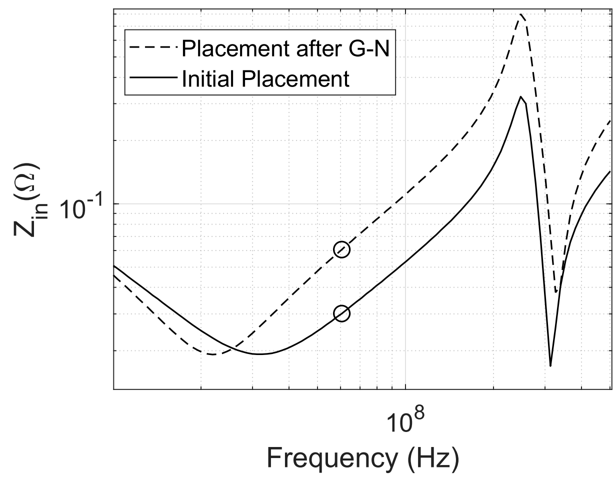

Fig. 2. Magnitude of the input impedance of the highlighted power pin of the configuration shown in Fig. 1. The calculation impedance is marked with circles on the two curves.

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