Recent Progress on Signal Integrity Modeling of Neuromorphic Chips by the PEEC Method

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***Abstract*—With the rapid advances of artificial intelligence and its applications, the design of memristor-based neuromorphic chips inspired by the human brain has become an important area of research. Signal integrity issues, such as crosstalk and IR drop, affect the performance of these chips and necessitate the use of signal integrity modeling and analysis methods during the early stages of chips design. In this mini review, we summarize recent progress on the application of the Partial Element Equivalent Circuit (PEEC) method to the signal integrity modeling of neuromorphic chips.**

Keywords—Neuromorphic chips, signal integrity, partial element equivalent circuit.

I. Introduction

Artificial intelligence (AI) has experienced ups and downs since it was formally put forward at Dartmouth Conference in 1956, and is now in the third wave of development and achieving new breakthroughs in many fields such as finance, medical care, education, transportation, logistics, security, leisure and entertainment. However, due to the "memory wall" problem of the traditional von Neumann architecture, efficient execution of artificial intelligence operations has become a huge challenge. Therefore, more and more world-leading scientific research institutions and companies have begun to focus on new artificial intelligence hardware and actively promote the research and development of neuromorphic chips [1-2].

Inspired by the working mechanism of human brain, neuromorphic chips are composed of devices that imitate neurons and synapses, which are more in line with biological characteristics with low energy consumption and high efficiency, thus holding the promise of super-high computing power, autonomous learning ability, and perceptual computing power beyond that of modern digital computers. Memristor-based neuromorphic chip [3-4] is a typical circuit architecture of neuromorphic chips, which adopts a crossbar array structure, utilizes memristors as artificial neural synapses, and realizes signal transmission between crisscross interconnecting wires. Such chip design reduces the steps of accessing the off-chip memory when acquiring data, and simply realizes the vector matrix multiplication on the circuit level. This results in higher learning ability and improved efficiency of AI computing.

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Memristor-based neuromorphic chips occupy a smaller area with lower power consumption compared with neuromorphic hardware based on traditional devices. However, due to the unstable device performance, special circuit structure, high integration and high operation speed, the reliability of the memristor-based neuromorphic chips is still poor. In particular, the driving signal of neuromorphic chips often shows transient time-varying pulse characteristics, which has the unique characteristics of low power consumption, low delay and space-time combination. Meanwhile, the integration of neuromorphic chips with other functional chips in a complex electromagnetic environment, calls for assessment of their signal integrity (SI) and power integrity during operation. For example, Fig. 1, depicts three SI concerns, namely, IR drop, crosstalk, and sneak path, which may affect operation and performance. Thus, it is necessary to consider the SI problems in the design stage of neuromorphic chips.

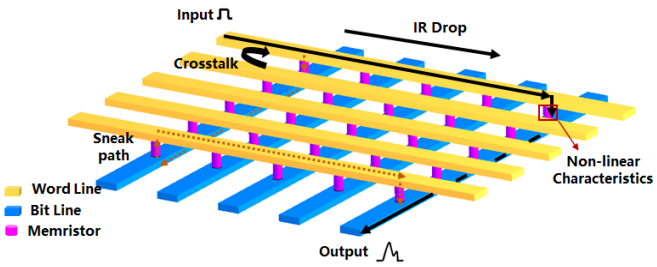

Fig. 1. Typical signal integrity issues in memristor-based neuromorphic chips.

At present, several modeling, analysis and design methods are being used to investigate signal integrity issues in memristor-based neuromorphic chips. Among them, the Partial Element Equivalent Circuit (PEEC) method [5] has been widely considered and studied. This paper reviews recent progress on the application of PEEC to signal and power integrity analysis of neuromorphic chips. Furthermore, starting from the development of PEEC method in memristor-based neuromorphic chips, this paper introduces the theory of extracting parasitic parameters of neuromorphic chips by PEEC method in detail, and discusses future research opportunities.

II. Equivalent Circuit Modeling of Memristor-based Neuromorphic Chips

As depicted in Fig. 1, memristor-based neuromorphic chips have periodic structure, which is composed of memristor and interconnection lines. Establishing the equivalent circuit model of crossbar array circuit offers an intuitive and convenient

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method to analyze signal integrity issues of neuromorphic chips. Included in the development of the equivalent circuit model is the modeling of the interconnection lines.

In early efforts, most circuit modeling of memristor-based neuromorphic chips only focused on accounting for the resistance of the interconnection lines, ignoring the influence of propagation delay and electromagnetic coupling on performance [6-7]. Such modeling is effective when the line width in memristor-based neuromorphic chips is of nanometer scale. For such cases, there are two typical signal integrity problems in neuromorphic chips: IR-drop and sneak path. However, when the wire width is larger and of micron-scale, the influence of the electromagnetic behavior of the interconnects must be accounted for in order to correctly predict the impact of voltage degradation, time delay, overshoot, crosstalk and coupling on the performance of the neuromorphic chips.

Commercial software (e.g., ANSYS Q3D Extractor) can be utilized to extract the relevant interconnect parameters for electromagnetic modeling of memristor-based neuromorphic chips [8]. Alternatively, PEEC modeling has been used to analyze the electromagnetic effect of the memristor-based neuromorphic chip, and study the recognition rate of the classification tasks [9]. A novel approach combining the PEEC method and domain decomposition was proposed in [10] for the modeling of structures depicted in Fig. 2. Using this method, the authors analyzed the influence of interconnection parasitic effects on the online training and testing process of neuromorphic chips [10]. This approach can be extended to any array size. Using this approach, the research team extended the signal integrity research of memristor-based neuromorphic chip to the examination of the influence of parasitic effect on spiking signal transmission [11] and STDP learning mechanism [12], and developed spike signal sequence [13] as well as STDP learning curve [14] which is more suitable for hardware implementation.

From the above, it is clear that the PEEC method offers a convenient equivalent circuit-based electromagnetic modeling framework to analyze the impact of electromagnetic effects on the performance of memristor-based neuromorphic chips. In the following, we provide a brief summary of the ways to generate the PEEC model, for crossbar array geometries depicted in Fig. 2. The reader is directed to [9]-[13] for more details.

III. Comprehensive PEEC Modeling Theory of Memristor based Neuromorphic Chips

The PEEC method is based on the electric field integral equation and interprets the electromagnetic field interactions described by the integral equation between electrically small elements of the structure under study into equivalent circuits. The time-domain PEEC method is very suitable for the modeling of the neuromorphic crossbar array because it is compatible with programming and is able to flexibly model the variation of the memristor conductance during neural network training process. The basic modeling method for crossbar array based on PEEC is described next.

A. Partial Elements Calculation

The first two steps of PEEC involve the discretization of the interconnect structure and the calculation of the elements of the PEEC circuit. Referring to Fig. 2, the partial resistance R can be directly calculated by:

$$R = \frac{\rho l}{wh}, \tag{1}$$

where ρ stands for resistivity, l, w and h represent unit wire length, width and height, respectively. Neglecting electromagnetic retardation effects for the purposes of this modeling, the partial inductance between cells m and n is calculated as:

$$Lp_{mn} = \frac{\mu_0}{4\pi a_m a_n} \int_{v_m} \int_{v_n} \frac{1}{|\vec{r_m} - \vec{r_n}|} dv_m dv_n, \tag{2}$$

where a_m and a_n are the cross-sections, which are perpendicular to the direction of current, of cells m and n, respectively. v_m and v_n are the volumes of volume cell m and n, respectively. $\vec{r_m}$ and $\vec{r_n}$ are the centers of volume cell m and n, respectively. The partial coefficient of potential between area cells i and j is given by

$$p_{ij} = \frac{1}{S_i S_j} \frac{1}{4\pi\varepsilon_0} \int_{S_i} \int_{S_j} \frac{1}{|\vec{r_i} - \vec{r_j}|} dS_j dS_i, \tag{3}$$

where S_i and S_j are the surface areas of area cells i and j, respectively. $\vec{r_i}$ and $\vec{r_j}$ are the centers of area cells of i and j, respectively.

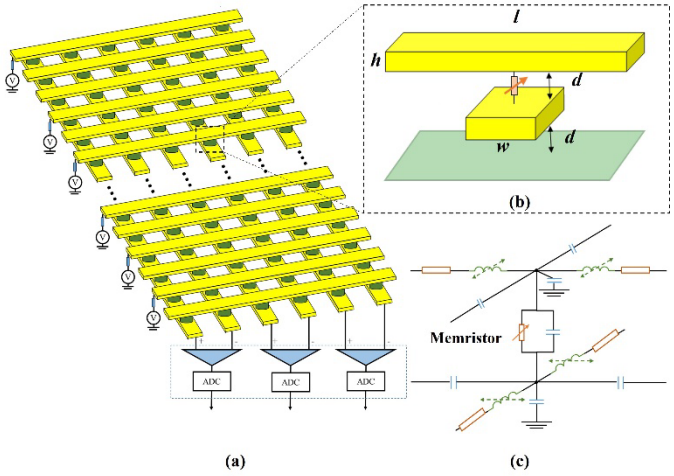

Fig. 2. Circuit modeling method for memristor-based neuromorphic chips [10]. (a) memristor-based neuromorphic chip; (b) and (c) are unit cell and equivalent circuit model based on PEEC. Reprinted with permission from [10]. Copyright 2021 IEEE.

B. PEEC Circuit Model

For the solution of PEECs in the time and frequency domain, a Modified Nodal Analysis (MNA) method is presented. The MNA method is widely used in modern circuit analysis software due to its full-spectrum properties and flexibility to include additional circuit elements. The calculated values of all the partial elements, as detailed in the previous section, are stored in

matrices to facilitate the formulation of the circuit equations. The resulting time domain matrix equation can be written as:

$$\begin{bmatrix} -\boldsymbol{H} & -\left(\boldsymbol{R}+\boldsymbol{L}\frac{d}{dt}\right) \\ \boldsymbol{C}\frac{d}{dt} & -\boldsymbol{H}^{T} \end{bmatrix} \begin{bmatrix} \boldsymbol{V} \\ \boldsymbol{I} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_{S} \\ \boldsymbol{0} \end{bmatrix}, \tag{4}$$

where $\boldsymbol{R}$, $\boldsymbol{L}$, $\boldsymbol{C}$ represent, respectively, the resistance, inductance, and short circuit capacitance matrix, $\boldsymbol{H}$ represents the connectivity matrix, and $\boldsymbol{Vs}$ is the voltage source excitation. $\boldsymbol{V}$ and $\boldsymbol{I}$ are node voltages and branch currents to be solved. Such PEEC based circuit modeling method was utilized to analyze the output signals of memristor-based neuromorphic chips [10]. The output currents before ADCs of the farthest vertical line (bit line) matched well with the 3D full-wave simulation outcomes obtained through ANSYS HFSS for a 100x6 memristor-based neuromorphic chip, as depicted in Fig. 3 (a) and (b). As shown in Fig. 3 (c) and (d), PEEC modeling method was also successfully applied to analyze the effects of different circuit structure designs [11] and input signal parameters [13] on output signal.

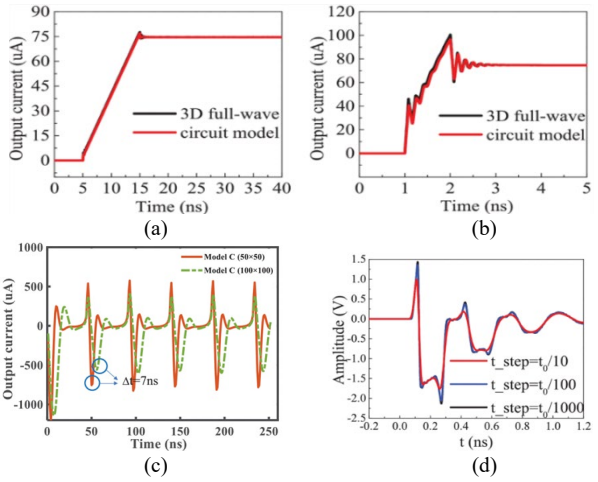

Fig. 3. Neuromorphic chip analysis using PEEC modeling method: (a) and (b) comparisons between PEEC modeling and ANSYS HFSS simulation results with input signal rise times of 10 ns and 1 ns, respectively. Reprinted with permission from [10]. Copyright 2021 IEEE. (c) output signal with different crossbar array sizes. Reprinted with permission from [11]. Copyright 2022 IEEE. (d) output signal with different input signal parameters. Reprinted with permission from [13]. Copyright 2023 IEEE.

IV. Discussion and Future Prospects

While currently the PEEC method has been proven to be an effective tool for memristor-based neuromorphic chips, it can be further improved in the following aspects: 1) High Frequency Modeling: The PEEC model described above does not include electromagnetic retardation effects. Thus, while its accuracy is sufficient at lower frequencies, it becomes inaccurate at high frequencies. Including electromagnetic retardation will allow us to improve its accuracy across a wider frequency range. 2) Memristor Modeling: As a new device, memristor is not a mature technology, so it is difficult to maintain consistency, stability and achieve high-density integration scale. In view of the different and complex working mechanism and characteristics of memristor, optimizing the modeling method of memristor and reducing the modeling error can effectively improve the design efficiency and yield of Memristor. 3) SI-PI-EMI Co-Simulation: Besides SI issues, the proposed PEEC-based modeling can be extended to study power integrity (PI) and electromagnetic interference (EMI) effects on the performance of memristor-based neuromorphic chips.

V. Conclusion

The application of the PEEC method to the signal integrity analysis of memristor-based neuromorphic chips has been reviewed in this paper. Given the relevance of neuromorphic chips to computing systems for AI applications, modeling methodologies that can predict the impact of electromagnetic effects on the performance of such chips need to be advanced and implemented. As discussed in this paper, PEEC offers a mature and intuitive equivalent circuit modeling framework to support such analysis.

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