# Design and Analysis of an Irregular-Shaped Power Distribution Network (PDN) for High Bandwidth Memory (HBM) Interposer

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***Abstract*—In this paper, we design and analyze the irregular-shaped power distribution network (PDN) for high bandwidth memory (HBM) interposer, taking into account practical application considerations. HBM is a promising solution to meet the high performance memory requirements of artificial intelligence (AI) applications, offering exceptional bandwidth with vast number of input/outputs (I/Os). The extensive I/Os switching operations can generate significant power noise, challenging power integrity with conventional uniform PDN designs. Therefore, a realistic and accurate design and analysis of the HBM interposer PDN, which accounts for irregularities in the PDN shape, becomes critical to ensure power integrity. Previous works focused on uniform PDN designs of the HBM interposer without considering these irregularities. We design the PDN of the HBM3 interposer based on practical considerations like ballmap from JEDEC and the routability of memory channels. We then model and analyze the PDN, including the power/ground through silicon via (P/G TSV), in the 10 MHz to 30 GHz frequency domain. The results show that we can effectively analyze the precise effects of the PDN by considering the irregular-shape of the PDN in real applications.**

***Index Terms*—High bandwidth memory (HBM), PDN impedance, Power distribution network (PDN), Power integrity, Silicon interposer**

## I. Introduction

Recently, the demand for artificial intelligence (AI) processors is increasingly driven by the escalating computation required for advanced algorithms and models of AI such as ChatGPT. The graphics processing unit (GPU) - high bandwidth memory (HBM) module, shown in Fig. 1, is widely used as a solution for these AI processors because of its extensive parallelism with 1024 I/Os per stack. To embrace the tremendous number of input/outputs (I/Os), it is inevitable to apply the silicon interposer which enables dense interconnections with fine pitch between the processor and HBM.

However, the large number of switching operations induces substantial simultaneous switching noise (SSN), derived from the product of the PDN impedance and the current spectrum flowing through the PDN. This underlines the importance of precise PDN analysis, as the accuracy of SSN directly relies on the accuracy of PDN impedance assessment. Although there have been research on designing and analyzing the PDN of HBM [1] with uniform-shaped PDNs, the non-uniform shape of the HBM PDN must be taken into account, given that PDN designs in real-world applications seldom conform to rectangular form for accurate analysis of power integrity.

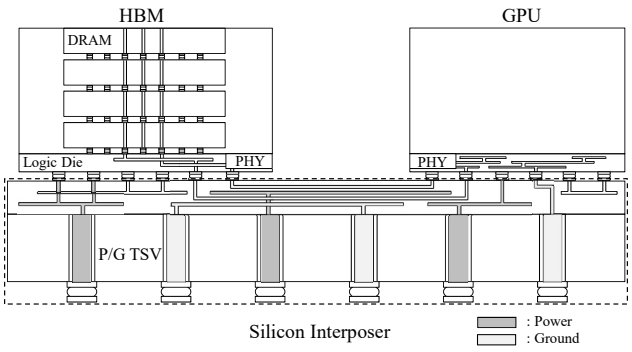


Fig. 1. The cross-sectional view of the GPU-HBM module for a graphics processing unit (GPU), illustrating the PDN of the HBM interposer.

In this paper, we design the irregular-shaped PDN for the HBM3 interposer considering practical design features. For analysis, we construct the PDN model of the P/G plane and P/G TSV within the designed HBM3 interposer, utilizing the W-element modeling method. By analyzing the PDN impedance, we show that a more precise analysis can be achieved by modeling the irregular structure of HBM PDN.

## II. Design of the Irregular-shaped HBM3 Interposer Power Distribution Network

In this section, we focus on designing the irregular-shaped PDN of the HBM3 interposer memory interface, where the HBM3 stack and the GPU is connected. The practical factors in real applications, such as the JEDEC ballmap of HBM and the routability of the memory channel, are considered for the PDN design.

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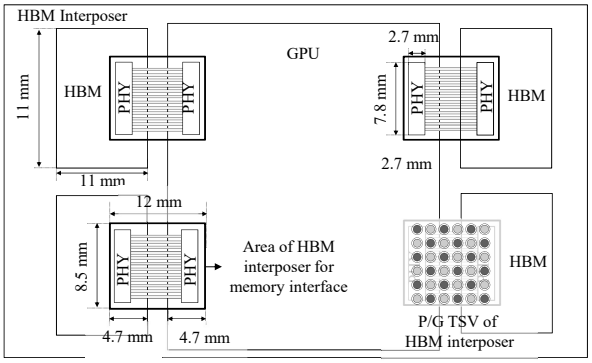
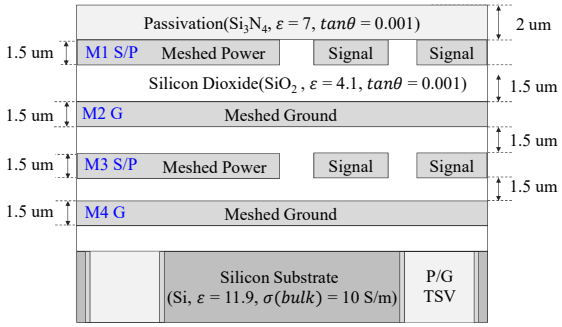



(a)




(b)

Fig. 2. (a) Top view of HBM interposer, illustrating the area for memory interface to the GPU. (b) Stack-up design of silicon interposer with 4 metal layers.

We design an irregular-shaped PDN for the HBM3 interposer memory interface that connects the HBM3 stacks to a GPU. As depicted in Fig. 2 (a), the dimensions of the memory interface area are 12 mm x 8.5 mm, accommodating 1024 memory channel interconnections. To allow for these numerous interconnections within a compact routing layer, we design the signal channels to reside in the same layer as the meshed power planes, resulting in an irregular-shaped power plane. Additionally, the PDN of the HBM interposer features a meshed type P/G plane with 75% metal density and 10 um unit mesh size, which exhibits less inductance and resistance than grid type P/G planes [1], [2]. Furthermore, the P/G TSVs are strategically positioned beneath the stack-up of the interposer, optimizing the PDN design for performance and efficiency.

The irregular-shaped HBM3 interposer stack-up includes four metal layers, with M1 and M3 layers accommodating both memory channels for signal routing and meshed power planes, and M2 and M4 layers designed solely as meshed ground planes, as shown in Fig. 2 (b). We design the interposer so that each VDDQ and VDDQL domain, which powers the HBM3 memory interface [3], is placed on the M1 and M3 layers, respectively. To optimize utilization within these confined layers, M1 and M3 have gaps for the signal routing from the HBM3 and GPU, leading to irregular-shaped power planes. Each metal and dielectric layer is 1.5 um thick, with a passivation layer of 2 um and a silicon substrate of 100 um on top and bottom of the interposer, respectively.

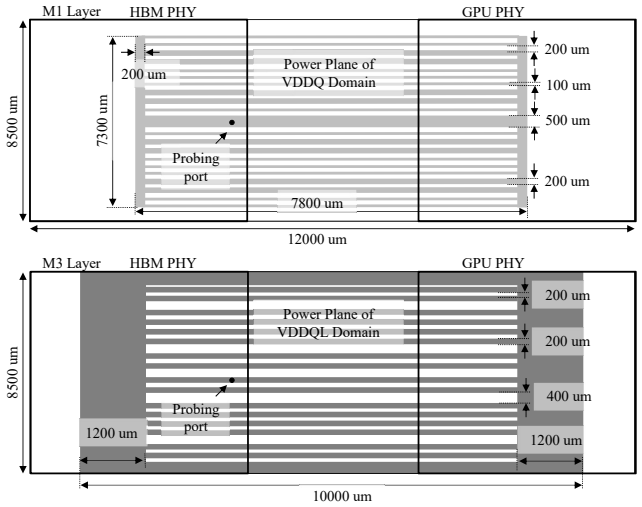
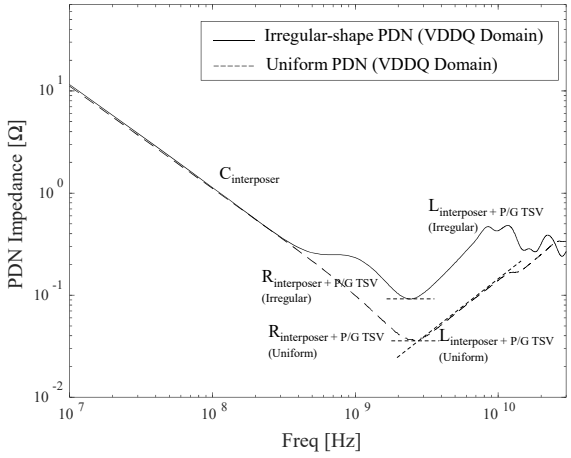



Fig. 3. Design of the non-uniform VDDQ and VDDQL domain power planes within the M1 and M3 layers of the HBM interposer.

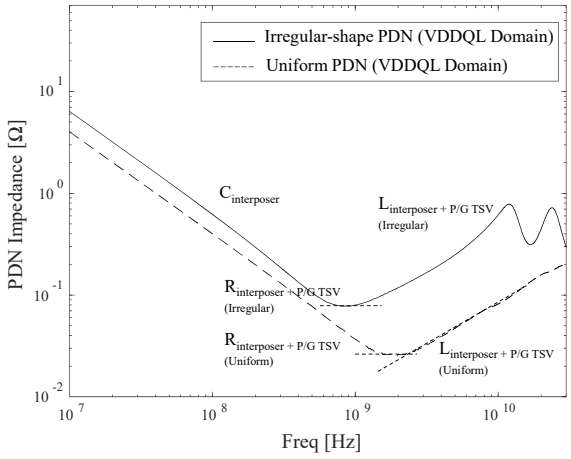
Fig. 3 illustrates the design for the power planes of the VDDQ and VDDQL domain, placed inside the area of HBM3 memory interface. The VDDQ and VDDQL power plane each occupy an area of 7300 um x 78000 um and 8500 um x 10000 um. Inside both power planes there are gaps with a length of 7800 um. The power plane is designed to have sufficient gaps for the routing of 1024 signal channels. Assuming that the power plane under the HBM3 PHY and GPU PHY are symmetric, the patterns from the power plane are designed based on the ballmap of the HBM3 JEDEC standard [3]. The ballmap shows the positioning of microbumps connecting the interposer to the logic die of HBM3, with each of its purposes denoted, whether if its for the VDDQ/VDDQL power domains, ground, or signal. Patterns for the VDDQ and VDDQL power planes align directly beneath their respective microbumps to allow vertical connections. Therefore, the irregular-shaped PDN design of the HBM3 interposer successfully integrates the complex design features of numerous signal channel routing and the JEDEC ballmap specification.

## III. Analysis of the Irregular-shaped PDN for HBM Interposer

In this section, we analyze the PDN impedance of the HBM3 interposer designed in section II. To analyze the PDN impedance of HBM3, the irregular-shaped interposer PDN and P/G TSV are modeled. The unit cell of the irregular-shaped interposer with a size of 10 um x 10 um is modeled by the W-element modeling method [4]. Then 5694 and 8500 unit cells are concatenated to form each VDDQ domain and VDDQL domain with the segmentation method. 156 P/G TSVs in the interposer located under the metal layers are modeled with an equivalent circuit model [5]. The P/G TSV is designed to have dimensions of 15 um diameter, 100 um height, 300 um pitch, 0.5 um thickness of the isolation silicon dioxide.




(a)




(b)

Fig. 4. (a) Comparison of the PDN impedance of the proposed irregular-shape PDN and uniform PDN of the M1 layer and (b) M3 layer.

The PDN impedance of the irregular-shaped power planes for the VDDQ and VDDQL domains is compared to that of uniform rectangular-shaped power planes, as shown in Fig. 4 (a) and (b). These comparisons are made using planes of equivalent sizes, 7300 um x 7800 um and 8500 um x 10000 um. The simulation results of the PDN impedance are taken from the probing port located under the area of HBM, from 10 MHz to 30 GHz to observe the difference of PDN impedance from the irregular-shaped power plane.

In both comparisons, the PDN impedance of the proposed irregular-shaped PDN is found to be higher than that of the PDN with uniform power planes. In the lower frequency range of 10 MHz to 500 MHz, the gaps within the power planes contribute to a reduction in the overall capacitance, subsequently leading to an increase in the PDN impedance. In higher frequencies, the PDN impedance of the irregular-shaped PDN is higher than that of the PDN with uniform power planes. This increase is attributed to the increase in inductance due to the extension of the current path in the irregular-shaped PDN [6]. This also causes plane resonance to appear at lower frequencies. Hence, the irregular configuration, including gaps within the power plane, results in higher PDN impedance.

Our analysis reveals that the PDN impedance increases when we account for the irregularities of the PDN as opposed to considering the power planes as uniform structures. Since the increase in PDN impedance is directly related to higher SSN, it is critical to analyze an accurate PDN design. Thus, by incorporating realistic factors into the design of the HBM3 interposer PDN, we can significantly refine the precision of the power integrity analysis of HBM3.

## IV. Conclusion

In this paper, we design and analyze the irregular-shaped power distribution network (PDN) for high bandwidth memory (HBM) interposer, taking into account practical design features. The irregular-shaped PDN of the HBM3 interposer is designed, integrating the stack-up of the HBM3 interposer and considering realistic elements. Then the designed PDN including the P/G TSV is modeled and analyzed. We show that the PDN impedance is higher than that of uniform PDNs due to the capacitive and inductive features of the irregular-shaped PDN. Therefore, we highlight that by integrating practical considerations into the design of the HBM interposer PDN we can significantly improve the accuracy of the power integrity analysis of HBM.

## V. Acknowledgement

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