HBM3 PPA Performance Evaluation by TSV Model with Micro-Bump and Hybrid Bonding

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***Abstract*—In this paper, through-silicon via (TSV) circuit models for the third generation of high bandwidth memory (HBM3) are developed utilizing 3D IC stacking technology with micro-bump or hybrid bonding. A good agreement between the results of the equivalent model and the full-wave simulation would be seen. In addition, the power, performance, and area (PPA) metrics of both stacking techniques are analyzed and compared. In all aspects, the hybrid bonding technique is more effective.**

Keywords—Signal integrity (SI), PPA, hybrid bonding, high bandwidth memory (HBM), through-silicon via (TSV)

I. INTRODUCTION

The need for high-performance computing (HPC) is growing due to advancements in artificial intelligence (AI), machine learning (ML), and other industrial applications, driving the demand for high-bandwidth systems. As depicted in Fig. 1, the most anticipated solution in current literature is adopting high bandwidth memory (HBM), primarily based on using through-silicon via (TSV) technology to integrate dynamic random-access memory (DRAM) on a single chip vertically. In contrast to traditional wire bonding, the TSVs structure is served as the interconnector between the upper and lower layers of the chip [1].

Compared to HBM2E, as shown in Table I [2], the transmission speed of HBM3 is doubled to 6.4 Gbps, and the number of stacked layers is increased to 12 layers. Therefore, signal integrity (SI) issues are increasingly important in HBM3. In previous studies, SI improvement methods were mainly focused on dimensional variables and patterns of TSVs [3] - [5]. However, the micro-bump structure is another crucial factor affecting SI performance. This is because the length of the interconnect and the degree of discontinuity between TSV and bump greatly influence the insertion loss and far-end crosstalk (FEXT). Recently, a new 3D stacking technology, called hybrid bonding, is gradually being applied to HBM architecture because it can directly connect the TSV and the Cu pad [5]. The fine pitch limit is overcome, and the interconnect length is reduced [6]. However, there is a lack of systematic SI-related investigation on hybrid bonding. In this paper, a hybrid bonding equivalent circuit is constructed. Moreover, a comprehensive analysis and comparison of the power, performance, and area (PPA) metrics between micro-bump and hybrid bonding are presented.

The rest of this article is divided into the following sections. Section II presents the modeling and verification of the equivalent circuit model of micro-bump and hybrid bonding. Section III compares the PPA metric of both technologies. Section IV concludes this paper.

II. STRUCTURE AND EQUIVALENT CIRCUIT MODEL

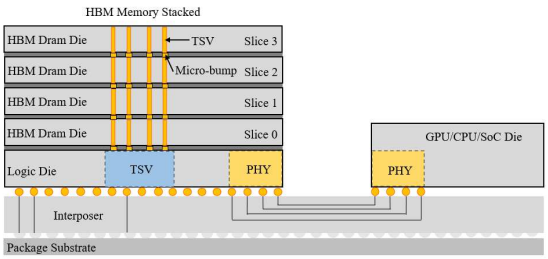


Fig. 1. Concept view of HBM module with stacked TSV structure and micro-bump.

TABLE I. SPECIFICATIONS FOR EACH GENERATION OF HBM

	HBM 1	HBM 2	HBM 2E	HBM3
Clock speed (MHz)	500	1000	1600	3200
Data rate (Gbps)	1	2	3.2	6.4
Bandwidth (GBps)	128	256	410	820
I/O pins	1024	1024	1024	1024
V_{DD} (V)	1.2	1.2	1.2	1.1

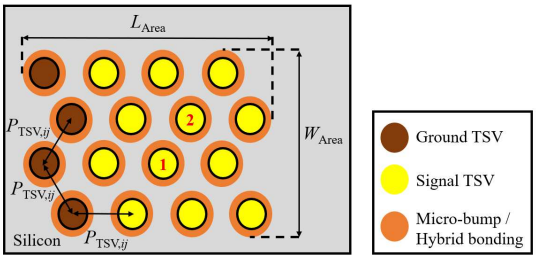


Fig. 2. A top view of the 4×4 TSV array.

A 4×4 model is constructed based on standards and process limits, as shown in Fig. 2 [2]. The model comprises four ground TSVs positioned at the outer edge, while the remaining TSVs are signal TSVs. Among the signal TSVs, two central ones are chosen as targets 1 and 2. The detailed structure and equivalent circuits of the micro-bump and hybrid bonding are introduced in the following section.

In Fig. 3(a), the detailed structure diagram of the micro-bump and TSV is shown. It consists of three parts, inter-metal dielectric (IMD), silicon substrate, and insulator. The IMD layer and insulator are assumed to be silicon dioxide (SiO_2). The micro-bump is located in the underfill layer, which is assigned to be epoxy silicone. The parameters for each layer are presented in Table II. Fig. 4(a) illustrates the equivalent circuit of the micro-bump model. In [6], the multiarray TSV equivalent circuit model is demonstrated under multi-ground conditions. According to the multiconductor transmission line (MTL) model, the equivalent inductance matrix, $\boldsymbol{L_{eq}}$, can

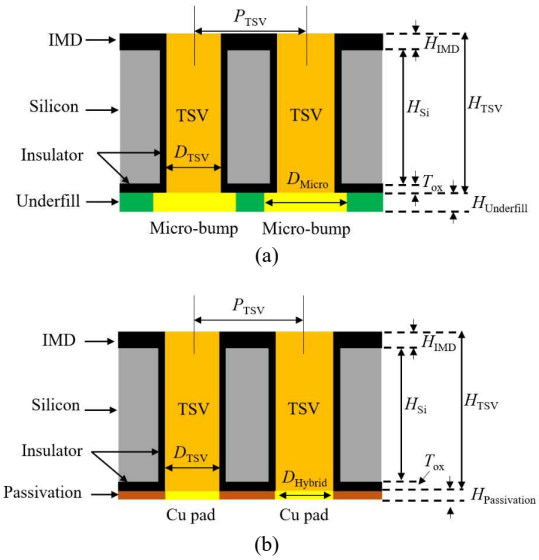


Fig. 3. Structure diagram of TSV with (a) micro-bump and (b) hybrid bonding.

TABLE II. PHYSICAL DIMENSIONS OF MICRO-BUMP AND HYBRID BONDING MODEL

	Micro-bump	**Hybrid bonding**
P_{TSV}	30 μm	10 μm
D_{TSV}	5 μm	
H_{IMD}	5 μm	
T_{ox}	1 μm	
H_{Si}	30 μm	
D_{Micro} / D_{Hybrid}	15 μm	7 μm
H_{Und} / H_{Pas}	10 μm	0.17 μm

be calculated with the ground voltage zero. The capacitance and conductance matrix of the coupling substrate, $\boldsymbol{C}_{Si}$, and $\boldsymbol{G}_{Si}$, can be calculated from the effective inductance by utilizing the property of a homogeneous medium. Considering the cross-section area of the micro-bump is larger than that of TSV, the bump-to-silicon substrate capacitance, $C_{Bump,\,top}$ and $C_{Bump,\,bot}$, is calculated using a parallel-plate capacitor model method as follows [3]:

$$C_{Bump,\,top} = \varepsilon_0 \varepsilon_{Si} \frac{\pi\left[\left(D_{Micro}/2\right)^2 - \left(D_{TSV}/2 + T_{ox}\right)^2\right]}{H_{IMD}} \quad (1)$$

$$C_{Bump,\,bot} = \varepsilon_0 \varepsilon_{Si} \frac{\pi\left[\left(D_{Micro}/2\right)^2 - \left(D_{TSV}/2 + T_{ox}\right)^2\right]}{T_{ox}} \quad (2)$$

The only difference between (1) and (2) is the thickness of the insulator, H_{IMD}, and T_{ox}, sandwiched between the bump and silicon substrate. After establishing the circuit model of 4×4 TSV array with micro-bump, Fig. 5 (a) shows the return loss (RL) and insertion loss (IL) of TSV #1. The *S*-parameters behaviors exhibit a good match up to 15 GHz between the full-wave simulation and circuit model.

Next, the TSV with the hybrid bonding structure is depicted in Fig 3(b), the corresponding variables are listed in Table II. Compared to the previous model, the critical difference lies in the bonding structure, and the material of the passivation layer is assigned to be SiO_2. Fig. 4(b) illustrates the equivalent circuit model of the hybrid bonding, the part related to TSVs is similar to the previous model. The notable

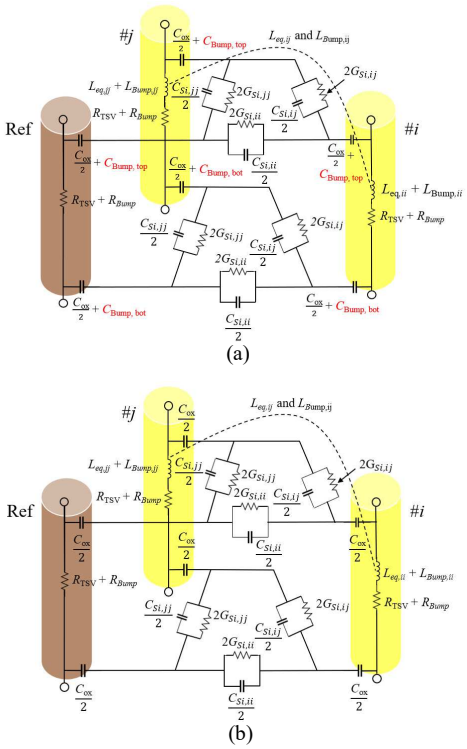


Fig. 4. The equivalent circuit of (a) micro-bump and (b) hybrid bonding.

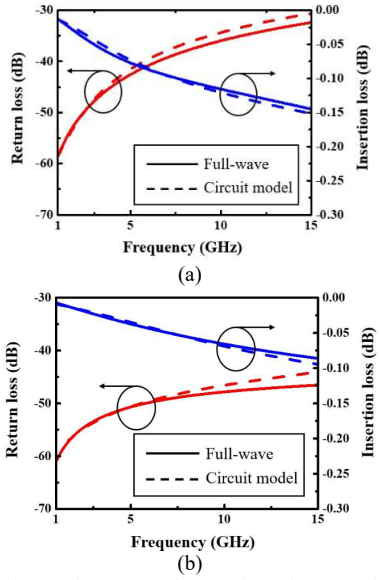


Fig. 5. Verification of the proposed equivalent circuit model of TSV with (a) micro-bump and (b) hybrid bonding at a single DRAM layer.

difference is the exclusion of the C_{Bump} due to the identicalness in the cross-section area between the Cu pad and the TSV. This factor influences the PPA metrics in the subsequent comparison. The 4×4 TSV array with hybrid bonding is also established. Fig. 5(b) shows that the proposed equivalent circuit model and the full-wave simulation of TSV #1 with hybrid bonding are consistent up to 15 GHz. These established models are used to calculate and compare the PPA metrics in the following sections.

III. COMPARISON OF PPA

In this section, the PPA metrics of the micro-bump and hybrid bonding are built and utilized as compared reference. The comparison focuses on dynamic power consumption, the frequency and time domain performance, and the TSV area.

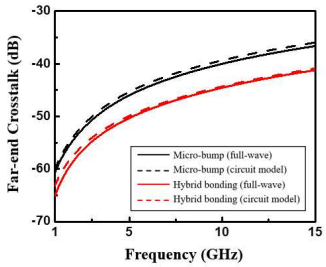
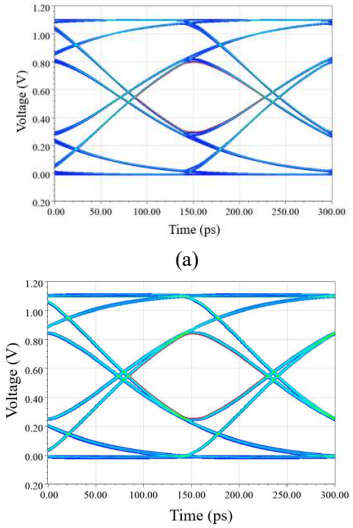


Fig. 6. Far-end crosstalk of the micro-bump and hybrid bonding at a single DRAM layer.



(a)

(b)

Fig. 7. Eye diagram of (a) micro-bump and (b) hybrid bonding at a data rate of 6.4 Gbps in HBM3.

A. Power

The formula to calculate the dynamic power consumption of TSV is based on [6] as follows:

$$Power = AF \cdot C_{TSV} \cdot V_{DD} \cdot f \tag{3}$$

, where AF is the activity factor, C_{TSV} is calculated as the sum of the capacitance in the circuit model, V_{DD} is the operating voltage, and f is the clock frequency of HBM3, as shown in Table I. The C_{TSV} of the hybrid bonding is smaller than that of the micro-bump due to its structural characteristics and shorter length. Therefore, after calculations, a 16.7% reduction in power consumption for hybrid bonding compared to micro-bumps, as shown in Table III.

B. Performance

In this work, the SI performance of the micro-bump and hybrid bonding is analyzed in the frequency and time domain. In the frequency domain, the comparison results of the RL and IL for both two methods are depicted in Fig. 5. At 6.4 GHz, the RL and IL of the hybrid bonding and micro-bump are −45.57 dB, −41.49 dB, and −0.048 dB, −0.089 dB, respectively. It is evident that the former performs better than the latter. This is because the length of the hybrid bonding and the discontinuity are much smaller than the micro-bump. Moreover, the simulated results of FEXT between TSV #1 and TSV #2 are shown in Fig. 6. Compared to the micro-bump, the FEXT of the hybrid bonding is decreased from −45.7 dB to −55.39 dB at 6.4 GHz due to the ground TSV being closer to the signal TSVs and the shorter interconnect length.

TABLE III. PPA COMPARISON OF THE MICRO-BUMP AND HYBRID BONDING

	Micro-bump	**Hybrid bonding**
Eye height (V)	0.48	0.58
Power (μW)	173.06	144.21
Area (μm^2)	11160	1386

As for the time domain simulation, the eye diagram of the 12-layer HBM is simulated by cascading the *S*-parameter of the single layer. The data rate is set to 6.4 Gbps. The simulated eye diagrams of micro-bump and hybrid bonding are shown in Fig. 7. The eye height of hybrid bonding is increased from 0.48 to 0.58 V by comparing with micro-bump, as shown in Table III. Hence, the hybrid bonding technique presents a significant improvement in SI performance in both the frequency and time domains.

C. Area

In Fig. 2, the L_{Area} and W_{Area} represent the length and width of the 4×4 TSV array area, including TSVs and either the micro-bumps or hybrid bonding. Table III demonstrates that the hybrid bonding exhibits a significant 87% reduction in the area compared to the micro-bump, indicating a remarkable improvement. It is increasingly important to minimize TSV occupied areas as it allows for freeing up space for other functionalities or cost reduction.

IV. CONCLUSION

In this paper, the equivalent circuit of a 4×4 TSV circuit model for micro-bump and hybrid bonding is constructed and utilized to compare PPA. The results show hybrid bonding exhibits lower dynamic power consumption, better SI performance, and a remarkably smaller TSV area than micro-bumps. These improvements become increasingly significant due to HBM plans to be extended to 2048 I/O and stacked to 16 layers. Therefore, it is expected that hybrid bonding will be increasingly adopted as a substitute for micro-bumps in HBM architectures.

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