Broadband Launcher-in-Package using HDI Substrate for Radar Applications

Nikita Mahjabeen, Robert Wenzel, Tingdong Zhou
NXP Semiconductors, Austin, TX
nikita.mahjabeen@nxp.com

***Abstract*— In this paper, a wideband launcher-in-package is proposed for FOWLP or FCCSP package mounted on a HDI substrate in radar applications. A differential stripline to rectangular waveguide transition has been shown using a conductor backed patch antenna. The new hybrid solution in 2023 Ansys HFSS has been explored where both modal and terminal wave port was combined in one solution. The simulated results show wideband performance from 71.2 GHz to 88.8 GHz. A 20 dB return loss and 0.74 dB insertion loss was obtained at 77 GHz.**

Keywords— Automotive radar, antenna, chip scale package, differential, flip chip, substrates, transmission, transition, wideband, wafer level package.

I. Introduction

Fan-out wafer-level package (FO-WLP) and flip-chip chip-scale package (FC-CSP) technologies are widely used in radar applications [1]. The flip chip assembly of the die makes these technologies suitable to utilize and integrate other components for heterogenous chip integration [2]. Due to high signal loss in BGA transitions and PCB routing, the waveguide RF connectors are a favorable low loss option. Launcher-in-package (LiP) technology [3] uses an antenna-like patch to launch the signal from transmission lines into the waveguide. To minimize the die size and cost, the launcher is designed on the package substrate.

In this paper, a LiP design has been explored using a chip-scale package combined with a high density interconnect (HDI) substrate [4]. This provides a cost effective solution as a hybrid of PCB and chip-scale package substrates. The HDI substrate uses finer line widths and spacing values than a typical PCB by using advanced fabrication process. Thus the HDI acts as an effective interposer having feature sizes that provide a good bridge between the chip-scale package substrate and the PCB.

This LiP design had been optimized for 77 GHz. Transition is made from differential stripline to rectangular waveguide using a slot fed patch similar to the patent in [3], but using a different design of the patch with optimized positioning. In the literature, many different transitions from single ended planar transmission line to rectangular waveguide have been developed for LiP [5]. One of the primary issues had been achieving a wide-enough band to allow for manufacturing tolerances and assembly variation. Ridged waveguide solutions have been proposed [6] but carry the downside of increased cost. We have studied the position of the patch and dimensions to achieve wideband response and have attempted to reduce sensitivity to the variations. Tolerance study was conducted to understand the feasibility of the LiP design. Additionally, the new released terminal solution in 2023 Ansys HFSS version have been explored for comparative analysis.

II. Launcher-in-Package

A. HDI Substrate Stackup

A 6-layer HDI substrate has been used to design the LiP as shown in Fig. 1. The thickness of the layers are chosen to vary between 50 µm and 100 µm, with 18 µm copper thickness. Low-loss dielectric materials were chosen for the HDI substrate. The minimum feature size for the line width and spacing is limited to 50 um. Conventional HDI typical dimensions were used in the design based on IPC-2226A standard [7].

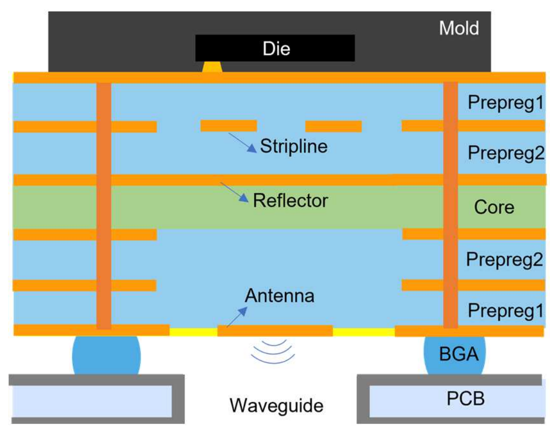

Fig. 1. Cross-section of the launcher-in-package where the signal from stripline in substrate is transitioned to rectangular waveguide in PCB using a patch antenna on substrate.

B. Transition Design

The top three layers (M1 to M3) were used for the RF differential coplanar striplines. The third layer, M3, was used as dual purpose: ground for the stripline, and back-reflector for the antenna patch. The cavity-backed patch antenna, which acts as a launcher, has been placed on the sixth layer (M6) by maintaining $\lambda g/8$ distance from the reflector and forming a waveguide cavity in the dielectric [8]. The cavity is surrounded by ground vias as shown in the top view of the LiP included in Fig. 2. The signal from the patch is launched into the custom waveguide (WG) on PCB [9]. It then propagates through the WR10 external waveguide screwed onto the PCB as shown in Fig. 3.

The stripline was designed for 100 ohm differential impedance and the signal vias were designed as conical instead of cylindrical shape to consider the actual shape of laser vias. The slot fed patch was optimized for the desired performance.

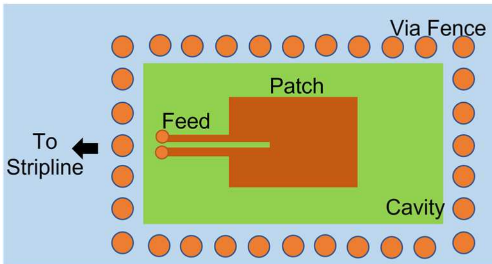

Fig. 2. Top view of the LiP in HDI substrate where the stripline in M2 layer is connected to the antenna in M6 layer. The cavity is surrounded by via walls.

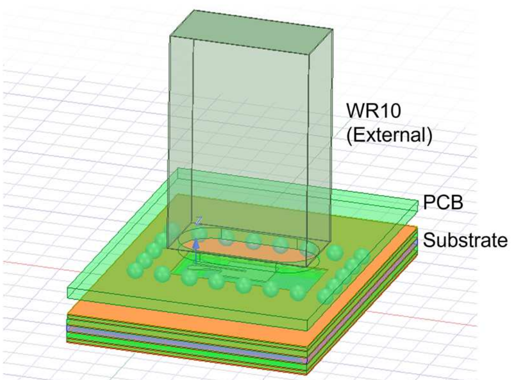

Fig. 3. 3D view in Ansys HFSS of the LiP design where the signal is launched by the antenna on HDI substrate through the custom waveguide on PCB towards the WR10 external waveguide.

C. S Parameter Performance

The LiP was designed and simulated in Ansys HFSS 3D EM tool. A modal solution with wave port excitation was set for both ports. Two modes were excited in Port 1 for the differential pair. The electric field in the port was observed to determine the differential and common modes. Port 2 was set at the top of metal waveguide where an integration line was defined for a single mode. An interpolating frequency sweep from 70 GHz to 90 GHz with 401 points was used for simulation.

Fig. 4 shows the S-parameter performance of the LiP. The |S11| is represented by the dashed line for the differential pair. The |S22| is represented by the dotted line for the waveguide. A wideband 17.6 GHz 10 dB response has been achieved from 71.2 GHz to 88.8 GHz. The return loss is 20 dB and the insertion loss is 0.74 dB at 77 GHz.

Based on the variation of the position of the patch in the cavity, the S-parameter performance can vary which is shown in Fig. 5. When the patch is not centered nor optimized, a narrowband 10 dB performance is achieved from 71.2 GHz to 77 GHz. When the patch is centered and the width is optimized, a very wideband performance is achieved from 71.2 GHz to 88.8 GHz. This study shows that the patch needs to be placed in the center relative to the walls of the cavity and the width needs to be optimized for the wide bandwidth.

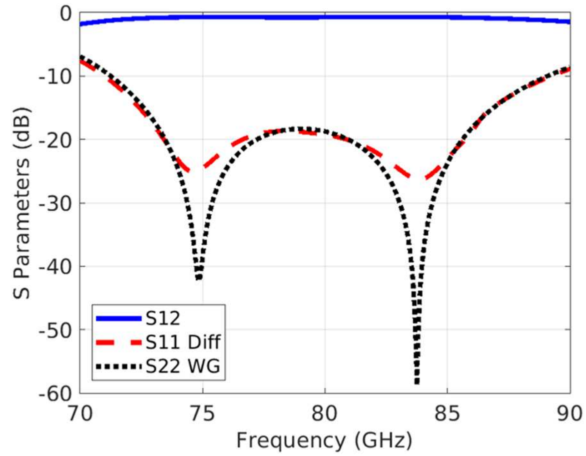

Fig. 4. Wideband S-parameter performance of the LiP from 70-90 GHz where Port 1 is the differential stripline in HDI substrate and Port 2 is the WR10 waveguide.

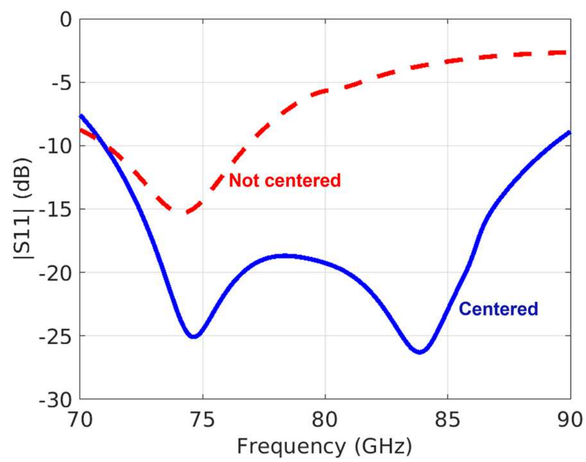

Fig. 5. S-parameter performance for the variation of the patch position.

A tolerance study was conducted for the dielectric thickness, copper thickness, line width, patch and slot dimensions as independent parameters. It was observed that the performance was most sensitive to the substrate thickness and the slot width. A shift in frequency by ±0.5 GHz was observed for ±10 µm variation in slot width, and the return loss varied in performance by ± 10 dB. A shift in frequency by ±1 GHz with ± 5 dB variation in return loss was observed for ±10 µm variation in dielectric thickness. This means a ±20 µm dielectric thickness variation (which is typical of HDI) can deteriorate the return loss to worse than 10 dB. Thus fabrication process improvement for tighter tolerance is key to this low cost solution.

D. *Modal vs Terminal Solution*

In general, Ansys HFSS has two types of solution. One is terminal and the other is modal. Traditionally terminal solution supports differential S-parameters [10] and modal solution is used for field-based transmission lines.

In the previous years, terminal and modal wave port were only possible as separate solutions. To consider both terminal and modal port in one solution, the 2023 Ansys HFSS version has introduced a hybrid port definition under terminal solution. To evaluate the differences, two cases are introduced. In Case 1 terminal solution is applied, where terminal wave port for differential stripline and modal wave port for rectangular waveguide was used. In Case2, modal solution was explored, where modal wave port was used for both differential stripline and rectangular waveguide. Two modes were introduced in the differential line to consider the differential and common mode.

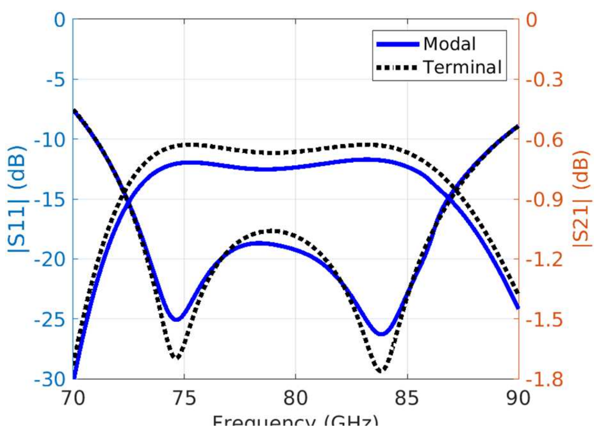

Fig. 6. Comparative analysis of the S-parameters for modal vs terminal solution of the differntial stripline in Ansys HFSS.

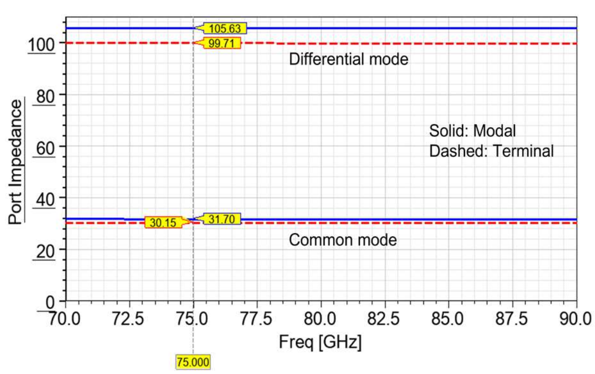

Fig. 7. Comparative analysis of the port impedance for modal vs terminal solution of the differntial stripline in Ansys HFSS.

Differences in the S-parameter response were observed for terminal vs modal solution as shown in Fig. 6. The modal solution shows 0.08 dB higher insertion loss (|S21|) than the terminal solution represented by solid and dotted line, respectively. Modal solution supports all modes whereas terminal supports only TEM [9]. This means that for modal solution, the additional modes between the signal and ground has been considered which accounts for the additional loss.

To further explore, the differential and common impedance of the differential lines was analyzed for both cases. This is shown in Fig. 7 which shows the comparative impedance analysis of the differential lines for modal and terminal solution. The differential impedance is observed to be 99.71 ohm for terminal and 105.63 ohm for modal solution at 75 GHz. The modal impedance is dependent on the port geometry unlike for terminal [9] which contributed to the difference.

III. Conclusion

In this paper, an automotive launcher-in-package (LiP) design has been presented using a hybrid chip-scale and HDI substrate package. A wideband performance has been achieved by centering the patch relative to the edge of the cavity and optimizing the patch geometry. In high frequency solution, modal solution is a better alternative to terminal solution to consider multimode propagation. One of the key challenges to achieve good electrical performance is to control manufacturing tolerance.

Acknowledgment

We would like to thank other colleagues in NXP Semiconductors for their collaboration and continued effort.

References

[1] T. Tang, B. -S. Fang, D. Ho, B. H. Ma, J. Tsai and Y. -P. Wang, "Innovative Flip Chip Package Solutions for Automotive Applications," 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 2019.

[2] M. J. Kim et al., "Novel 2.5D RDL Interposer Packaging: A Key Enabler for the New Era of Heterogenous Chip Integration," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 321-32.

[3] G. Carluccio, M. B. Vincent, M. Spella, A. J. M. de Graauw, and H. T. Shivamurthy, ‘‘Package,’’ U.S. Patent 0 231 408 A1, Jul. 21, 2022. [Online].

[4] A. Lamminen, J. Säily, J. Ala-Laurinaho, J. de Cos, and V. Ermolov, “Patch antenna and antenna array on multilayer high-frequency PCB for D-band,” IEEE Open J. Antennas Propag., vol. 1, pp. 396-403, 2020.

[5] Q. Ren et al., "Gapwaveguide Automotive Imaging Radar Antenna With Launcher in Package Technology," in IEEE Access, vol. 11, pp. 37483-37493, 2023.

[6] Y. Shi et al., "Novel W -Band LTCC Transition From Microstrip Line to Ridge Gap Waveguide and its Application in 77/79 GHz Antenna Array," in IEEE Transactions on Antennas and Propagation, vol. 67, no. 2, pp. 915-924, Feb. 2019.

[7] “Sectional Design Standard for High Density Interconnect (HDI) Printed Boards IPC-2226A”, IPC International, Inc.

[8] Kyutae Lim, A. Obatoyinbo, M. Davis, J. Laskar and R. Tummala, "Development of planar antennas in multi-layer packages for RF-system-on-a-package applications," IEEE 10th Topical Meeting on Electrical Performance of Electronic Packaging (Cat. No. 01TH8565), Cambridge, MA, USA, 2001, pp. 101-104.

[9] J. S. Häseker and M. Schneider, ‘‘90 degree microstrip to rectangular dielectric waveguide transition in the W-band,’’ *IEEE Microw. Wireless Compon. Lett*., vol. 26, no. 6, pp. 416–418, Jun. 2016.

[10] *Ansys Manual on HFSS Lumped vs Wave Port Basics (2020)* Accessed: July 12, 2023. [Online]. Available: https://courses.ansys.com/wp-content/uploads/2021/07/HFSS_GS_2020R2_EN_LE6_Port_Basics.pdf