Robust and Efficient Design of On-Chip Compact Delay Units Based on Bridged T-Coil

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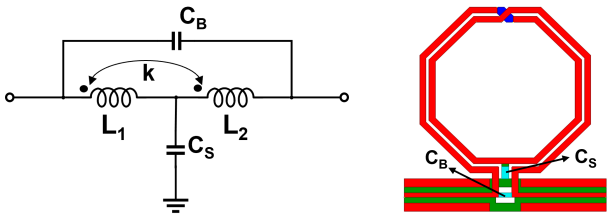
***Abstract*—This paper presents a robust and efficient design methodology for on-chip compact delay units using the bridged T-coil (BTC). This layout design methodology reduces circuit complexity by realizing the BTC with a center-tapped return path close to the input and output ports. Further, coupled inductor designs with a rotationally adjustable inductor layout and a modified differential layout enable wider control of positive and negative magnetic coupling coefficient while keeping layouts compact. The new design methodology provides single-pass layout designs for delay units with BTCs. The design methodology is demonstrate in a Tower Semiconductor 0.18µm SiGe BiCMOS process with fullwave electromagnetic simulations for singled-ended and differential BTC designs with lowpass delay characteristics and cascaded BTCs with flat bandpass group and phase delay characteristics.**

***Index Terms*—true time delay, on-chip delay unit, bridged-T coil, compact layout design**

I. Introduction

True time delay (TTD) units are widely used components in many signal processing and RF applications, including time-to-digital converters, signal path delay compensation, and beamforming in phased-array antennas. Numerous studies have been done for the design and implementation of time delay units. Some researchers have also leveraged the inherent time delay property to construct phase shifters, but sacrificing the group delay stability [1]. Others have pursued designs utilizing off-chip structures [2], while some have employed active devices within the delay lines [3]. However, the preservation of signal integrity for time delay of a compact on-chip TTD unit necessitates further refinement and research. On the other hand, the design complexity and stability challenges associated with on-chip TTD implementations have prevented widespread industrial application. Consequently, the availability of an efficient and robust design methodology for TTD units has gained significant importance.

To facilitate the implementation of on-chip TTD designs, we utilize the well-known bridged T-coil (BTC) circuit, as illustrated in Fig. 1(a). The major challenge in the implementation of a BTC is the ability to control the magnetic coupling coefficient (k). Differential inductor layouts are commonly employed in on-chip BTC designs due to their compact size and widespread availability in semiconductor processes. However, the control parameters for varying inductance and coupling coefficient of these differential inductors are limited to dimensions and conductor spacing. Typically, the achievable range for k is between 0.4 and 0.8, depending on the process technology.



(a) (b)

Fig. 1: (a) Bridged T-coil circuit. (b) Layout of center-tapped return path close to the input and output ports to reduce inductive parasitics.

We demonstrate the robustness of our new design approach for single-ended and differential delay units with lowpass delay response, and a cascaded BTC unit for 150 ps TTD over the Ku-band (12-18 GHz). All delay units are designed in the Tower Semiconductor 0.18µm SiGe BiCMOS process [4], and full-wave electromagnetic simulations are done in HFSS [5].

II. Design Methodology

Figure 1(b) shows the implemented layout of a BTC using the differential inductor topology. By center tapping the C_S path close to the signal input and output paths, we effectively eliminate the uncertainty and complexity associated with using a ground ring as part of the return path (as in [6]). Here, we have adapted the magnetic flux cancellation technique introduced in [7] into the BTC design to overcome the limitation of realizing small or negative k values with the standard differential inductor topology. We also introduce (i) the Rotationally Adjustable Inductor Layout (RAIL) in which both inductors are rotated with respect to the center tap position to achieve small positive and negative k values, as illustrated in Fig. 2(a), and (ii) the modified differential inductor layout in Fig. 2(b) for BTCs requiring $k < 0$ values.

Our new layout designs enable short connections with negligible parasitics between the BTC and the main line, providing single-pass layout designs that can be readily inserted at any point along the main line, as illustrated in Fig. 3.

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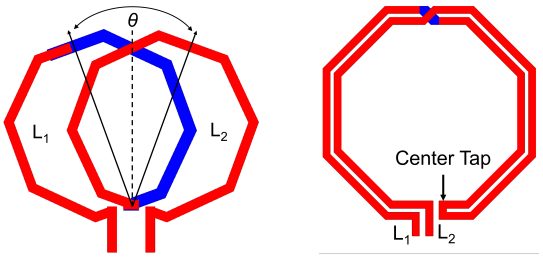


(a) (b)

Fig. 2: (a) Illustration of RAIL. L_1 and L_2 refer to the inductors shown in Fig. 1(a); magnetic coupling coefficient k adjusted with rotation angle θ. (b) Layout of modified differential inductor for negative k values.

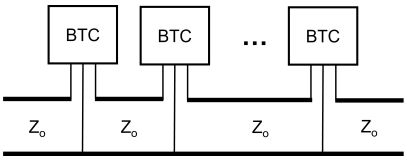


Fig. 3: BTCs inserted along a transmission line.

III. TTD Unit Design and Results

To design a TTD unit based on the BTC, it is necessary to establish constraints for both group delay and phase delay in order to ensure accurate TTD performance. The determination of phase delay, τ_{pd}, and group delay, τ_{gd}, can be accomplished through the utilization of the following equations [8]:

$$\tau_{\text{pd}} = -\frac{\angle(S_{21}(\omega))}{\omega} \quad (1) \qquad \tau_{\text{gd}} = -\frac{d(\angle(S_{21}(\omega)))}{d\omega} \quad (2)$$

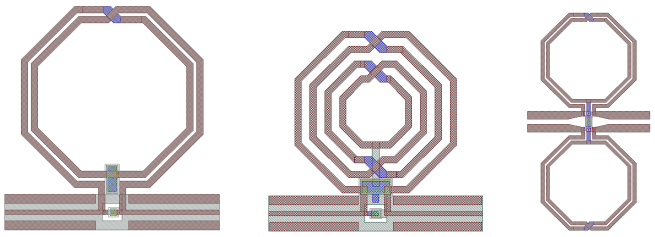
A. Lowpass TTD Unit Design

For an ideal delay unit, scattering parameter S_{21} is an exponential transfer function ($e^{-s\tau}$). To realize a maximally flat time delay response over a finite bandwidth with a BTC, a second-order Padé approximation of the exponential transfer function is employed as given by (3) [9].

$$S_{21} = e^{-s\tau} \approx \frac{1 - \frac{\tau}{2}s + \frac{\tau^2}{12}s^2}{1 + \frac{\tau}{2}s + \frac{\tau^2}{12}s^2} \quad (3)$$

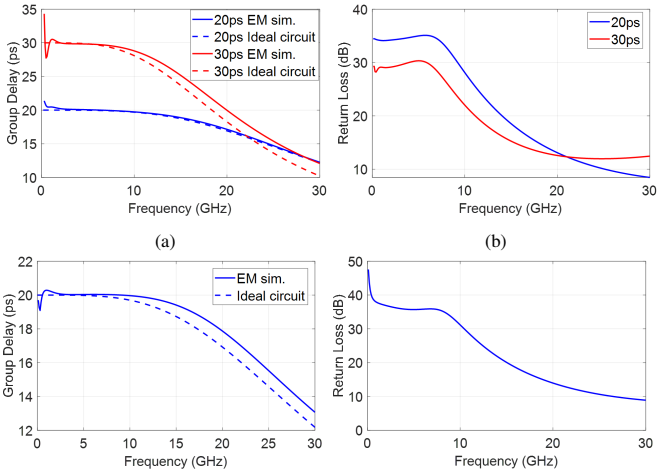
Here, τ is the time delay. The BTC circuit elements can readily be determined using the even-odd mode analysis technique ([10],[6]). The circuit element values of the BTC circuit shown in Fig. 1(a) can then be expressed in terms of delay time τ and system impedance Z_0 (see e.g. [6]).

Figure 4(a) shows the layout of a 20 ps single-ended TTD unit realized by a two-turn differential inductor structure. The electromagnetic (EM) simulation results for group delay and return loss are shown by the blue curves in Figs. 5(a)-(b), respectively. For the 30 ps TTD unit implementation, a four-turn differential inductor structure is employed due to the higher inductance requirement. The corresponding EM simulation results are shown by the red curves in Figs. 5(a)-(b), respectively. Figure 4(c) shows the layout of a differential TTD unit with 20 ps delay response. The structure is configured as a four-port network with 100 Ω differential line impedance. The EM simulation results for group delay and return loss are shown in Figs. 5(c)-(d), respectively, and compared to circuit simulations with ideal circuit components and implemented in Advanced Design System (ADS) [11].



(a) (b) (c)

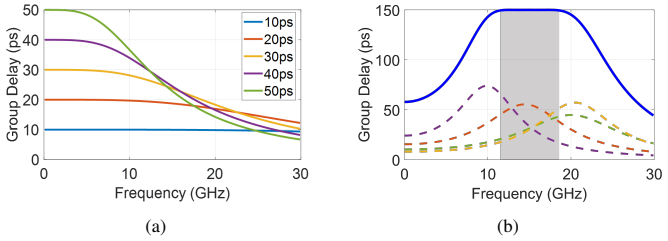
Fig. 4: Layout of three lowpass TTD unit designs: (a) 20 ps TTD, 2-turn center-tapped differential inductor; (b) 30 ps TTD, 4-turn center-tapped differential inductor; (c) Differential TTD with 20 ps delay.



(a) (b) (c) (d)

Fig. 5: Fullwave electromagnetic simulation results: Single-ended BTCs (20 ps design shown in blue, 30 ps design shown in red): (a) group delay, (b) return loss. Differential TTD unit with 20 ps delay: (c) group delay; (d) return loss.

B. Bandpass TTD Unit Design



(a) (b)

Fig. 6: Time delay responses: (a) lowpass time delay responses for different fixed time delays; (b) illustration of synthesized flat bandpass time delay response (blue curve) with four BTCs each with a peaked time delay response (dashed curves).

When realizing larger time delays with a single lowpass BTC cell, the effective bandwidth with flat group delay is reduced by a factor approximately inversely proportional to time delay, as illustrated in Fig. 6(a). To address this limitation, multiple lowpass BCT cells, each with a small time delay but of sufficiently large bandwidth, can be cascaded. A common alternative technique for synthesizing a given group delay within a bandpass region is to cascade a smaller number of

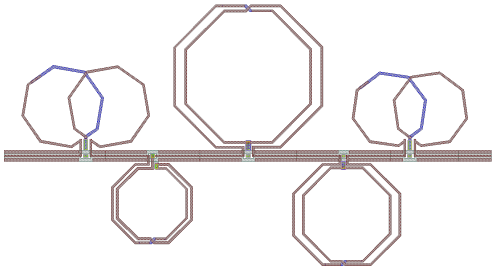


Fig. 7: Layout of a 150 ps bandpass TTD unit using five cascaded cells. The overall dimensions are $1,100\mu$m $\times 630\mu$m.

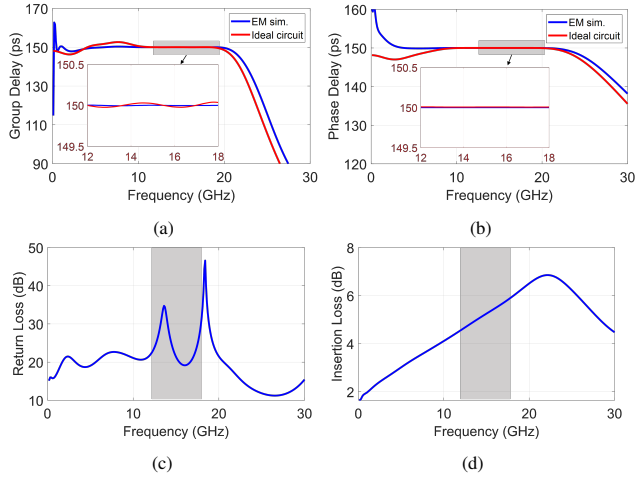


Fig. 8: Fullwave electromagnetic simulation results for 150 ps bandpass TTD design: (a) group delay, (b) phase delay, (c) return loss. (d) insertion loss.

allpass networks each with a peaked group delay response. Figure 6(b) illustrates the synthesis of a bandpass group delay response cascading four BTC cells with the shown different peaked group delay profiles to achieve a 150 ps group delay within the frequency range of 12 GHz to 18 GHz. Alternatively, to achieve the same group delay and frequency range using a lowpass topology, a total of 15 BTC cells, each with a 10 ps delay, would need to be cascaded.

For the peaked time delay response, the second-order BTC transfer function can be expressed as [8]

$$S_{21} = \frac{s^2 - \frac{\omega_r}{Q}s + \omega_r^2}{s^2 + \frac{\omega_r}{Q}s + \omega_r^2} \tag{4}$$

where ω_r is the pole resonant frequency in radians per second and Q is the pole quality factor. Substituting (4) into (1) and (2), the peaked time delay response is obtained as

$$\tau_{\text{pd}} = 2\tan^{-1}\left(\frac{\frac{\omega\omega_r}{Q}}{\omega_r^2 - \omega^2}\right) \quad (5) \qquad \tau_{\text{gd}} = \frac{2Q\omega_r(\omega^2 + \omega_r^2)}{Q^2(\omega^2 - \omega_r^2)^2 + \omega^2\omega_r^2} \quad (6)$$

A TTD design requires both a constant group delay τ_{gd} and a constant and equal phase delay τ_{pd} within the frequency band of interest. This imposes additional constraints on the synthesis algorithm and usually requires slightly more cascaded cells compared to when only the group delay response is synthesized. Once the values of ω_r and Q have been determined for each cell via (5) and (6), the corresponding BTC circuit elements k, L, C_B, and C_S can be found from [8].

A bandpass TTD unit was designed in a Tower Semiconductor 0.18μm SiGe BiCMOS process [4] for a flat group and phase delay of 150 ps across the frequency range of 12 GHz to 18 GHz. The layout of the design is shown in Fig. 7. The design was implemented as a cascade of five BTC cells. The ω_r and Q values of each BTC cell were determined simultaneously with a fast customized optimization algorithm. The respective k values for the BTC cells, depicted from left to right in Fig. 7, are 0.078, -0.571, 0.470, 0.471, and 0.085. By the fullwave electromagnetic simulation results as shown in Fig. 8, the bandpass TTD design achieves excellent flatness in group and phase delay while the insertion loss is less than 6 dB and the return loss better than 18 dB within the Ku-band.

IV. Conclusion

This paper presented a robust design methodology for on-chip lowpass and bandpass delay units using single and cascaded BTC cells. By moving the center tap close to the signal input and output, the BTCs can accurately be designed and efficiently be tapped into the main transmission line. The presented methodology significantly reduces the design complexity of BTC based delay units. Moreover, the modified differential inductor layout and the coupled magnetic flux management in the RAIL topology enable the compact realization of a wide range of magnetic coupling coefficient values. The proposed design methodology has broad applicability and exhibits high accuracy and simplicity in the design of on-chip delay units.

Acknowledgment

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References

[1] E. V. P. Anjos, D. M. M.-P. Schreurs, et al., "A 14–50-GHz phase shifter with all-pass networks for 5G mobile applications," *IEEE Trans. Microwave Theory Techn.*, vol. 68, no. 2, pp. 762–774, 2020.

[2] M. Jasinski, L. Yang, et al., "RF multi-functional input-reflectionless dispersive-delay structure with sharp-rejection filtering using channelization techniques," *IEEE Trans. Circuits Systems II : Express Briefs*, vol. 70, no. 4, pp. 1410–1414, 2023.

[3] D. Hao, W. Zhang, et al., "A low insertion loss variation trombone true time delay in GaAs pHEMT monolithic microwave integrated circuit," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 7, pp. 889–892, 2021.

[4] Tower Semiconductor, website: https://towersemi.com/.

[5] *HFSS*. (2022R2). ANSYS. [Online]. Available: https://www.ansys.com/products/electronics/ansys-hfss.

[6] S. R. Mahendra and A. Weisshaar, "A compact and broadband on-chip delay line design based on the bridged T-coil," in Proc. IEEE 25th Workshop on Signal and Power Integrity (SPI), 2021, pp. 1–4.

[7] X. Dong and A. Weisshaar, "Design of compact integrated lumped-element coupled-resonator filters," in Proc. IEEE 27th Conf. Electr. Perform. Electron. Packag. Syst. (EPEPS), 2018, pp. 289–291.

[8] A. B. Williams and F. J. Taylor, Electronic filter design handbook. McGraw-Hill Education, 2006.

[9] G. H. Golub and C. F. Van Loan, Matrix computations. JHU press, 2013.

[10] D. M. Pozar, Microwave engineering. John Wiley & Sons, 2011.

[11] *PathWave Advanced Design System*. (2022). Keysight Technologies. [Online]. Available: https://www.keysight.com/us/en/home.html.