D-Band Flip-Chip Packaging with Wafer-Level Cu-pillar Bumps

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***Abstract*— The transmission loss of a Cu pillar microstrip-microstrip transition in a flip-chip package is characterized. The used components are fabricated in the back-end layers of a standard BiCMOS process, with Cu pillars deposited on top as the flipped die and UBM coating on pad as the substrate. Four variations with different pitches and openings on the ground plane are all characterized and compared using both measurement and FEM simulation. It is found that a small pitch with a de-coupling aperture are the keys to minimize the transition losses. The de-embedded insertion loss of a single Cu-pillar transition is between 0.3-0.5 dB over 110-170 GHz (D-band). Such a wafer-level bumping approach greatly improves the throughput and uniformity, and meanwhile, demonstrates comparable transition losses with other flip-chip packages using similar sized bumps.**

Keywords—Cu pillar, flip-chip, D-band, microstrip, FEM

I. Introduction

As the transistors approach their physical limits, the research focus starts to shift to the heterogeneous integration towards “More than Moore” technologies. The package solutions for mm-wave applications is, of course, an important aspect to be considered.

The conventional wire bond, although is still under development, is limited by its bandwidth due to the large wire inductance [1][2]. The flip-chip packaging and the fan-out wafer level packaging have both demonstrated outstanding RF capabilities [3-6]. In this study, a Cu pillar bumped flip-chip package is developed and characterized. The advantage of this approach is its small pitch, small bump sizes, and its uniformity as a wafer-level bumping process. All these features are critically advantageous in the mm-wave range, making it a promising packaging solution for applications at D-band and above.

II. Methodology

A. Sample design

Since the targeted band is 110-170 GHz, the substrates used in the flip-chip assembly should be carefully selected to handle the high frequency signals. As a result, the

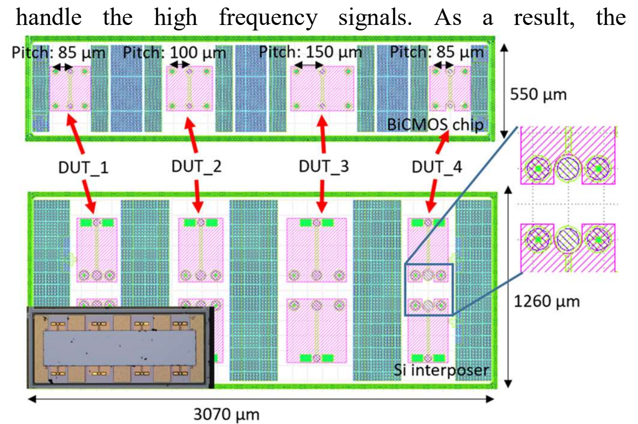

Fig. 1 The flip-chip samples, both the GDS layout and the fabricated test vehicles are shown. There are four variations with different pitches and de-coupling apertures on the ground.

transmission lines are designed in the standard BiCMOS back-end stacks using IHP’s state-of-the-art SG13 BEOL runs. Two dies are flip-chip assembled, one smaller die is used to accommodate Cu pillars, and the other larger die is used as substrate with under-bump-metallization (UBM) coatings on the pads. As is shown in Fig. 1, a microstrip-to-microstrip transition structure is exploited, with four variations for comparison. The first three variations differ in pitch, which ranges from 85 µm to 150 µm, and the last one uses a de-coupling aperture on the ground plane to minimize the parasitic capacitances.

Since the pillars have around 15 µm of SnAg solder cap on top, the flip-chip assembly is implemented using a mass solder reflow process. The die with pillars is first dipped in a tray with flux materials, then flipped and aligned with the Fineplacer Pico bonder. The assembled chips are cleaned with ultra-sonic after the reflow to remove the excessive flux materials and ensure low losses in the D-band.

To enable a direct evaluation of the influences of the Cu pillar transitions, the structure is compared with a plain

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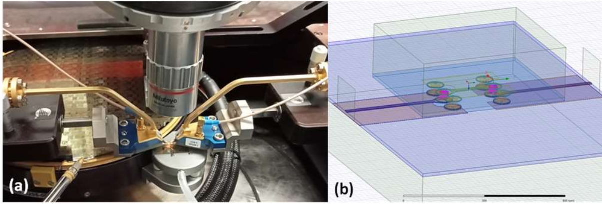

Fig. 2 The measurement and simulation setups. (a) is the D-band on wafer measurement setup, and (b) is the HFSS simulation setup.

microstrip line. With such objective, several microstrips with different lengths are designed and fabricated using the same technology.

B. Simulation setup

The modelling of the Cu pillar transition is implemented in Ansoft HFSS. Such a full-wave solver ensures the accuracy of the modelling, which is especially critical for complex 3D structures working at such high frequencies. The model is fully parametrized to ease the study of different geometry variations. The details of the modelling are illustrated below.

The driven modal is utilized to solve for the S parameters. And considering the wide bandwidth (110 GHz to 170 GHz), discrete solutions are needed to ensure the modelling accuracy over the whole frequency band. Besides, wave ports are directly used on the transmission line without pads to be comparable with de-embedded measurement results. A radiation boundary is assigned in order to minimize the reflected waves. The HFSS model is shown in Fig. 2, together with the measurement setup discussed below.

C. Measurement

The measurement setup is shown in Fig. 3. Rhode & Schwarz ZVA 24 is used together with frequency extenders to measure from 110 GHz to 170 GHz. Since the packaged sample is too small to be fixed on the wafer chuck, it is placed on an auxiliary chuck. Infinity probes with a pitch of 75 µm are used.

Worth noticing that the probe contact is problematic to the UBM coating. The few-micrometer-thick Nickel is too hard for the probes to penetrate, leading to small contact areas. This results in a contact resistance ranging from a few Ohms to tens of Ohms depending on the contact attempt. Two indicators are taken to measure the quality of the contact: 1) the VNA frequency sweeping results should be stable over time, and 2) the S11 and S22 should be similar due to the symmetry of the structures. With these considerations, proper contacts are ensured.

However, even with a proper contact, the contact resistance is still much higher than that on the aluminum pads. To make sure the obtained results are comparable with those in the literature, de-embedding is necessary. A TRL method, which is suitable for the D-band frequencies, is exployed for all the measurements to remove the pad effects since all the pad configurations are the same.

III. RESULTS AND DISCUSSION

The comparisons of measurement and simulation for all four flip-chip structures are shown in Fig. 3. Good matchings

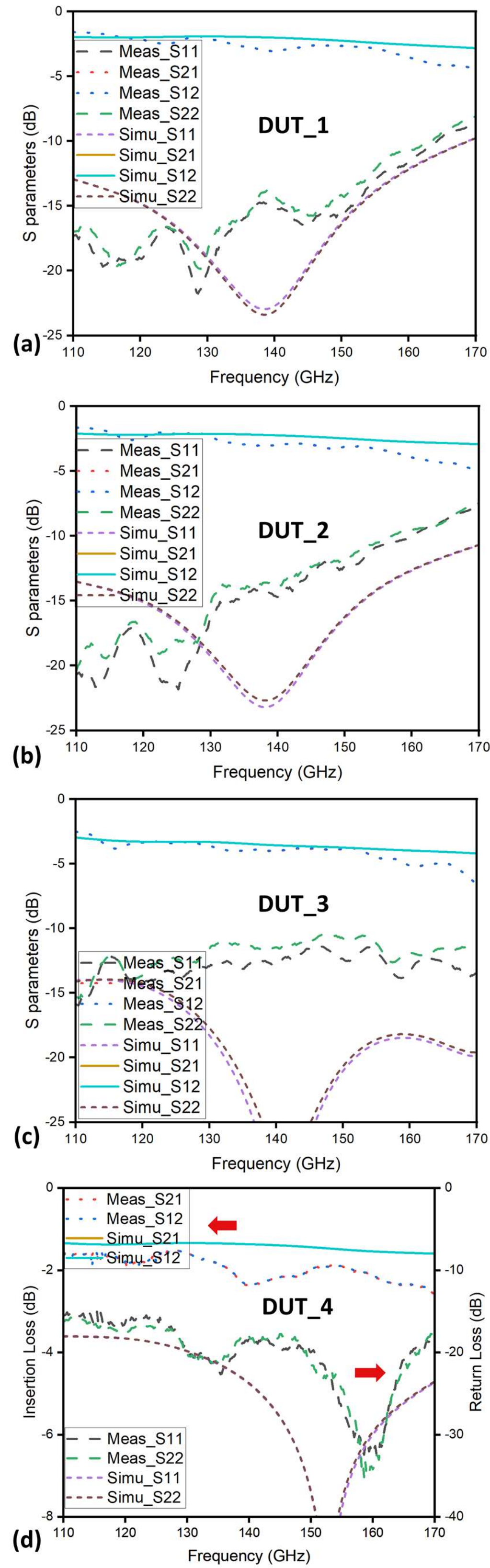

Fig. 3 The comparison between the measurement and simulation results for all four different flip-chip structures. (a), (b), (c), and (d) represent the S parameters of DUT1, 2, 3, and 4 respectively.

Table 1. The comparison of this result to the literatures

	Beer et al. [1]	Monayakul et al. [6]	Sinha et al. [7]	Khan et al. [8]	Lu et al. [9]	This work
Bumping Technology	Gold stud bump	AuSn bump	NA	Gold stud bump	Cu pillar	Cu pillar
Bump size (µm)	50	4	2	50	30	30
Insertion loss per transition	1 dB @ 170 GHz	NA	0.1 dB @ 170 GHz	0.3 dB @ 165 GHz	NA	0.3-0.5 dB @ 170 GHz
Insertion loss total structure	5.5 dB @ 170 GHz (7 mm line)	1.3 dB @ 170 GHz (0.8 mm)	1 dB @ 170 GHz (1.6 mm line)	1.2 dB @ 165 GHz (1.35 mm line)	2 dB @ 100 GHz (0.94 mm line)	2.5 dB @ 170 GHz (0.8 mm)
Transition type	CPW-CPW	STL-CPW	STL-STL	CPW-CPW	CPW-CPW	MS-MS

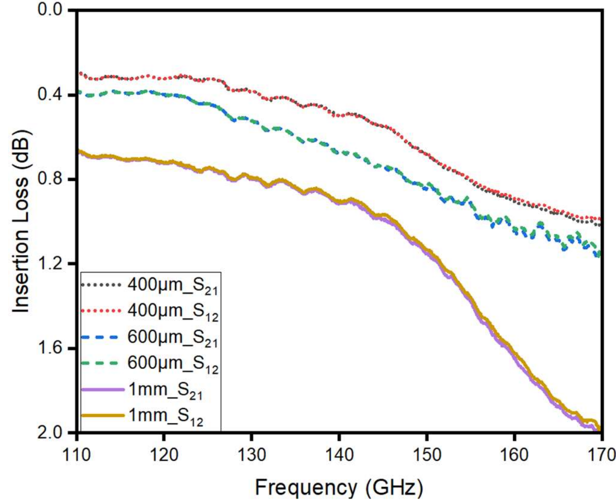

Fig. 4 The de-embedded D-band S parameter measurement of pure microstrip transmission lines with different lengths.

are achieved, validating the modelling setups. It is observed that both the pitch and the de-coupling aperture have big influences on the Cu pillar transition losses. The $|S_{21}|$ at 170 GHz corresponding to the 85 µm, 100 µm, and 150 µm pitches are -4.5 dB, -5 dB, and -6.5 dB respectively. And the DUT_4, which has an opening on the ground for de-coupling, even reduces the loss to -2.5 dB at 170 GHz. Within this context, the critical points in the transition design are the small pitch and de-coupling opening on the ground plane.

Fig. 4 shows the measurement results for the plain transmission lines after de-embedding. Considering that the total length of the flip-chip structure is 800 µm, the corresponding transmission line loss is around 1.6-2 dB at 170 GHz. The extra losses introduced by the Cu pillar transition can, therefore, be extracted by simple subtractions. A loss of 0.3-0.5 dB per Cu pillar transition over the whole D-band is obtained. A brief comparison of the flip-chip transition loss state-of-the-art is done in Table 1, where CPW stands for coplanar-waveguide, MS stands for microstrip, and STL stands for strip line. Worth noticing that Sinha et al. demonstrates a flip-chip transition only 0.1 dB loss at 170 GHz. Such a low loss is mainly attributed to two reasons: 1) an ultra-small 2 µm bump is used to minimize the parasitics, and 2) the presented D-band S-parameter measurement has huge variations (± 0.5 dB), which leads to uncertainties of the extracted per transition loss. To conclude, the extracted 0.3-0.5 dB per transition in this study agrees quite well with other results using similar sized bumps.

IV. Conclusion

In this paper, a Cu pillar flip-chip package is demonstrated with a loss of 0.3-0.5 dB per transition over the whole D-band. Such a low loss agrees well with other results using similar sized bumps, indicating that the Cu pillar flip-chip can be a good alternative for D-band applications in addition to the existing technologies. The wafer-level bumping process also ensures high uniformity and throughput, making it especially suitable to be exploited for mass production of RF applications.

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