Efficient Estimation of Power Supply Induced Jitter via Machine Learning

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***Abstract*—This paper presents an efficient method for the analysis of power supply induced jitter using machine learning techniques in the presence of supply noise for CMOS inverter circuits. In the proposed hybrid approach, knowledge-based neural network and deep belief neural network produce reasonably accurate jitter response while providing an efficient training using training data extracted from both analytical models as well as a circuit simulator. The proposed model can also handle varying inputs without re-training the network's parameters.**

***Index Terms*—Deep belief neural networks, knowledge-based neural networks, power supply induced jitter.**

I. Introduction

Even with the most recent developments in VLSI technology, the performance and quality of the system are significantly affected by the power supply noise which is a major contributor of producing timing jitter in high-speed high-density digital circuits. Jitter becomes very critical when power supply is shared with many IPs, making it harder to achieve the desired timing budgets. Hence, ensuring signal and power integrity to meet the desired timing budgets have become very challenging for modern electrical circuits.

For jitter estimation, traditional approaches require simulation of large number of bits that can make the process prohibitively CPU expensive. In order to address the computational burden, several efficient models can be found in the literature [1]-[4]. Efficient semi-analytical methods for determining PSIJ for current mode and voltage mode drivers are introduced in [1] and [2], respectively. In [3], power supply induced jitter is obtained in the presence of transmission media as well as ground bounce noise for voltage mode driver circuits. Recently, device parameter-based model for PSIJ analysis is proposed in [4].

Computer-aided design (CAD) approaches based on neural networks have been introduced for signal and power integrity analysis [5]-[9]. In [5], knowledge-based neural network for on-chip interconnects is investigated. Eye-width prediction using S-parameter based on ANNs is proposed in [6]. In [7], height of the eyediagram is estimated using artificial neural network for USB 3.0-based models. Recently, an efficient modeling using knowledge-based neural networks for analysis of PSIJ and PSIJ transfer function in CMOS inverters is presented in [8] and [9], respectively.

In this paper, analysis in [9] is further advanced to estimate PSIJ in the presence of power supply noise. For this purpose, knowledge-based neural network via deep belief neural network [10] and [11] is developed. The primary benefit of this approach is that it eliminates the process of retraining for each case of varying input noise, as in [9]. Also, the training process in [9] starts with a random initialization of weights for multilayer perceptron (MLP) neural networks which may lead to slower convergence and the training process can get trapped in local optima. The proposed model also eliminates random initialization of weights to achieve global optimization by employing an unsupervised learning technique. Results from a case study of inverters based on 22 nm CMOS technology [12] demonstrate that the proposed model predicts the PSIJ with reasonable accuracy while ensure the faster convergence.

II. Development of the proposed approach for the analysis of power supply induced jitter

In this section, an efficient model for predicting PSIJ using deep belief and knowledge-based neural networks is presented. For the development of the purposed hybrid neural network model, an application of a CMOS inverter is considered as shown in Fig. 1. Both the transistors, NMOS (M_n) and PMOS (M_p) are connected to a load capacitor (C_L) and a data input $(v_{in}(t))$. The noise source $(v_n(t))$ is also injected into the system, connected to a supply voltage (V_{DD}).

The traditional approach for PSIJ analysis associated with CMOS inverters requires thousands of SPICE based transient simulations for a reasonable PSIJ estimation which can make the process prohibitively CPU expensive.

On the other hand, MLP-based neural networks can be significantly more efficient [9] than traditional approaches since they can approximate any non-linear complex function. However, there are some drawbacks to consider such as random initialization of the network's parameters (weights and biases) that can effect the scalability of the networks; training process can also get trapped in local optima [10] since the PSIJ response at the output of CMOS inverter is highly nonlinear with multiple minima and maxima. Therefore, an efficient and accurate training process is required that can determine the

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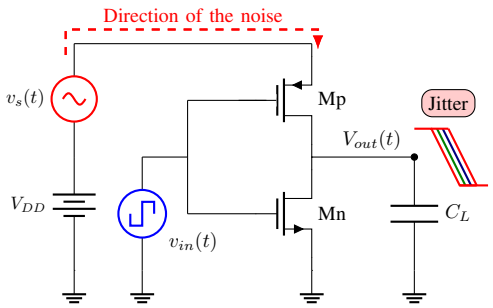

Fig. 1: CMOS inverter with PSN and load capacitor

suitable initial weights while eliminating the learning process to terminate at local optima, as discussed in the following section.

A. Deep Belief Neural Network (DBNN)

Deep belief neural networks are multi-layer probabilistic generative models that can learn to extract a deep hierarchical nonlinear representation of the training data in an unsupervised manner. A DBNN model is a collection of stacked RBMs (Restricted Boltzmann Machines) where the output of the previous RBM is considered as the input of the next RBM as shown in Fig. 2. All the RBMs are sequentially trained via unsupervised learning approach in order to obtain initial weights $(W_1, \ldots, W_4)$. This training process pretrains the weights in a systematic way and has an advantage over random initialization of weights that leads to a faster convergence to achieve global optimization.

For unsupervised training, contrastive divergence (CD) algorithm is used to train these multiple RBMs. The CD algorithm [10] uses energy function associated with RBMs to optimize the corresponding probability distribution in order to update the weight parameters.

Once all the RBMs are trained, an additional layer of neurons which represents the output of deep belief neural network is added for the purpose of supervised learning (Fig. 2). In this process, weights obtained using unsupervised training are further adjusted in order to improve the detection performance of the network while obtaining the global minimum. Note that, a single neuron is used as an additional layer since PSIJ is evaluated only at the output of CMOS inverter.

For supervised learning, the Levenberg-Marquardt (LM) algorithm [9] is used to fine-tune the network's parameters. The LM algorithm propagates error information from the output layer to the input layer and updates the parameters accordingly.

B. Proposed Hybrid Neural Network Model using Deep Belief and Knowledge-based Neural Networks (DB-KBNN)

In this section, knowledge-based neural network developed in [9] is advanced via deep belief network for PSIJ analysis. First, an error vector is calculated using both, fast-to-evaluate analytical model for PSIJ [4] and CPU expensive circuit simulator (HSPICE). The error vector can be written as: $\vec{J}_E = \vec{J}_H - \vec{J}_A$ where $\vec{J}_A$ and $\vec{J}_H$ are the PSIJ responses (training data) associated with analytical model and HSPICE, respectively. Note that, HSPICE gives accurate PSIJ response.

Next, DBNN is trained employing $\vec{J}_E$. Once DBNN is trained, the error response can be evaluated at any given input. The DBNN-based error response is referred to as, $\vec{J}_{DB}$.

Next, the final PSIJ response $(\vec{J})$ is obtained for any given input by combining both, the analytical response as well as the DBNN-based error response, given as $\vec{J} = \vec{J}_{DB} + \vec{J}_A$.

Since norm of $\vec{J}_E$ is usually smaller than the norm of $\vec{J}_A$ and $\vec{J}_H$, the training process can be considerably efficient. Hence, additional layer of knowledge employed by KBNN via analytical relations accelerates the training process.

C. Data Generation and Training of the Proposed Model

In this section, the proposed model is trained using an appropriate set of training data.

Let the input $(\vec{I})$ of the proposed model be defined as: $\vec{I} = [A_s \;\; f_s \;\; \phi_s \;\; C_L]^T$ where A_s, f_s and ϕ_s represent amplitude, frequency and phase angle of power supply noise $(v_s(t))$, respectively. The corresponding lower and upper limits for parameters related to I are: $0 \leq A_n \leq 100\ mV$, $10MHz \leq f_s \leq 1\ GHz$, $0^\circ \leq \phi_s \leq 360^\circ$ and $0 \leq C_L \leq 250\ fF$.

In this work, training data for input I is divided into two sets. The first set of data contains equally spaced input samples and holds 20% of the total data. For the second set, input is randomly distributed and contains 80% of the total data.

The data set based on equally spaced samples provides a discrete nonlinear PSIJ spectrum with varying frequencies. In this process, PSIJ is evaluated at midpoint of the desired input range $(I/2)$. Note that, 20% of the data gives good approximation of the PSIJ spectrum. For the second set, PSIJ is evaluated when input parameters related to I are randomly distributed by applying a uniform distribution.

The PSIJ spectrum is generated at the midpoint of the desired range $I/2$ in order to allow for an even distribution of random samples. Since PSIJ spectrum provides a discrete nonlinear pattern with varying frequencies, it can be considered as an ideal reference plane. On the other hand, generating data based on random sample injects PSIJ variations in the network.

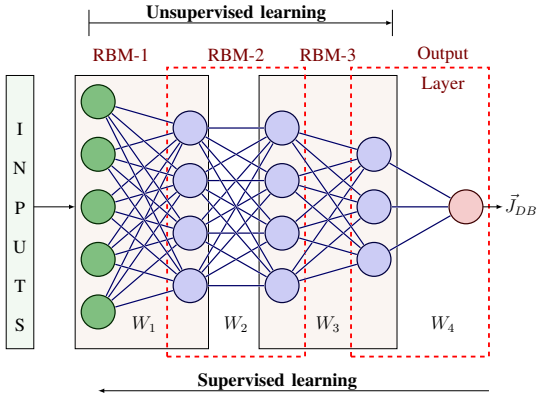

Fig. 2: Structure of DBNN with three RBMs.

This gives information on how the PSIJ is varying with respect to the reference (PSIJ spectrum). Note that, the above analysis is used to generate PSIJ responses for both analytical model and HSPICE for the purpose of calculating error vector $\vec{J}_E$, which is then used to train DBNN.

III. Results and Discussion

In this section, the proposed methodology to predict power supply induced jitter is validated. For this purpose, CMOS circuit operating at 125 MHz with a DC supply voltage (VDD) of 1.2V is considered. While obtaining the PSIJ training data, either using HSPICE or analytical expressions, PSIJ is computed over 500 bits.

In this experiment, a single-tone noise of 311 MHz is applied on the power supply of a CMOS inverter having 10 fF load capacitor. Both, amplitude and phase of the noise source are varied simultaneously from 0 to 100 mV and 0° to 275° with a step size of 4 mV and 8 °, respectively.

In the training process, a total of 50 training data points are generated and 2 RBMs with 6 hidden neurons in each layer are considered. The training time using the CD algorithm is 0.1 sec and 107 epochs are required to achieve a training error of 10^{-10}. Using pretrained weights from unsupervised learning, training via LM algorithm requires only 5 epochs to achieve an error of 10^{-12} in 0.001 sec. Thus, optimizing the initial weights using unsupervised learning not only provides a good initial guess but also assists supervised learning to calculate global optimization in an efficient manner.

For comparison purpose, ANN developed in [9] is trained using a similar structure as used for the proposed approach. Based on random initialization, training time using the LM algorithm is 0.14 sec and 115 epochs are required to achieve an error of 10^{-12}.

The corresponding PSIJ responses for all the four approaches, the proposed model, closed-form expressions [4], MLP-based neural network [9] and approach directly using HSPICE are shown in Fig. 3. As can be seen, the proposed approach matches reasonably well with the conventional approach more accurately compared to analytical and MLP-based responses, while achieving a speed up of 261 compared to HSPICE with a relative error of 0.98%.

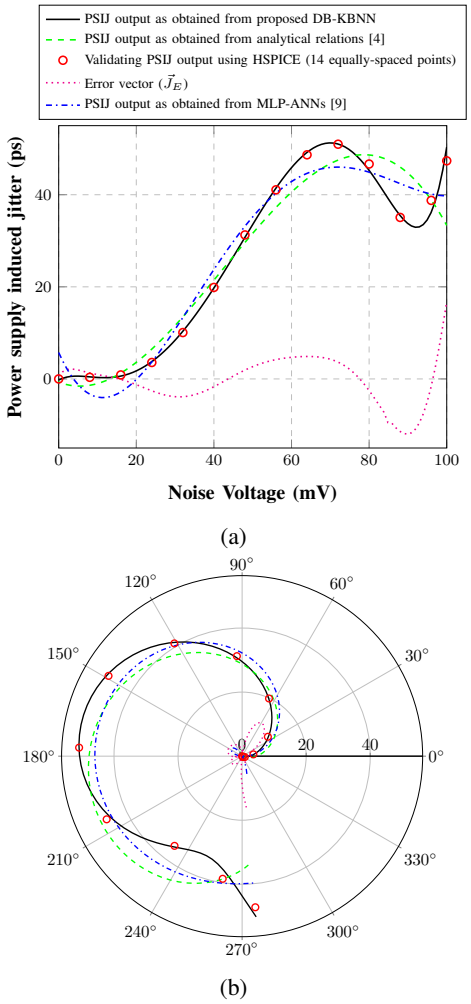

Fig. 3: Comparison of PSIJ responses: (a) Comparison of PSIJ vs. noise voltage, (b) Comparison of PSIJ vs. phase angle

IV. Conclusions

In this paper, knowledge-based neural network is combined with deep belief network to develop an efficient method that predicts reasonably accurate PSIJ response. Validating example demonstrates the efficiency and accuracy of the proposed model while ensure the faster convergence.

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